



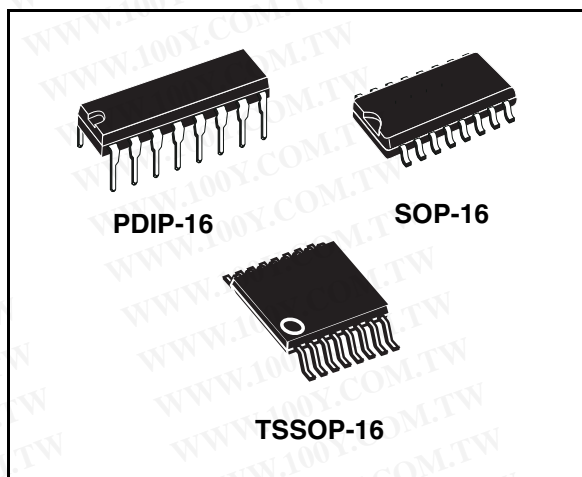
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## M74HC4051

### Single 8-channel analog multiplexer/demultiplexer

#### Features

- Low power dissipation:
  - $I_{CC} = 4 \mu\text{A}(\text{max})$  at  $T_A = 25^\circ\text{C}$
- Logic level translation to enable 5 V logic signal to communicate with  $\pm 5$  V analog signal
- Low ON resistance:
  - $70 \Omega$  typ ( $V_{CC} - V_{EE} = 4.5$  V)
  - $50 \Omega$  typ ( $V_{CC} - V_{EE} = 9$  V)
- Wide analog input voltage range :  $\pm 6$  V
- Fast switching:
  - $t_{pd} = 15$  ns (typ) at  $T_A = 25^\circ\text{C}$
- Low crosstalk between switches
- High ON/OFF output voltage ratio
- Wide operating supply voltage range ( $V_{CC} - V_{EE}$ ) = 2 to 12 V
- Low sine wave distortion:
  - 0.02% at  $V_{CC} - V_{EE} = 9$  V
- High noise immunity:
  - $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Pin and function compatible with 74 series 4051



#### Description

The M74HC4051 is a single 8-channel analog multiplexer/demultiplexer fabricated with silicon gate  $C^2$ MOS technology, pin-to-pin compatible with the equivalent metal gate CMOS4000B series. It contains 8 bidirectional and digitally controlled analog switches.

A built-in level shifting is included to allow an input range up to  $\pm 6$  V (peak) for an analog signal with digital control signal of 0 to 6 V.

The  $V_{EE}$  supply pin is provided for analog input signals. It has an inhibit (INH) input terminal to disable all the switches when is at high level. For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND.

A, B and C control inputs select one channel out of eight. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
M74HC4051RM13TR	SOP-16	Tape and reel
M74HC4051TTR	TSSOP-16	Tape and reel

# 1 Pin connection and IEC logic symbols

Figure 1. Pin connection

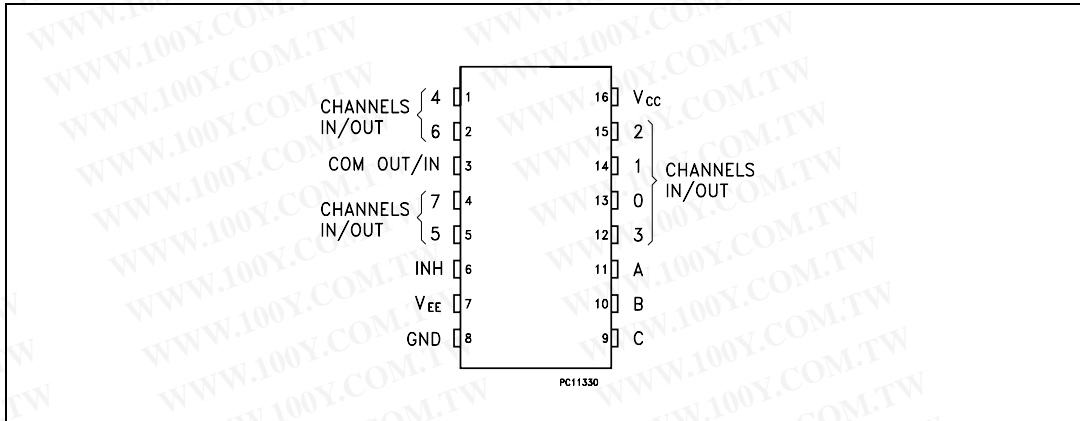
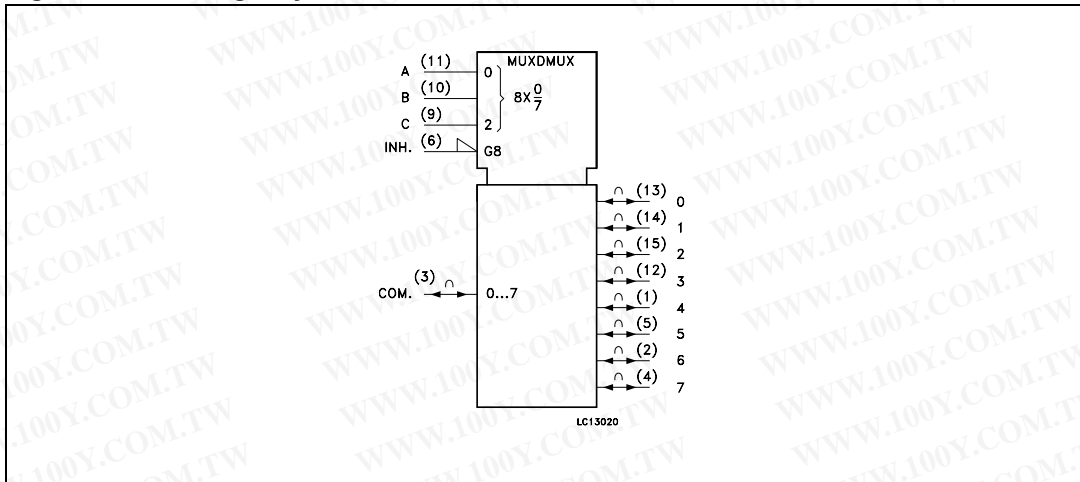


Figure 2. IEC logic symbols



## 1.1 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
3	COM OUT/IN	Common output/input
6	INH	Inhibit input
7	V <sub>EE</sub>	Negative supply voltage
11, 10, 9	A, B, C	Select inputs
13, 14, 15, 12, 1, 5, 2, 4	0 to 7	Independent input/outputs
8	GND	Ground (0 V)
16	V <sub>CC</sub>	Positive supply voltage

Figure 3. Control input equivalent circuit

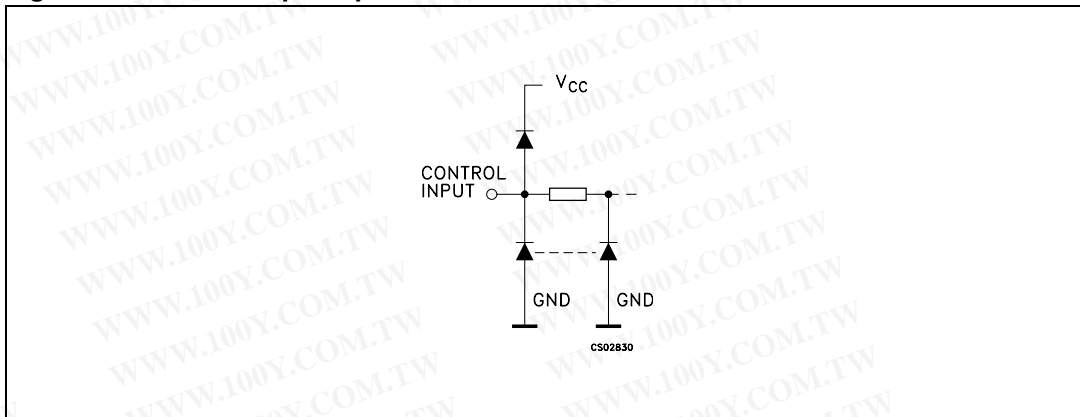


Figure 4. I/O equivalent circuit

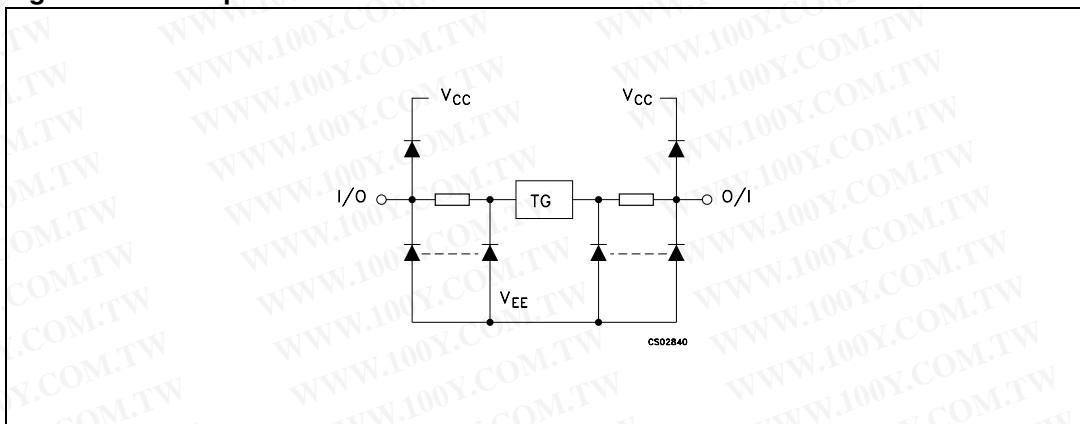
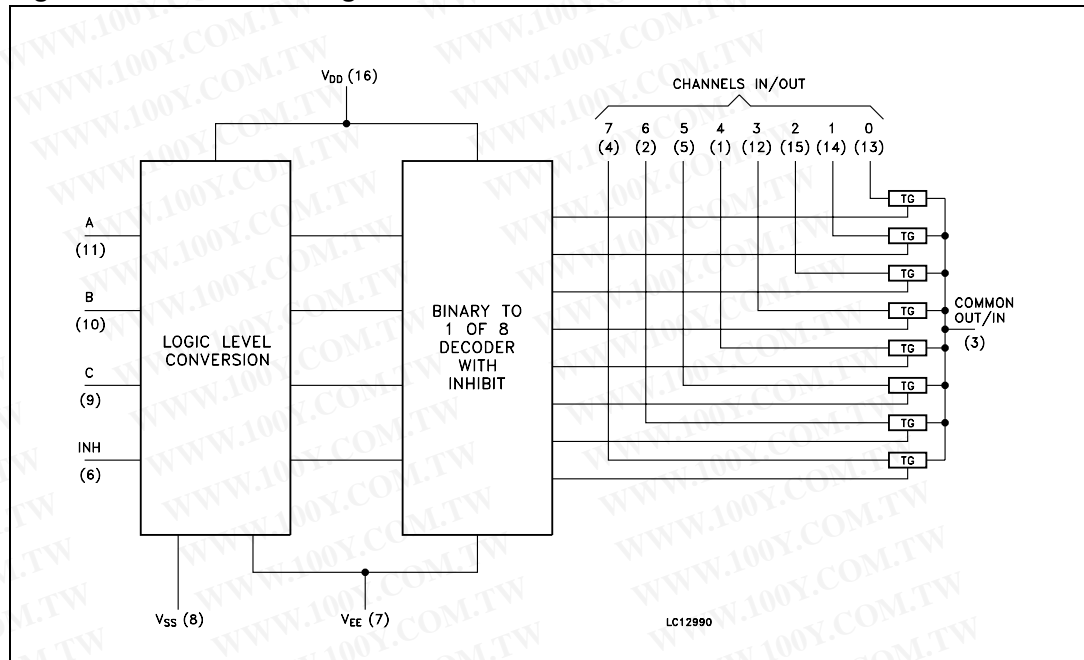


Table 3. Truth table

Input state				ON channel
INH	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	NONE

x: Don't care

Figure 5. Functional diagram



## 2 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage	-0.5 to +7	V	
$V_{CC} - V_{EE}$	Supply voltage	-0.5 to +13	V	
$V_I$	Control input voltage	-0.5 to $V_{CC} + 0.5$	V	
$V_{I/O}$	Switch I/O voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V	
$I_{CK}$	Control input diode current	$\pm 20$	mA	
$I_{IOK}$	I/O diode current	$\pm 20$	mA	
$I_T$	Switch through current	$\pm 25$	mA	
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or ground current	$\pm 50$	mA	
$P_D$	Power dissipation	DIP-16	500 <sup>(1)</sup>	mW
		SOP-16 and TSSOP-16	180	mW
$T_{stg}$	Storage temperature	-65 to +150	°C	
$T_L$	Lead temperature (10 sec)	300	°C	

1. 500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65 °C to 85 °C

**Table 5. Recommended operating conditions**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage	2 to 6	V	
$V_{EE}$	Supply voltage	-6 to 0	V	
$V_{CC} - V_{EE}$	Supply voltage	2 to 12	V	
$V_I$	Input voltage	0 to $V_{CC}$	V	
$V_{I/O}$	I/O voltage	$V_{EE}$ to $V_{CC}$	V	
$T_{op}$	Operating temperature	-55 to 125	°C	
$t_r, t_f$	Input rise and fall time	$V_{CC} = 2.0$ V	0 to 1000	ns
		$V_{CC} = 4.5$ V	0 to 500	
		$V_{CC} = 6.0$ V	0 to 400	



Table 6. DC electrical specifications

Symbol	Parameter	Test condition		Value						Unit		
		V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	T <sub>A</sub> = 25 °C			-40 to 85 °C		-55 to 125 °C			
				Min	Typ	Max	Min	Max	Min		Max	
V <sub>IHC</sub>	High level input voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V <sub>ILC</sub>	Low level input voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
R <sub>ON</sub>	ON resistance	4.5	GND	V <sub>I</sub> = V <sub>IHC</sub> or V <sub>ILC</sub> V <sub>I/O</sub> = V <sub>CC</sub> to V <sub>EE</sub> I <sub>I/O</sub> ≤ 2mA		85	180		225		270	W
		4.5	-4.5			55	120		150		180	
		6.0	-6.0			50	100		125		150	
		2.0	GND		150							
		4.5	GND	V <sub>I</sub> = V <sub>IHC</sub> or V <sub>ILC</sub> V <sub>I/O</sub> = V <sub>CC</sub> or V <sub>EE</sub> I <sub>I/O</sub> ≤ 2mA		70	150		190		230	
		4.5	-4.5			50	100		125		150	
6.0	-6.0		45		80		100		120			
ΔR <sub>ON</sub>	Difference of ON resistance between switches	4.5	GND	V <sub>I</sub> = V <sub>IHC</sub> or V <sub>ILC</sub> V <sub>I/O</sub> = V <sub>CC</sub> or V <sub>EE</sub> I <sub>I/O</sub> ≤ 2mA		10	30		35		45	W
		4.5	-4.5			5	12		15		18	
		6.0	-6.0			5	10		12		15	
I <sub>OFF</sub>	Input/output leakage current (switch off)	6.0	GND	V <sub>OS</sub> = V <sub>CC</sub> or GND V <sub>IS</sub> = GND or V <sub>CC</sub> V <sub>I</sub> = V <sub>ILC</sub> or V <sub>IHC</sub>			±0.06		±0.6		±1.2	μA
		6.0	-6.0				±0.1		±1		±2	
I <sub>Iz</sub>	Switch input leakage current (switch on, output open)	6.0	GND	V <sub>OS</sub> = V <sub>CC</sub> or GND V <sub>I</sub> = V <sub>IHC</sub> or V <sub>ILC</sub>			±0.06		±0.6		±1.2	μA
		6.0	-6.0				±0.1		±1		±2	
I <sub>I</sub>	Input leakage current	6.0	GND	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±0.1		±1	μA
I <sub>CC</sub>	Quiescent supply current	6.0	GND	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA
		6.0	-6.0				8		80		160	

**Table 7. AC electrical characteristics** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	Test condition			Value						Unit	
		$V_{CC}$ (V)	$V_{EE}$ (V)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
					Min.	Typ	Max	Min	Max	Min		Max
$\Phi_{I/O}$	Phase difference between input and output	2.0	GND			25	60		75		90	ns
		4.5	GND			6	12		15		18	
		6.0	GND			5	10		13		15	
		4.5	-4.5			4						
$t_{PZL}$ $t_{PZH}$	Output enable time	2.0	GND	$R_L = 1\text{ K}\Omega$		64	225		280		340	ns
		4.5	GND			18	45		56		68	
		6.0	GND			15	38		48		58	
		4.5	-4.5			18						
$t_{PLZ}$ $t_{PHZ}$	Output disable time	2.0	GND	$R_L = 1\text{ K}\Omega$		100	250		315		375	ns
		4.5	GND			33	50		63		70	
		6.0	GND			28	43		54		64	
		4.5	-4.5			29						

**Table 8. Capacitive characteristics**

Symbol	Parameter	Test condition			Value						Unit	
		$V_{CC}$ (V)	$V_{EE}$ (V)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
					Min	Typ	Max	Min	Max	Min		Max
$C_{IN}$	Input capacitance	5.0				5	10		10		10	pF
$C_{I/O}$	Common terminal capacitance	5.0	-5.0			36	70		70		70	pF
$C_{I/O}$	Switch terminal capacitance	5.0	-5.0			7	15		15		15	pF
$C_{IOS}$	Feed through capacitance	5.0	-5.0			0.95	2		2		2	pF
$C_{PD}$	Power dissipation capacitance (1)	5.0	GND			70						pF

1.  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  
 $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

**Table 9. Analog switch characteristics** (GND = 0 V; T<sub>A</sub> = 25°C)

Symbol	Parameter	Test condition			Value	Unit	
		V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	V <sub>IN</sub> (V <sub>p-p</sub> )	Typ		
	Sine wave distortion	2.25	-2.25	4	f <sub>IN</sub> = 1 KHz R <sub>L</sub> = 10 KΩ C <sub>L</sub> = 50 pF	0.025	%
		4.5	-4.5	8		0.020	
		6.0	-6.0	11		0.018	
f <sub>MAX</sub>	Frequency response (Switch on) <sup>(1)</sup>	2.25	-2.25	Adjust f <sub>IN</sub> voltage to obtain 0 dBm at V <sub>OS</sub> . Increase f <sub>IN</sub> Frequency until dB meter reads -3dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF, f <sub>IN</sub> = 1 KHz sine wave	120	MHz	
		4.5	-4.5		190		
		6.0	-6.0		200		
f <sub>MAX</sub>	Frequency response (switch on) <sup>(2)</sup>	2.25	-2.25	Adjust f <sub>IN</sub> voltage to obtain 0 dBm at V <sub>OS</sub> . Increase f <sub>IN</sub> Frequency until dB meter reads -3dB R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10 pF, f <sub>IN</sub> = 1KHz sine wave	45	MHz	
		4.5	-4.5		70		
		6.0	-6.0		85		
	Feed through attenuation (switch off)	2.25	-2.25	V <sub>IN</sub> is centered at (V <sub>CC</sub> - V <sub>EE</sub> )/2 Adjust input for 0 dBm R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF, f <sub>IN</sub> = 1 KHz sine wave	-50	dB	
		4.5	-4.5		-50		
		6.0	-6.0		-50		
	Crosstalk (control input to signal output)	2.25	-2.25	Adjust R <sub>L</sub> at set up so that I <sub>S</sub> = 0A. R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF, f <sub>IN</sub> = 1 KHz square wave	60	mV	
		4.5	-4.5		140		
		6.0	-6.0		200		
	Crosstalk (between any two switches)	2.25	-2.25	Adjust V <sub>IN</sub> to obtain 0d Bm at input R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF, f <sub>IN</sub> = 1 KHz sine wave	-50	dB	
		4.5	-4.5		-50		
		6.0	-6.0		-50		

1. Input common terminal, and measured at switch terminal.

2. Input switch terminal, and measured at common terminal.

These characteristics are determined by the design of the device.



## 2.1 Switching characteristics test circuit

Figure 6. Output enable/disable time

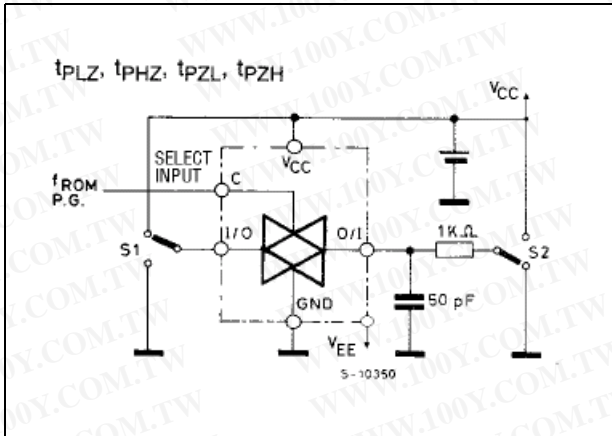


Figure 7. Crosstalk (control to output)

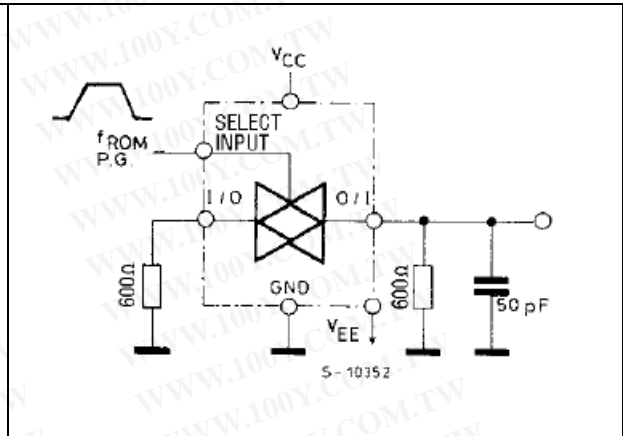


Figure 8. Bandwidth and feedthrough attenuation

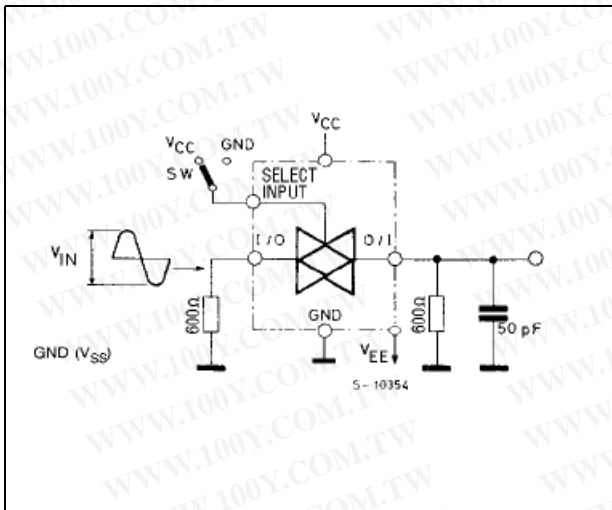


Figure 9. Crosstalk between any two switches

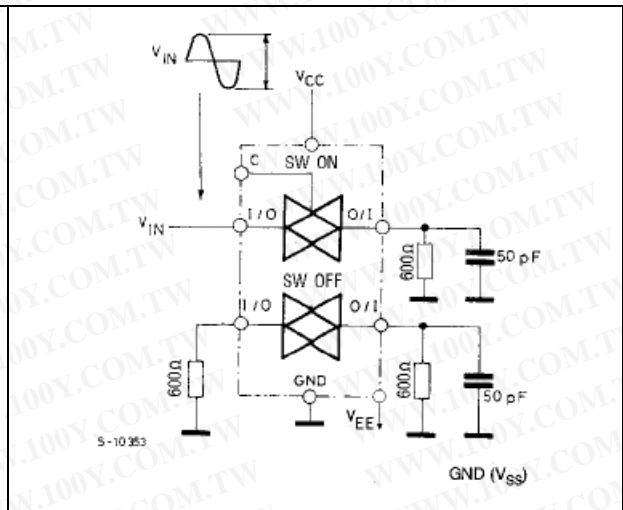


Figure 10. Common terminal capacitance ( $C_{I-O}$ ,  $C_{I/O}$ )

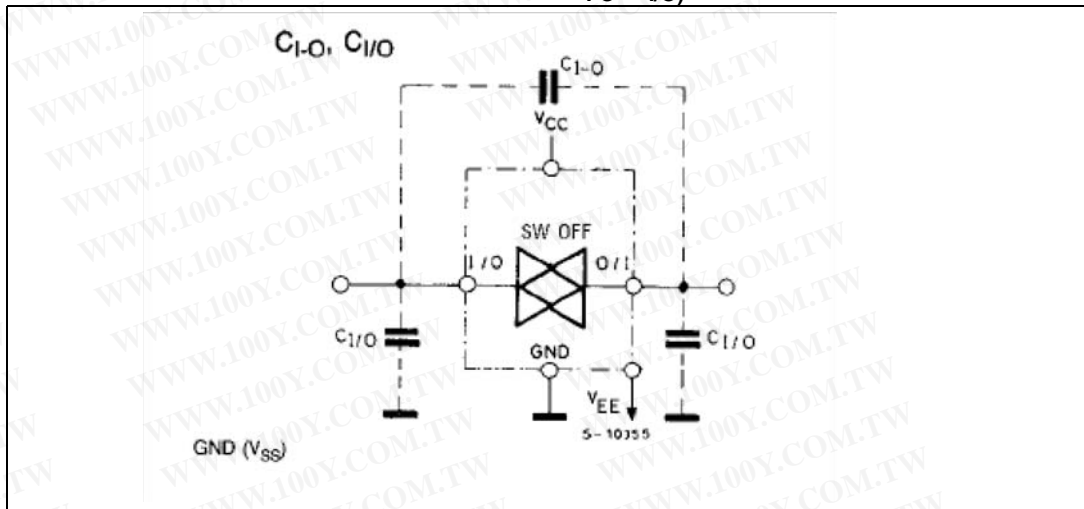


Figure 11. Switching characteristics waveform

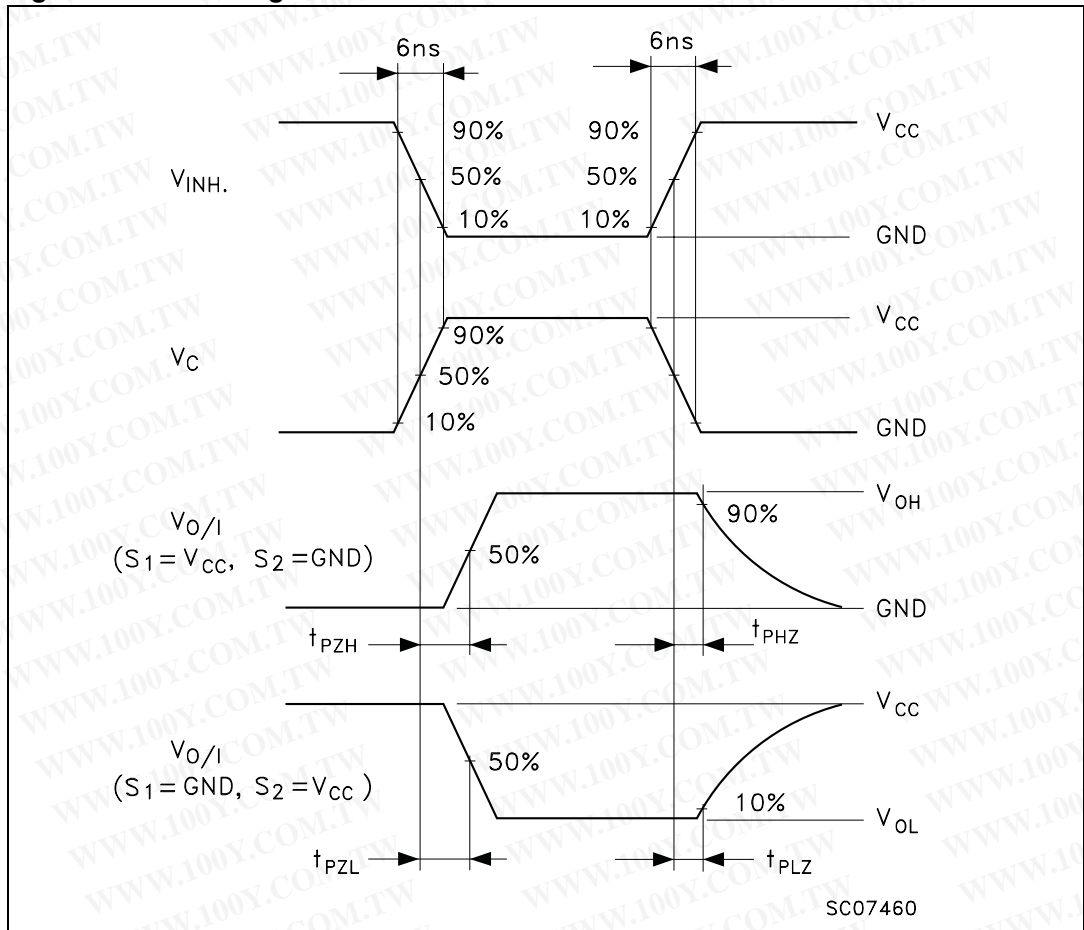


Figure 12. Channel resistance ( $R_{ON}$ )

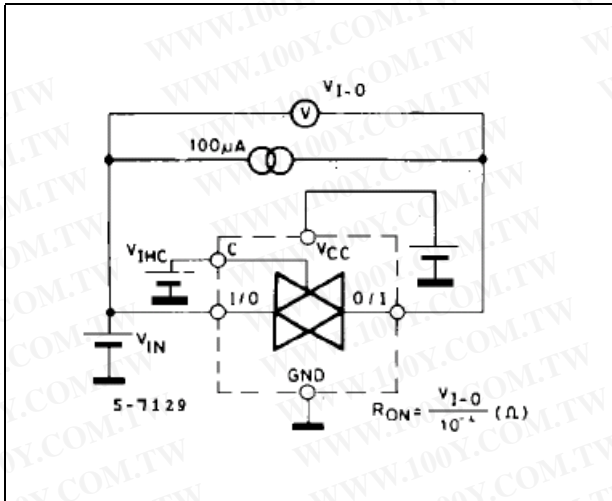
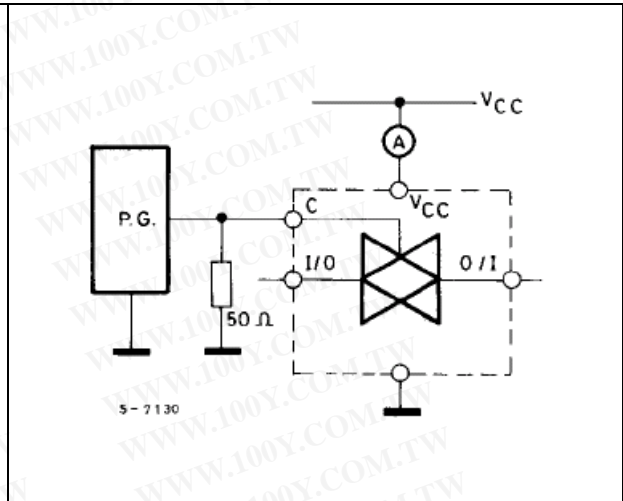


Figure 13. Quiescent supply current -  $I_{CC}$  (opr)



### 3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Figure 14. Plastic DIP-16 (0.25) package information

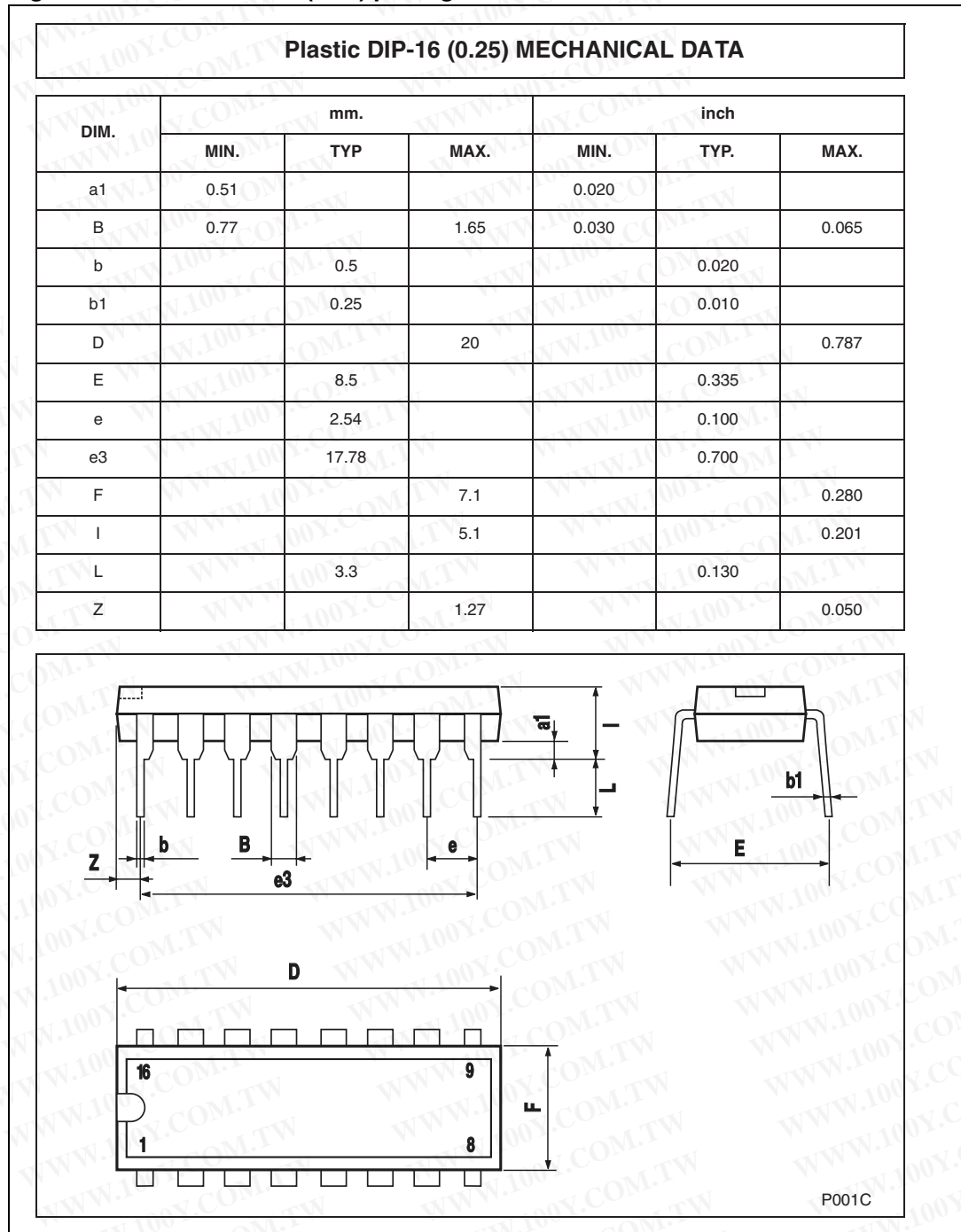




Figure 15. SO-16 package information

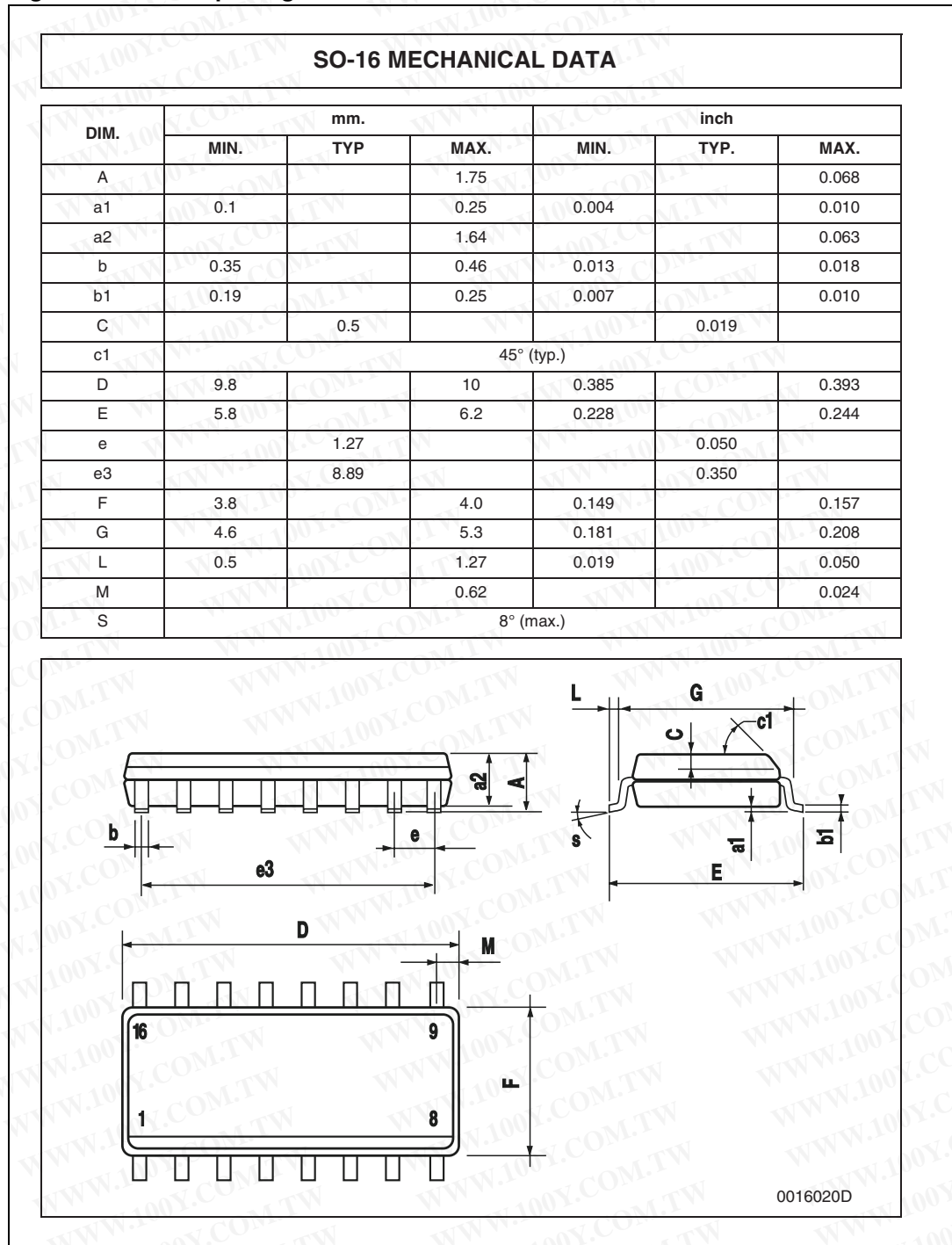
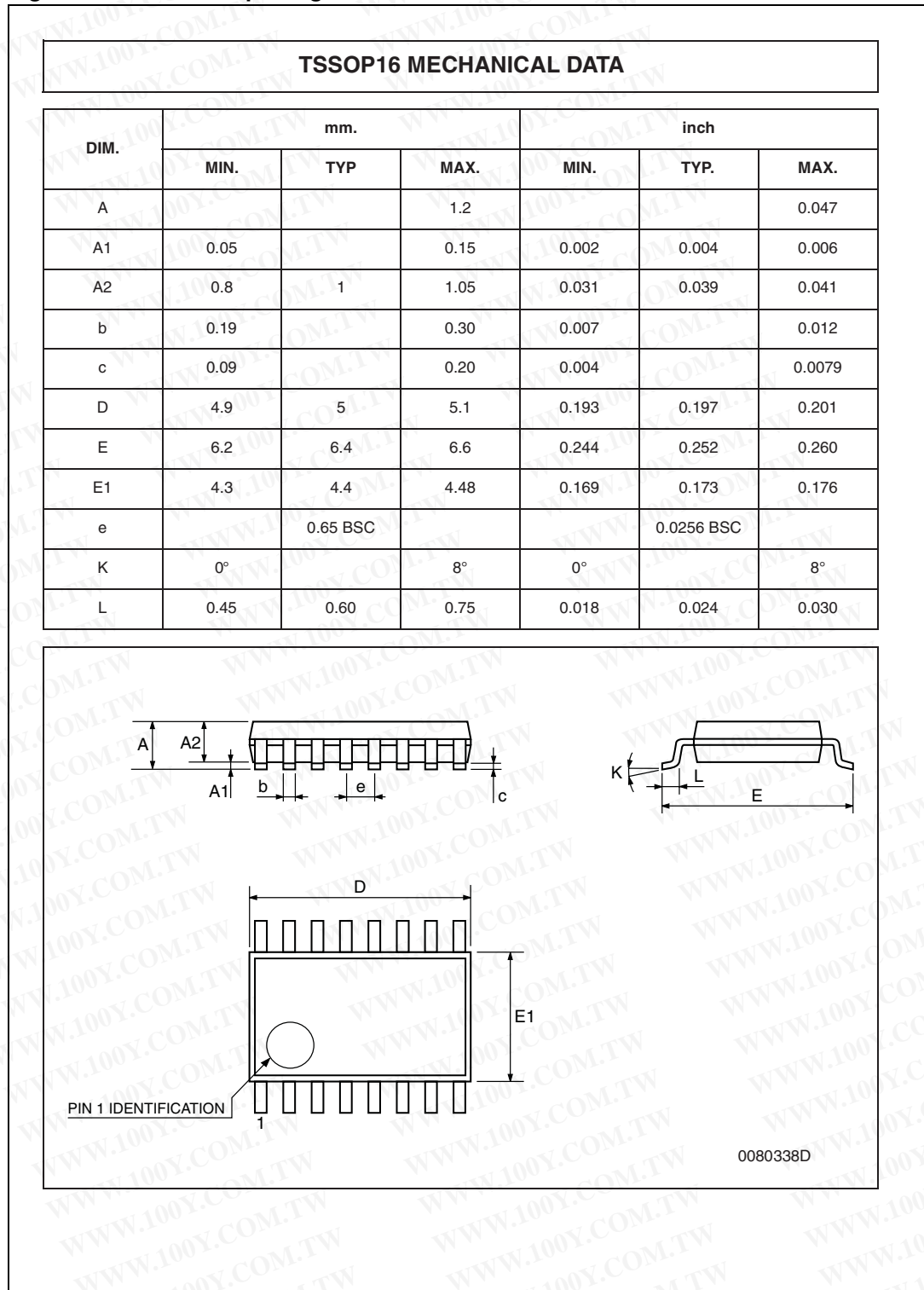


Figure 16. TSSOP16 package information



## 4 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
01-Jul-2001	1	Initial release.
21-June-2004	2	Document internal migration, no content change.
10-Mar-2008	3	Document restructured and converted to new ST template, updated <a href="#">Table 4 on page 5</a> , removed tube packing info.
21-Apr-2008	4	Replaced M74HC4051M13TR with M74HC4051RM13TR in <a href="#">Table 1 on page 1</a> .

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