

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

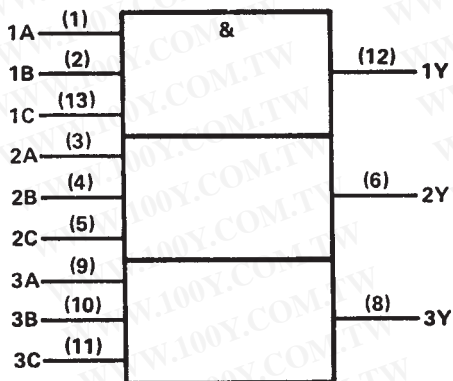
These devices contain three independent 3-input AND gates.

The SN54LS11 and SN54S11 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS11 and SN74S11 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

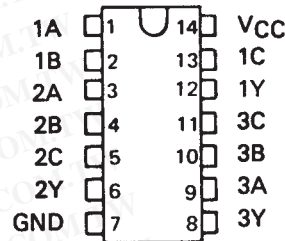
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for D, J, N, and W packages.

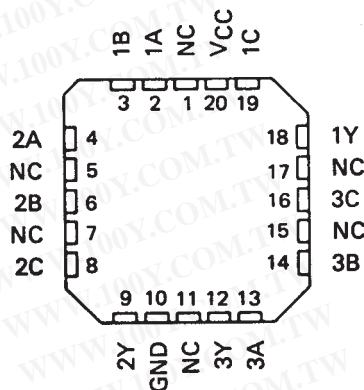
SN54LS11, SN74S11 . . . J OR W PACKAGE
 SN74LS11, SN74S11 . . . D OR N PACKAGE

(TOP VIEW)



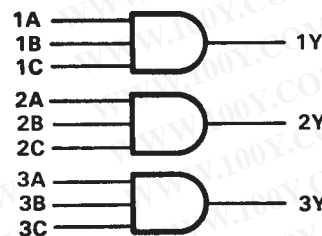
SN54LS11, SN54S11 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



$$Y = A \cdot B \cdot C \text{ or}$$

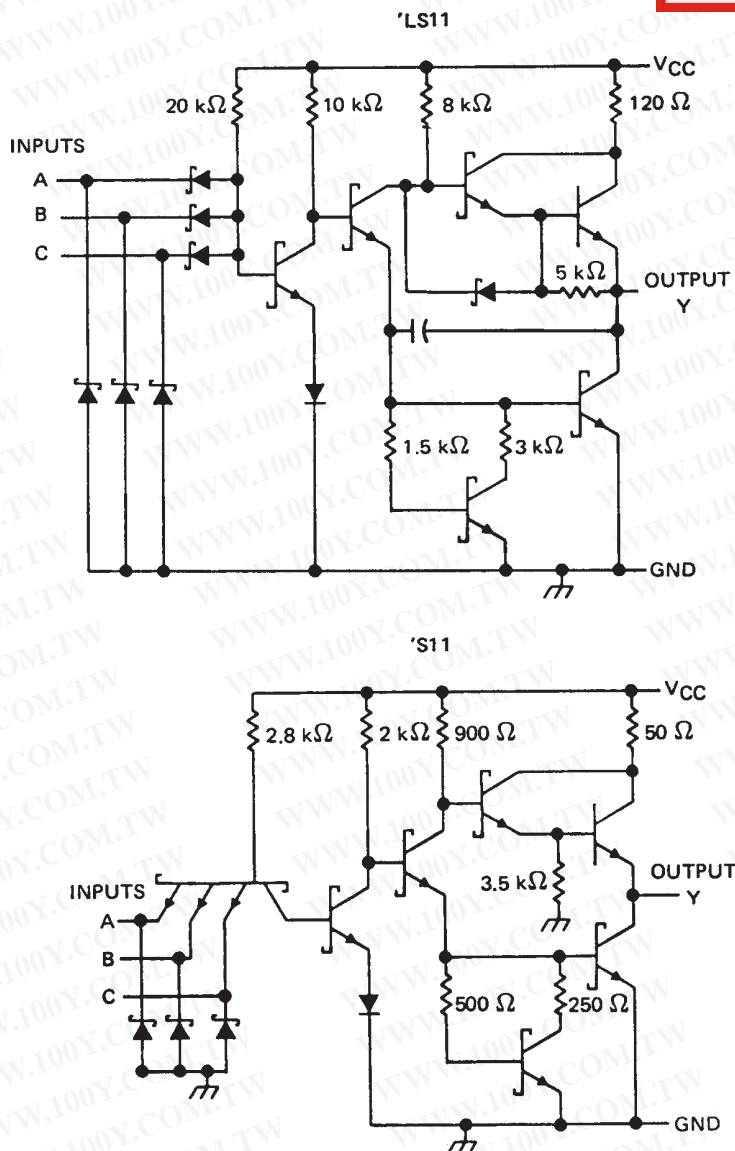
$$Y = \overline{\overline{A} + \overline{B} + \overline{C}}$$

SN54LS11, SN54S11, SN74LS11, SN74S11 TRIPLE 3-INPUT POSITIVE-AND GATES

SDLS131 – APRIL 1985 – REVISED MARCH 1988

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勝特力电子(上海) 86-21-34970699
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'S11	5.5 V
'LS11	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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recommended operating conditions

	SN54LS11			SN74LS11			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			– 0.4			– 0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS11			SN74LS11			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	– 20		– 100	– 20		– 100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	1.8	3.6		1.8	3.6		mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	3.3	6.6		3.3	6.6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		8	15	ns
t_{PHL}					10	20	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



TEXAS
INSTRUMENTS

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SN54LS11, SN54S11,
SN74LS11, SN74S11
TRIPLE 3-INPUT POSITIVE-AND GATES

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recommended operating conditions

	SN54S11			SN74S11			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			– 1			– 1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S11			SN74S11			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = – 18 mA			– 1.2			– 1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = – 1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			– 2			– 2	mA
I _{OS} §	V _{CC} = MAX	– 40		– 100	– 40		– 100	mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V		13.5	24		13.5	24	mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V		24	42		24	42	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 280 Ω, C _L = 15 pF		4.5	7	ns
t _{PHL}					5	7.5	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		6		ns
t _{PHL}					7.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
JM38510/08001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
JM38510/08001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
JM38510/31001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
JM38510/31001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
JM38510/31001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN54LS11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN54S11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN74LS11D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	Samples Not Available
SN74LS11N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74LS11N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	Samples Not Available
SN74LS11NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74LS11NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LS11NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74S11D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	Samples Not Available
SN74S11N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	Samples Not Available
SN74S11N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	Samples Not Available

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SNJ54LS11FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54LS11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54LS11W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54S11FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54S11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54S11W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS11, SN54S11, SN74LS11, SN74S11 :

- Catalog: [SN74LS11](#), [SN74S11](#)

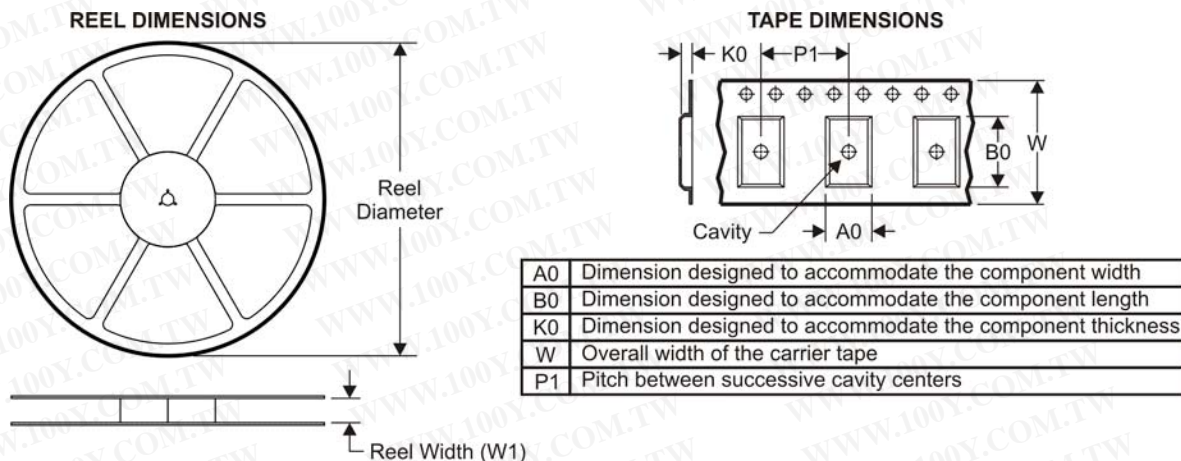
- Military: [SN54LS11](#), [SN54S11](#)

NOTE: Qualified Version Definitions:

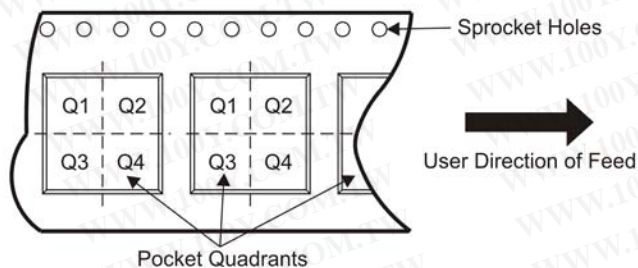
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

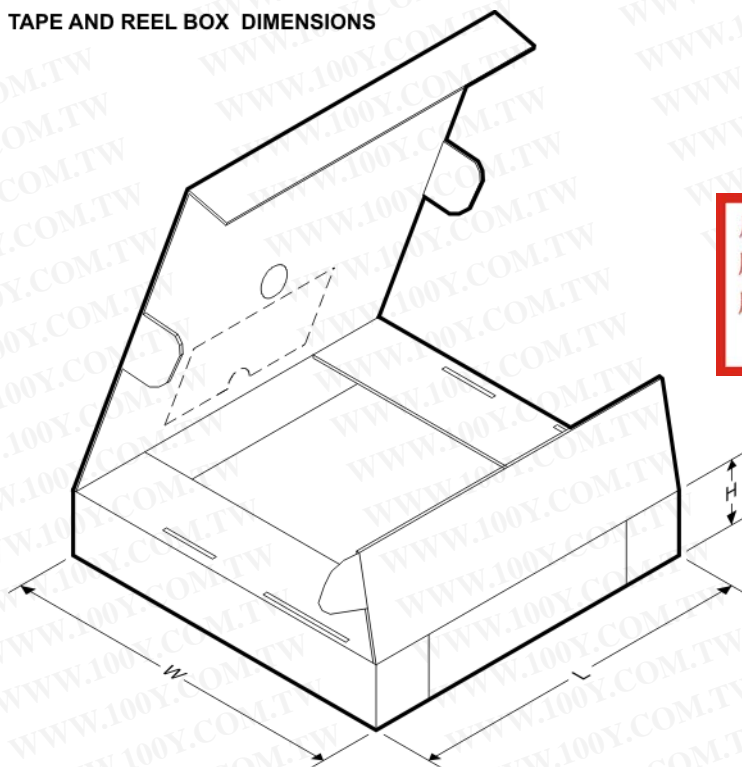


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS11DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS11NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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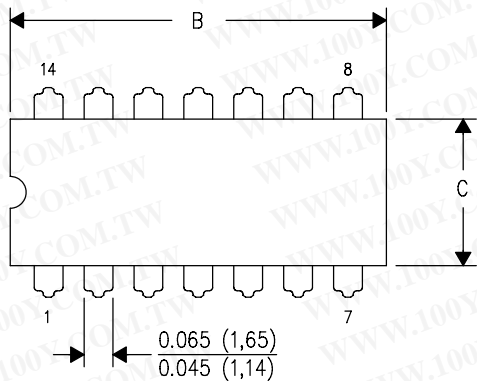
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS11DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS11NSR	SO	NS	14	2000	346.0	346.0	33.0

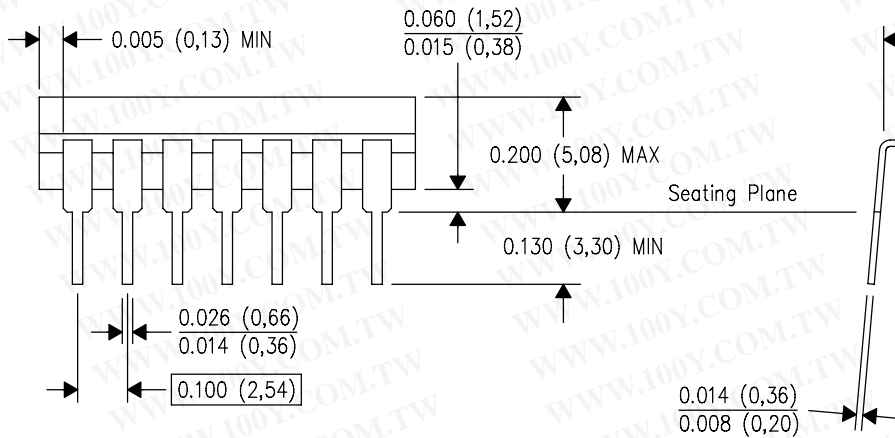
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

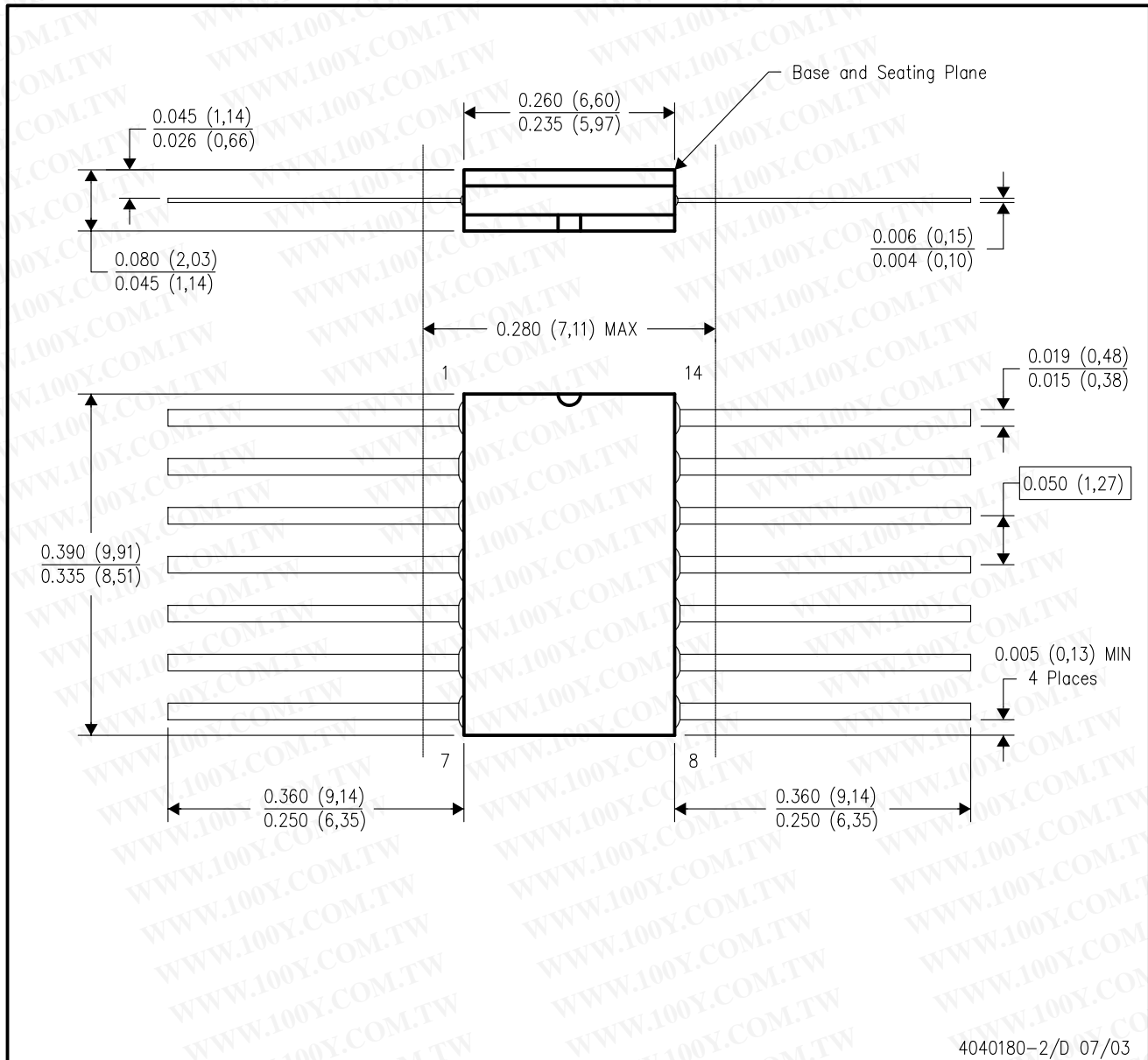


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



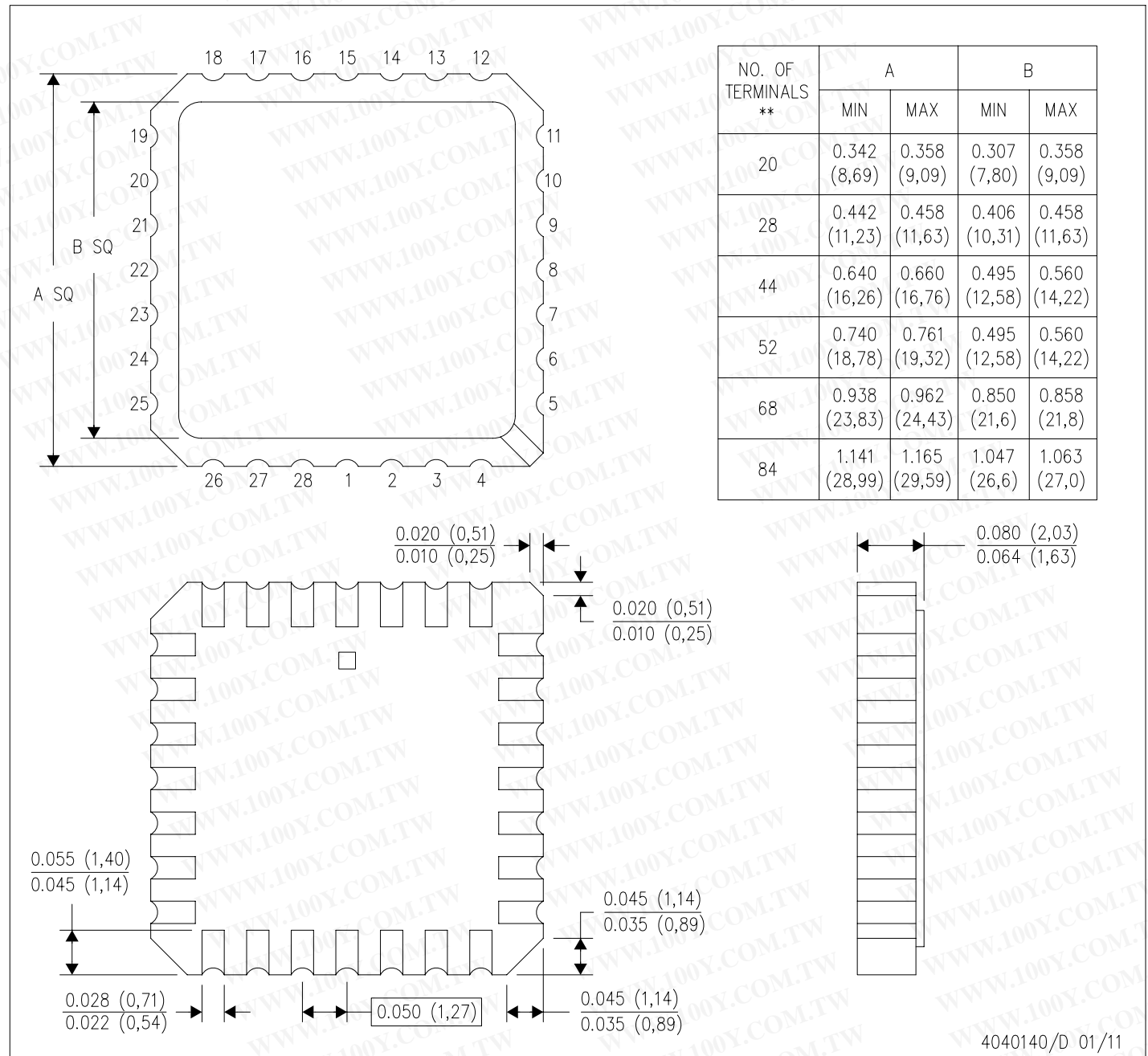
4040180-2/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

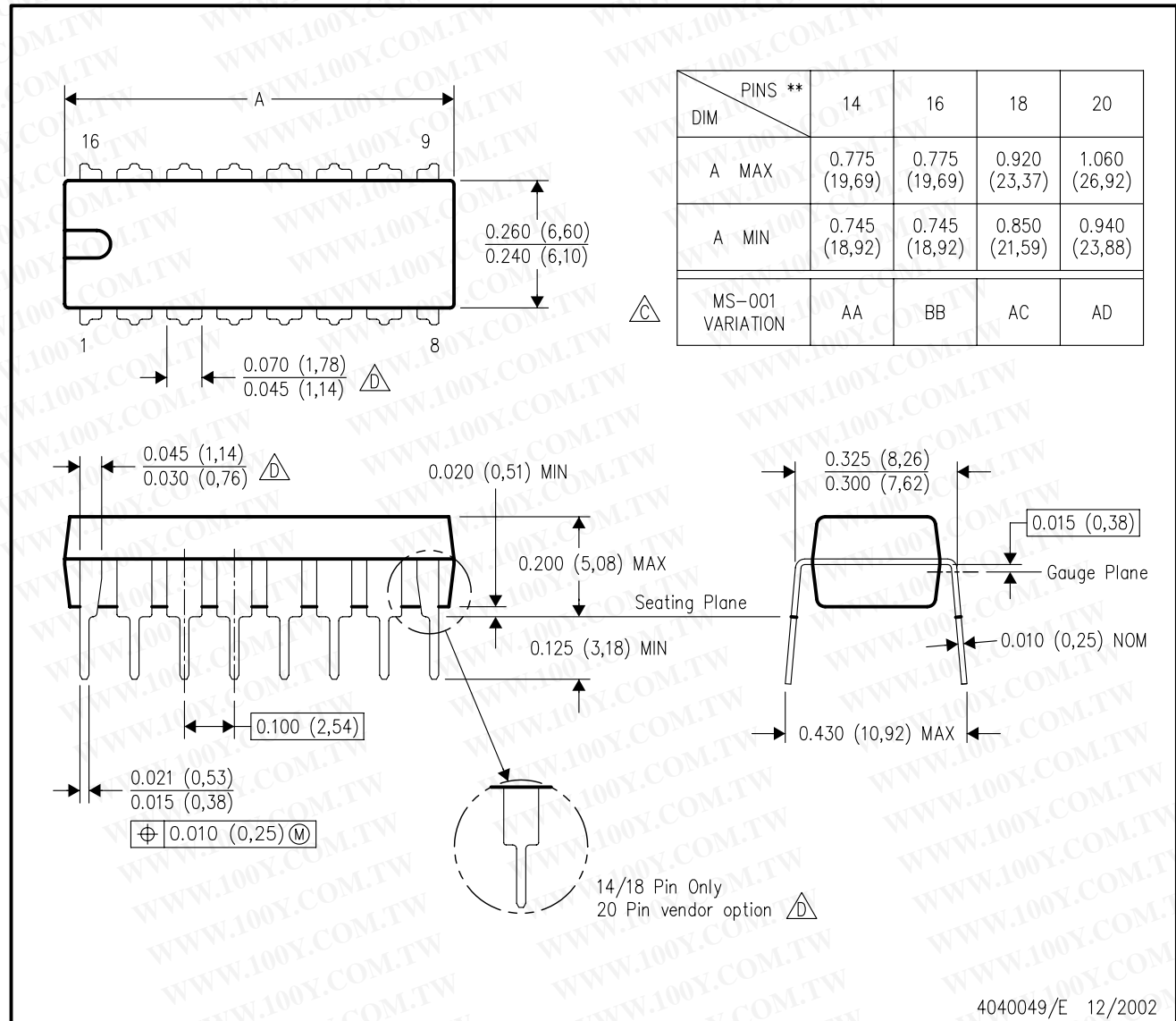


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

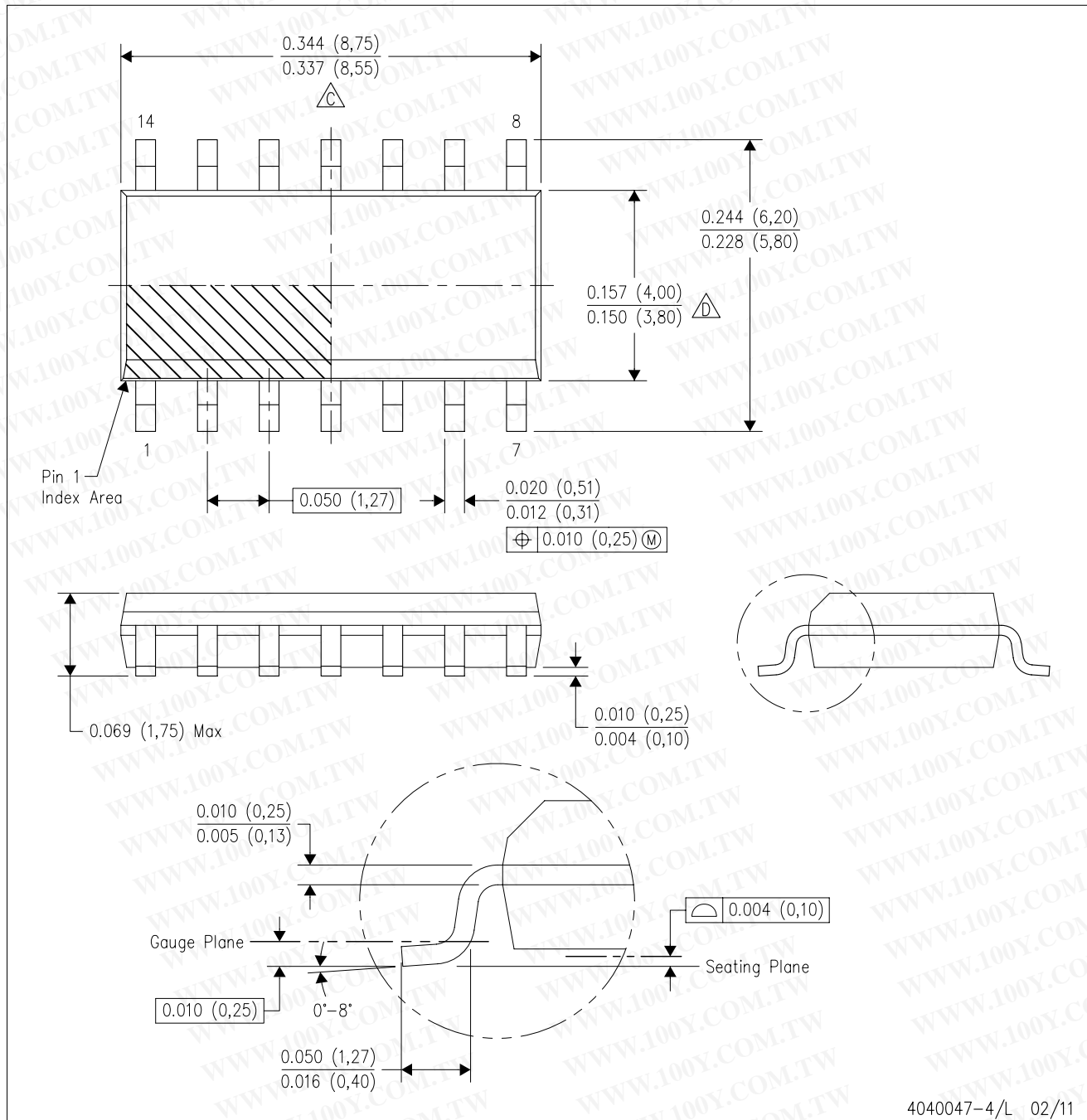
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

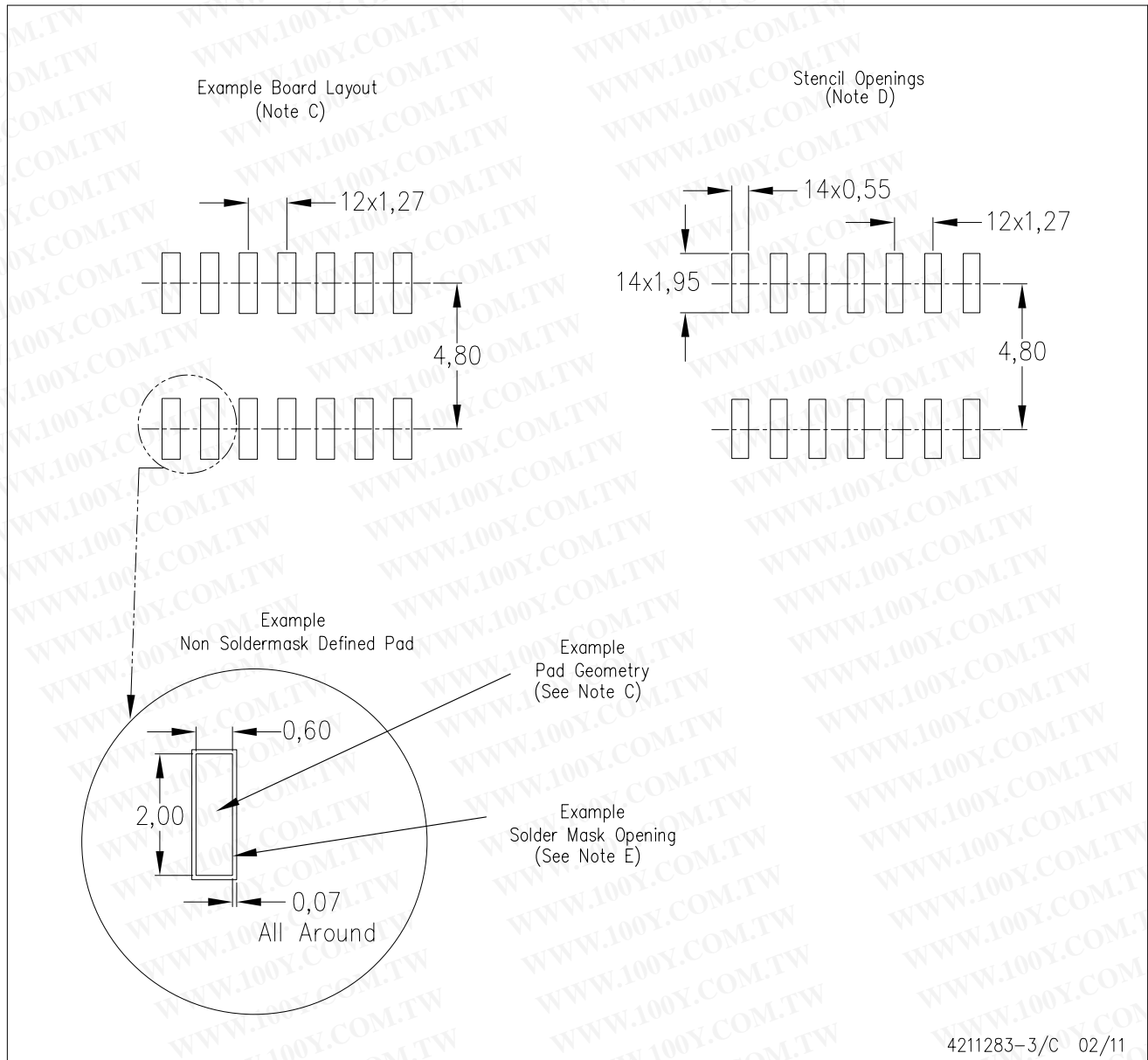
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



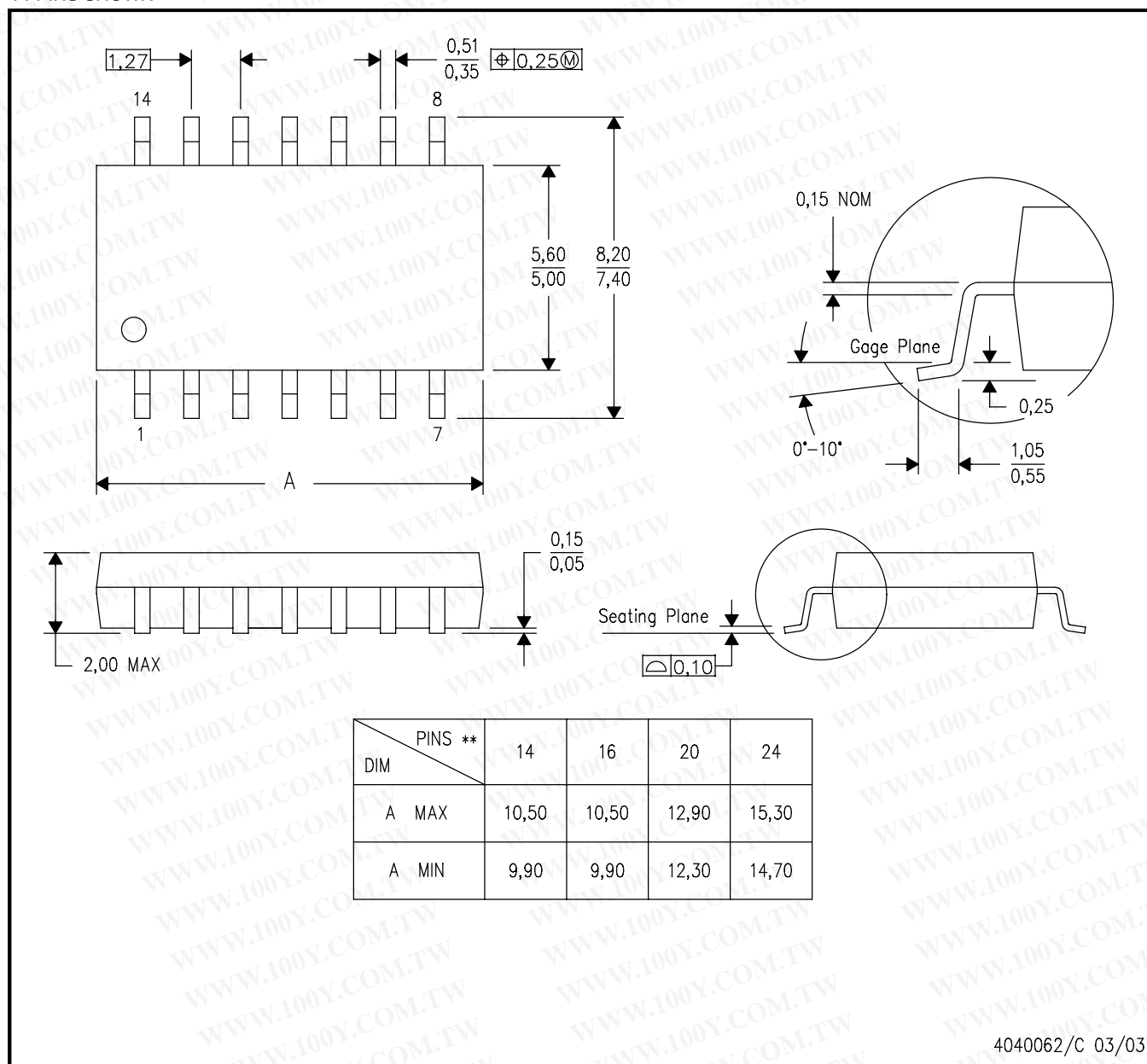
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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