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Features

- Low-voltage and Standard-voltage Operation
  - V_{CC} = 1.7 to 5.5V
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1MHz (5.0V) and 400KHz (1.8V Compatibility)
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Lead-free/Halogen-free Devices
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, 5-lead SOT23 and 8-ball VFBGA
- Die Sales: Wafer Form, Waffle Pack and Bumped Wafers

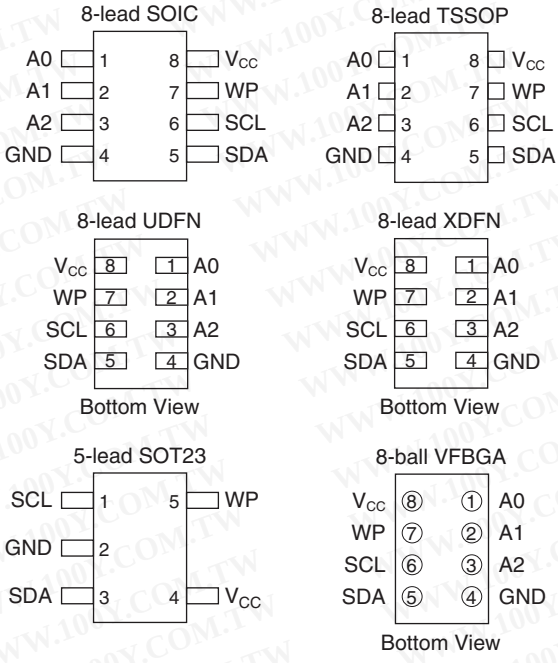
Description

The Atmel® AT24C32D/64D provides 32,768-/65,536-bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8-bits each. The device's cascadable feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32D/64D is available in space saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, 5-lead SOT23 and 8-ball VFBGA and is accessed via a 2-wire serial interface. In addition, the entire family operates from 1.7V to 5.5V.

Table 0-1. Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

Note: For use of 5-lead SOT23, the software A2, A1, and A0 bits in the device address word must be set to zero to properly communicate



2-Wire Serial Electrically Erasable and Programmable Read-only Memory

32K (4096 x 8)

64K (8192 x 8)

Atmel AT24C32D
Atmel AT24C64D

8717B–SEEPR–6/10

1. Absolute Maximum Ratings*

Operating Temperature	-55 to +125°C
Storage Temperature	-65 to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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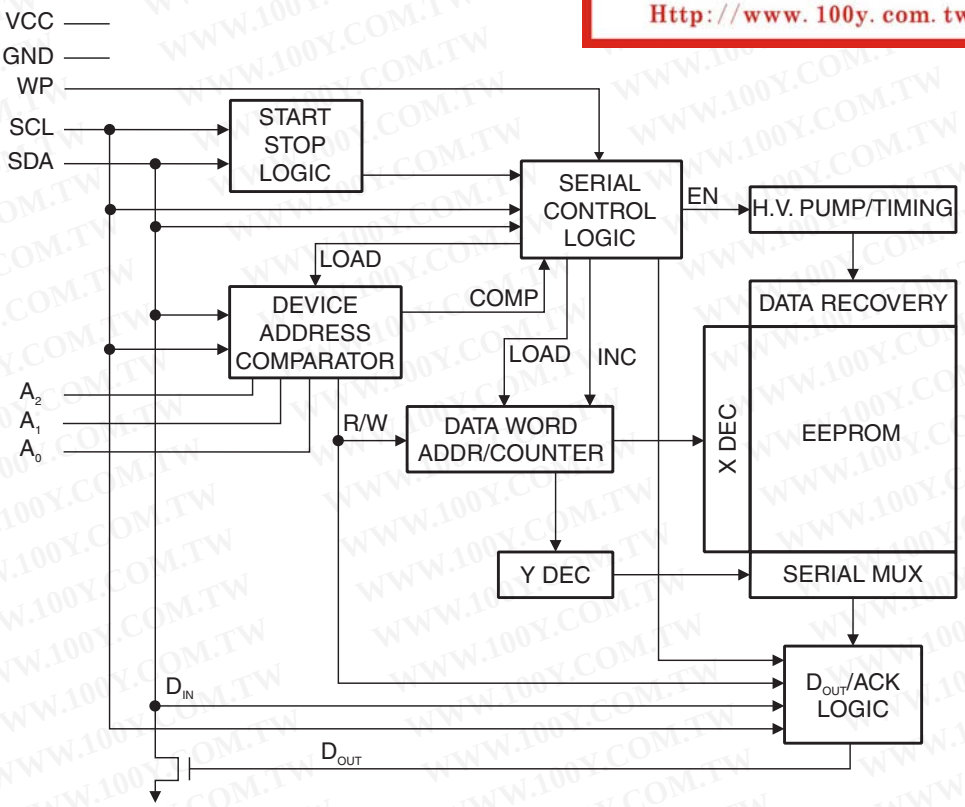
Figure 1-1. Block Diagram



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2. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with other Atmel® AT24CXX devices. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the address pins to GND.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the pin to GND.

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3. Memory Organization

Atmel AT24C32D/64D, 32/64K SERIAL EEPROM: The 32K/64K is internally organized as 128/256 pages of 32-bytes each. Random word addressing requires a 12-/13-bit data word address.

Table 3-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +1.7V to 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested

Table 3-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40 to +85°C, V_{CC} = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current (+1.7V option)	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 5.5V				6.0	µA
I_{LI}	Input Leakage Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current V_{CC} = 5.0V	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested

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Table 3-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted)

Symbol	Parameter	1.7V		5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_i	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3kΩ (2.5V, 5.0V), 10kΩ (1.7V)
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall times: ≤ 50ns
   Input and output timing reference voltages: 0.5 V_{CC}

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4. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to "Data Validity" diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to "Start and Stop Definition" diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to "Start and Stop Definition" diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The Atmel® AT24C32D/64D features a low power standby mode which is enabled:

- Upon power-up
- After the receipt of the Stop bit and the completion of any internal operations.

SOFTWARE RESET: After an interruption in protocol, power loss or system reset, and 2-wire part can be protocol reset by following these steps:

- Create a start bit condition
- Clock nine cycles
- Create another start bit followed by stop bit condition as shown below.

The device is ready for next communication after above steps have been completed.

Figure 4-1. Software Reset

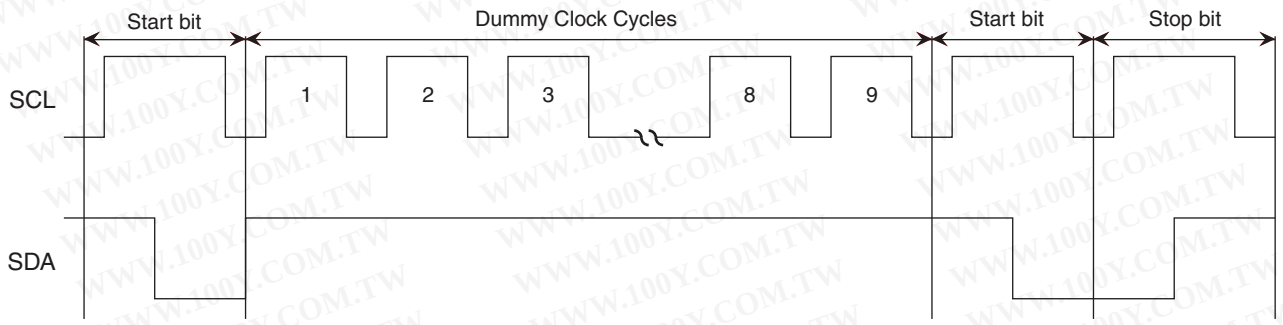

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Figure 4-2. Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

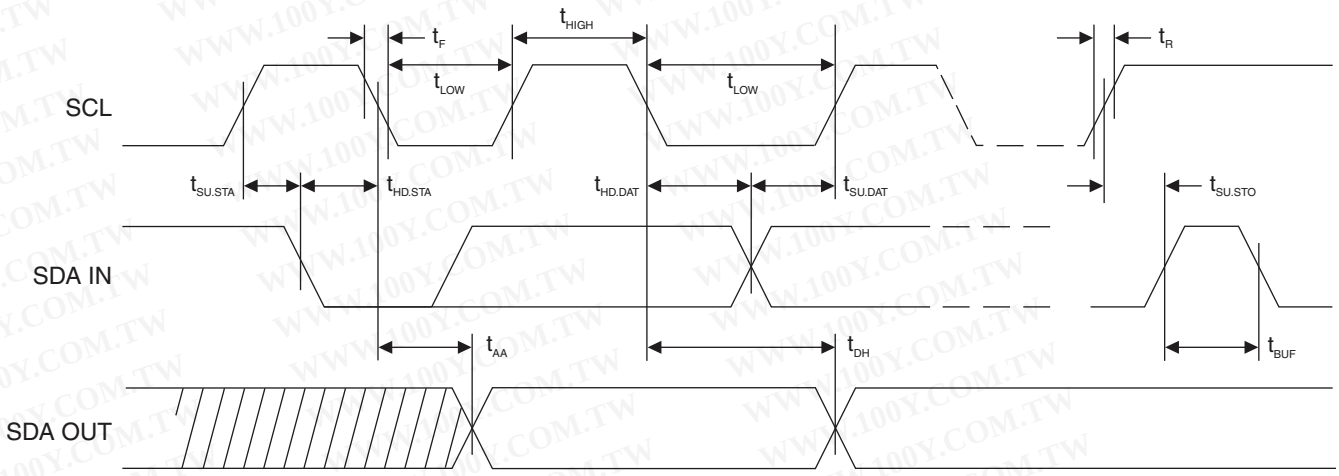
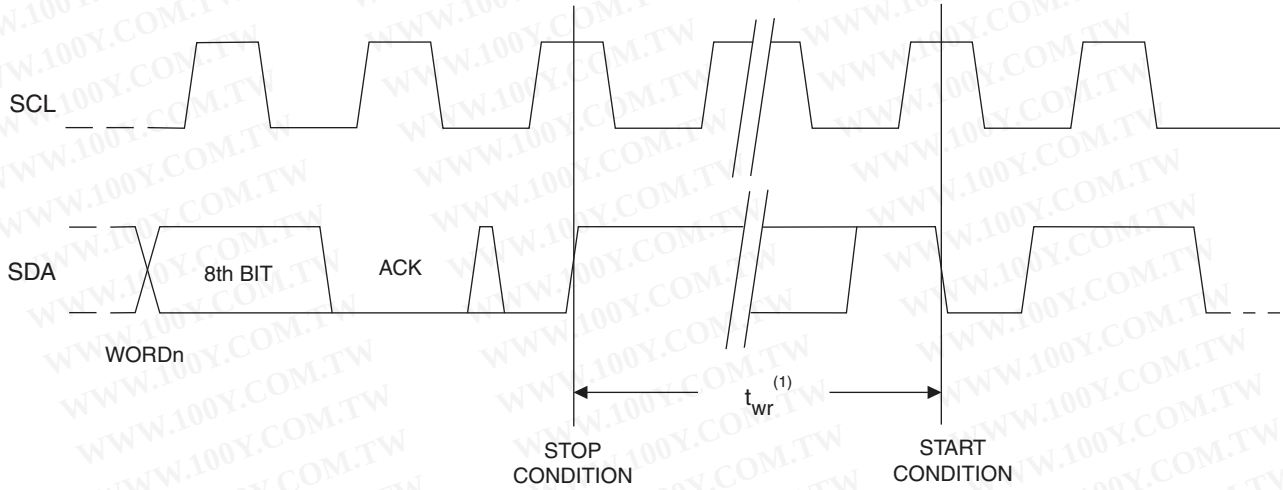


Figure 4-3. Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O



Notes: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

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Figure 4-4. Data Validity

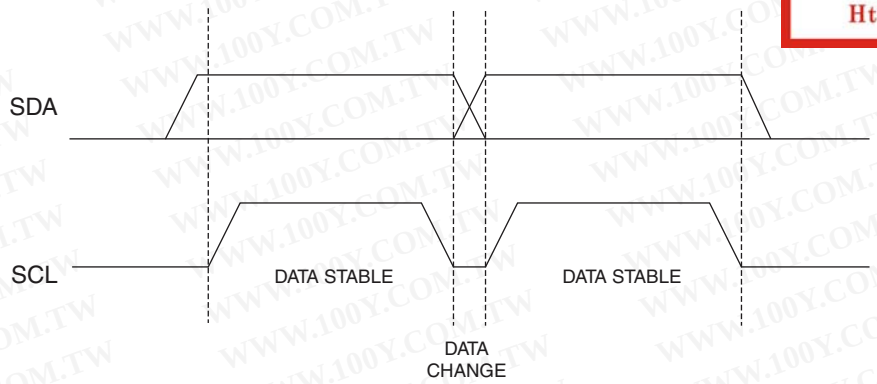


Figure 4-5. Start and Stop Definition

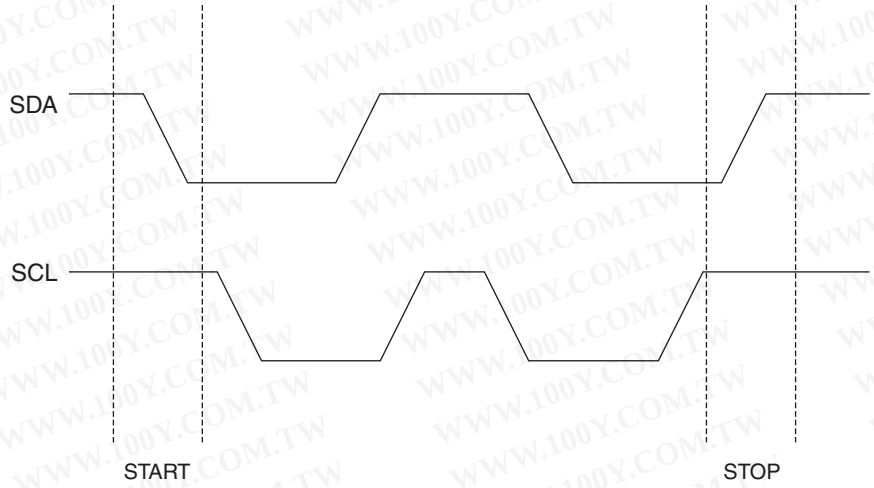
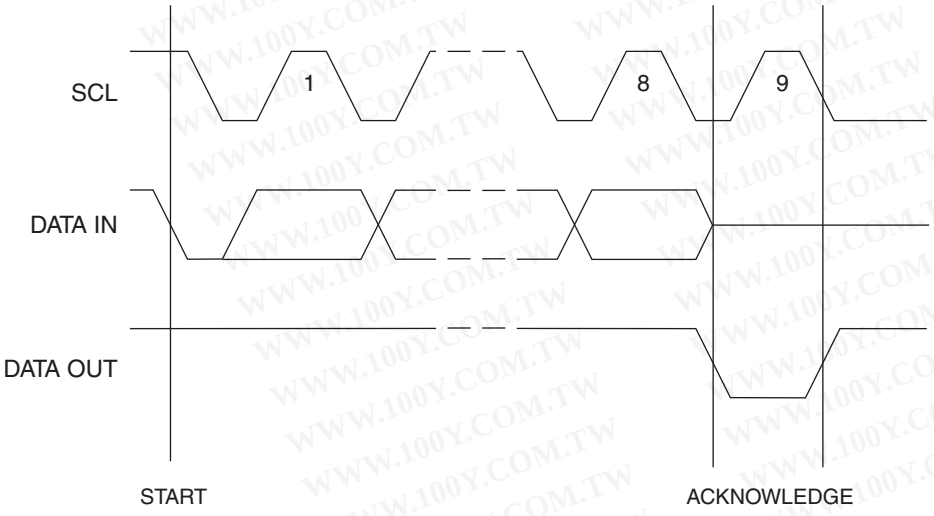


Figure 4-6. Output Acknowledge



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5. Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 7-1 on page 10). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

DATA SECURITY: The Atmel® AT24C32D/64D has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

6. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 7-2 on page 10).

PAGE WRITE: The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 7-3 on page 11).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

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7. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 7-4 on page 11).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 7-5 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 7-6 on page 11).

Figure 7-1. Device Address

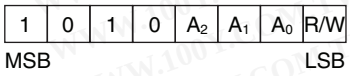
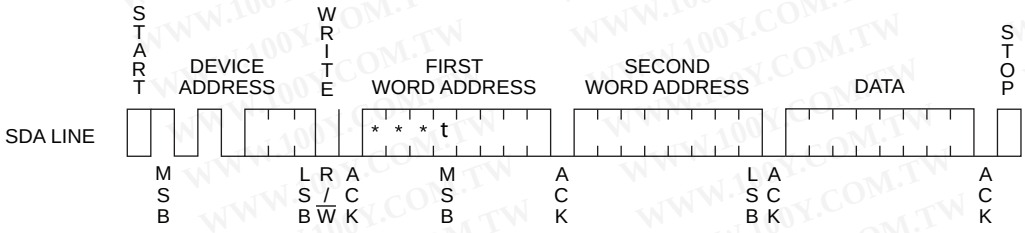


Figure 7-2. Byte Write



Notes: 1. * = DON'T CARE bits
2. t = DON'T Care bit for Atmel AT24C32D

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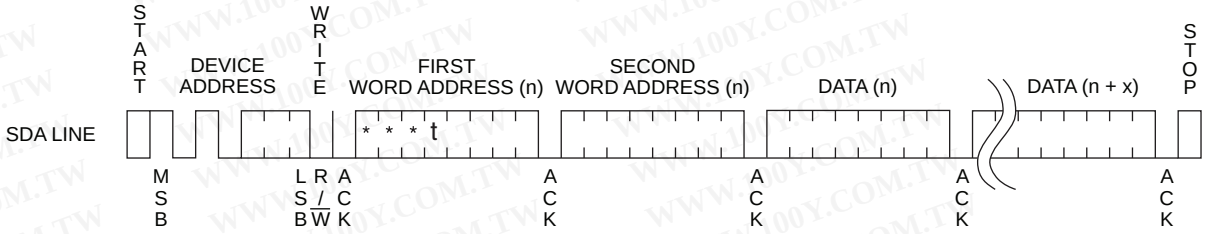
Figure 7-3. Page Write



Notes: 1. * = DON'T CARE bits
2. t = DON'T CARE bit for Atmel AT24C32D

Figure 7-4. Current Address Read

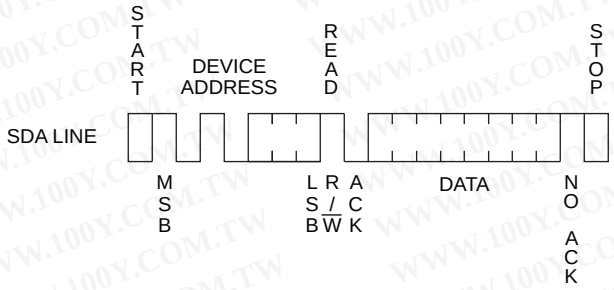
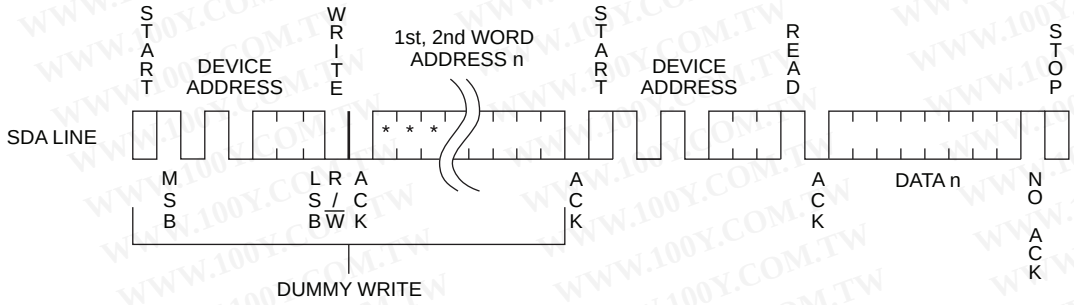
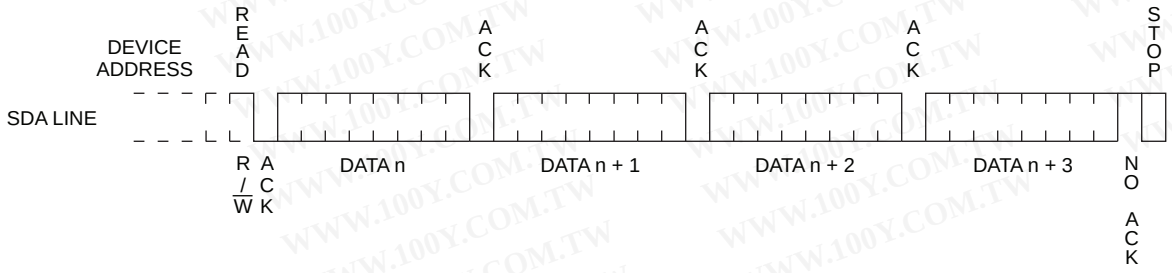


Figure 7-5. Random Read



Notes: 1. * = DON'T CARE bits

Figure 7-6. Sequential Read



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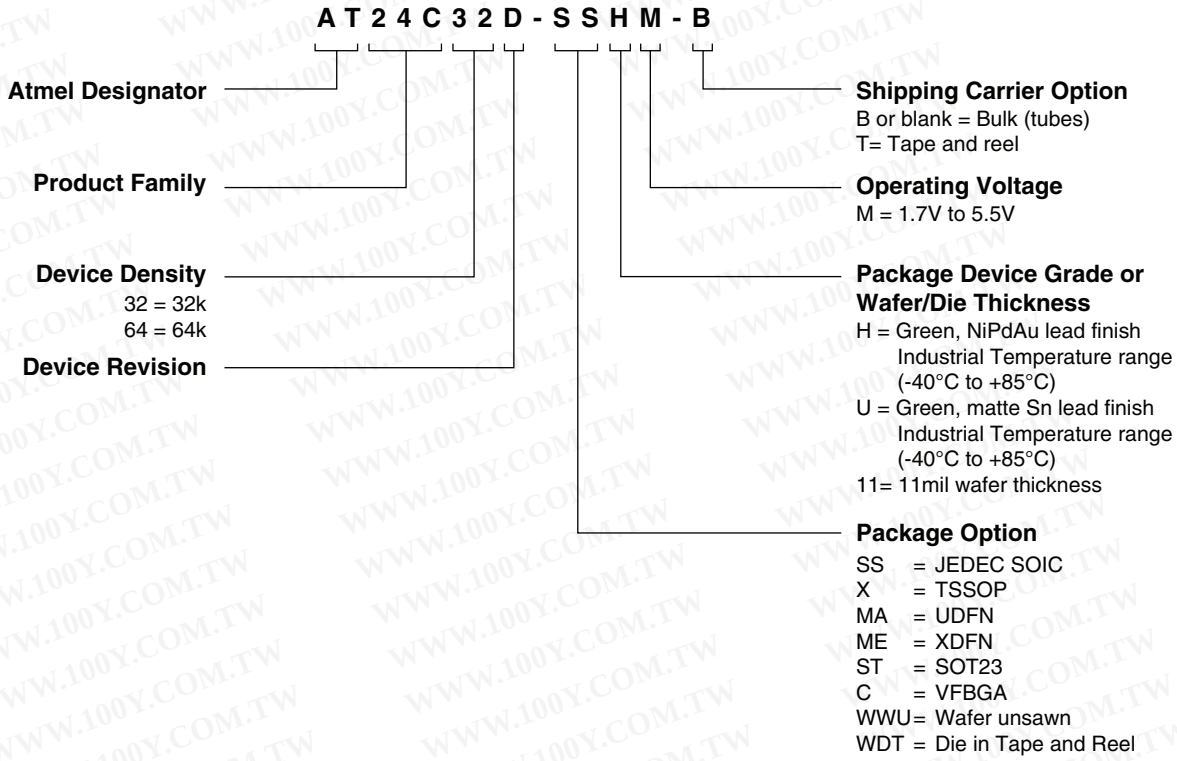
8. Ordering Code Detail



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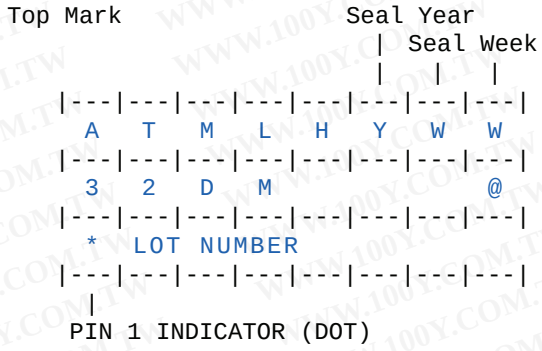
9. Part Markings

9.1 Atmel AT24C32D

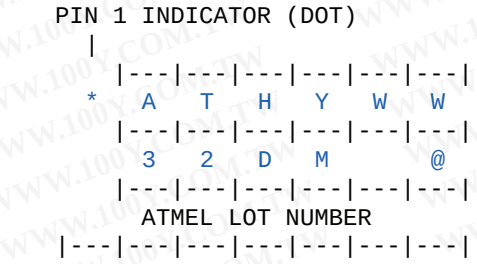
Atmel AT24C32D-SSHM




```
Y = SEAL YEAR          WW = SEAL WEEK
8: 2008      2: 2012   02 = Week 2
9: 2009      3: 2013   04 = Week 4
0: 2010      4: 2014   :: : :::: :
1: 2011      5: 2015   :: : :::: ::
                       50 = Week 50
                       52 = Week 52
@ = Country of Assembly

BOTTOM MARK
              No Bottom Mark
```

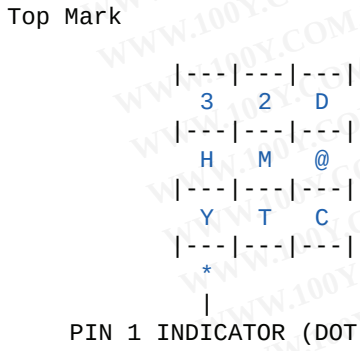
Atmel AT24C32D-XHM




```
Y = SEAL YEAR          WW = SEAL WEEK
8: 2008      2: 2012   02 = Week 2
9: 2009      3: 2013   04 = Week 4
0: 2010      4: 2014   :: : :::: :
1: 2011      5: 2015   :: : :::: ::
                       50 = Week 50
                       52 = Week 52
@ = Country of Assembly

No Bottom Mark
```

Atmel AT24C32D-MAHM




```
Y = YEAR OF ASSEMBLY
TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND
    WITH TRACE CODE LOG BOOK)
Y = SEAL YEAR
8: 2008      2: 2012
9: 2009      3: 2013
0: 2010      4: 2014
1: 2011      5: 2015
```

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Atmel AT24C32D-MEHM

Top Mark

```
          |---|---|---|
            3   2   D
          |---|---|---|
            Y   T   C
          |---|---|---|
            *
            |
PIN 1 INDICATOR (DOT)
```

```
Y = YEAR OF ASSEMBLY
TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND
    WITH TRACE CODE LOG BOOK)
Y = SEAL YEAR
8: 2008      2: 2012
9: 2009      3: 2013
0: 2010      4: 2014
1: 2011      5: 2015
```

Atmel AT24C32D-STUM

Top Mark

```
                |---|---|---|---|---|
Line 1 -------->  B   D   M   W   U
                |---|---|---|---|---|
                  *
                  |
                 PIN 1 INDICATOR (DOT)
```

```
BD= Device Code
M = Operating Voltage
W = Write Protect Feature
U = Material Set
```

Bottom Mark

```
|---|---|---|---|
  Y   M   T   C
|---|---|---|---|
```

```
Y = One Digit Year Code
M = Seal Month
TC= Trace Code
```

Atmel AT24C32D-CUM

Top Mark

```
                |---|---|---|---|
Line 1 ------->   3   2   D   U
                |---|---|---|---|
                  Y   M   T   C
                   |<--PIN 1 THIS CORNER
```

```
Y = One Digit Year Code
8: 2008      1: 2011
9: 2009      2: 2012
0: 2010      3: 2013

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
A = JANUARY
B = FEBRUARY
" " "         "
J = OCTOBER
K = NOVEMBER
L = DECEMBER

TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND
    WITH TRACE CODE LOG BOOK)
    (e.g. XX = AA, AB... YZ, ZZ)
```

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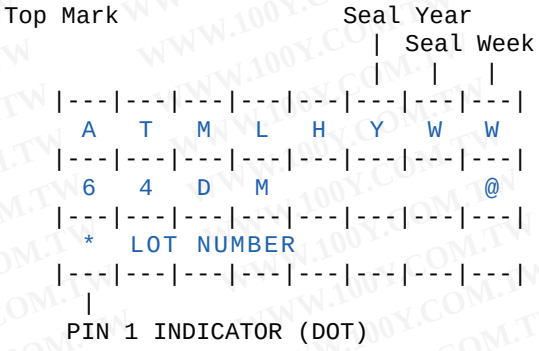
9.2 Atmel AT24C64D

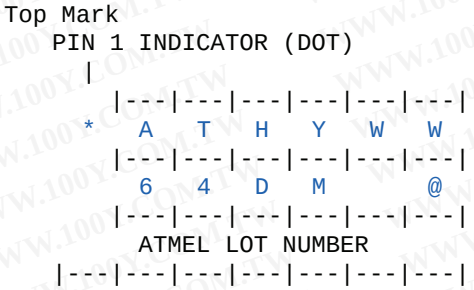
Atmel AT24C64D-SSHM




```
Y = SEAL YEAR          WW = SEAL WEEK
8: 2008      2: 2012   02 = Week 2
9: 2009      3: 2013   04 = Week 4
0: 2010      4: 2014   :: : :::: :
1: 2011      5: 2015   :: : :::: ::
                       50 = Week 50
                       52 = Week 52
@ = Country of Assembly

BOTTOM MARK
              No Bottom Mark
```

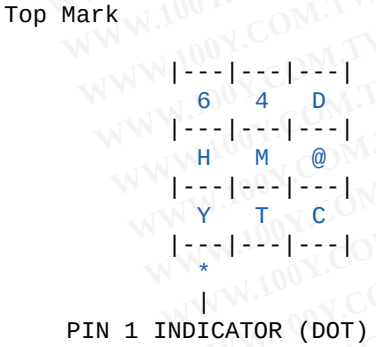
Atmel AT24C64D-XHM




```
Y = SEAL YEAR          WW = SEAL WEEK
8: 2008      2: 2012   02 = Week 2
9: 2009      3: 2013   04 = Week 4
0: 2010      4: 2014   :: : :::: :
1: 2011      5: 2015   :: : :::: ::
                       50 = Week 50
                       52 = Week 52
@ = Country of Assembly

No Bottom Mark
```

Atmel AT24C64D-MAHM




```
Y = YEAR OF ASSEMBLY
TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND
    WITH TRACE CODE LOG BOOK)
Y = SEAL YEAR
8: 2008      2: 2012
9: 2009      3: 2013
0: 2010      4: 2014
1: 2011      5: 2015
```

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Atmel AT24C64D-MEHM

Top Mark

```
|---|---|---|
  6   4   D
|---|---|---|
  Y   T   C
|---|---|---|
  *
  |
PIN 1 INDICATOR (DOT)
```

Y = YEAR OF ASSEMBLY
TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND WITH TRACE CODE LOG BOOK)
Y = SEAL YEAR

8: 2008	2: 2012
9: 2009	3: 2013
0: 2010	4: 2014
1: 2011	5: 2015

Atmel AT24C64D-CUM

Top Mark

```
                |---|---|---|---|
Line 1 ------->   6   4   D   U
                |---|---|---|---|
                  Y   M   T   C
                  |<--PIN 1 THIS CORNER
```

Y = One Digit Year Code

8: 2008	1: 2011
9: 2009	2: 2012
0: 2010	3: 2013

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
A = JANUARY
B = FEBRUARY
" " """""""""
J = OCTOBER
K = NOVEMBER
L = DECEMBER

TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND WITH TRACE CODE LOG BOOK)
(e.g. XX = AA, AB... YZ, ZZ)

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10. Ordering Codes

Atmel AT24C32D Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C32D-SSHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	Lead-free/Halogen-free Industrial Temperature (-40°C to +85°C)
AT24C32D-SSHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	
AT24C32D-XHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C32D-XHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C32D-MAHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8Y6	
AT24C32D-MEHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8ME1	
AT24C32D-STUM-T[2]	1.7 to 5.5	5TS1	
AT24C32D-CUM-T[2]	1.7 to 5.5	8U3-1	
AT24C32D-WWU11M[3]	1.7 to 5.5	Die Sale	Industrial Temperature (-40°C to +85°C)

Notes: 1. "-B" denotes bulk delivery
2. "-T" denotes tape and reel delivery. SOIC = 4K/reel. TSSOP, UDFN, XDFN, SOT23 and VFBGA = 5K/reel
3. For Wafer sales, please contact Atmel Sales

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Dual no Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body, (XDFN)
5TS1	5-lead, 1.60mm Body, Plastic Thin Shrink Small Outline Package (SOT-23)
8U3-1	8-ball, 1.50mm x 2.00mm Body, 0.50mm Pitch, Small Die Ball Grid Array (VFBGA)

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Atmel AT24C64D Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C64D-SSHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	Lead-free/Halogen-free Industrial Temperature (-40°C to +85°C)
AT24C64D-SSHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8S1	
AT24C64D-XHM-B[1] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C64D-XHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C64D-MAHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8Y6	
AT24C64D-MEHM-T[2] (NiPdAu Lead Finish)	1.7 to 5.5	8ME1	
AT24C64D-CUM-T[2]	1.7 to 5.5	8U3-1	
AT24C64D-WWU11M[3]	1.7 to 5.5	Die Sale	Industrial Temperature (-40°C to +85°C)

Notes: 1. "-B" denotes bulk delivery
2. "-T" denotes tape and reel delivery. SOIC = 4K/reel. TSSOP, UDFN, XDFN, SOT23 and VFBGA = 5K/reel
3. For Wafer sales, please contact Atmel Sales

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Dual no Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body, (XDFN)
8U3-1	8-ball, 1.50mm x 2.00mm Body, 0.50mm Pitch, Small Die Ball Grid Array (VFBGA)

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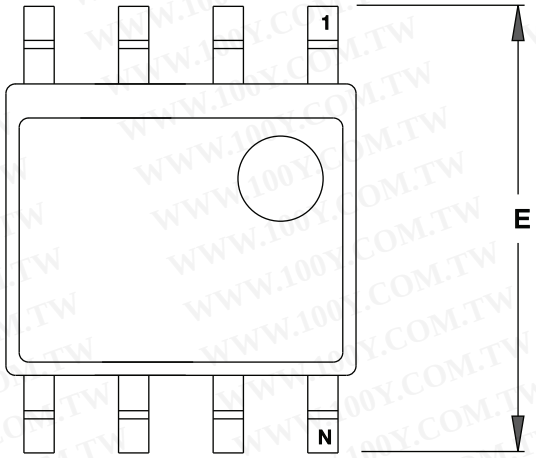
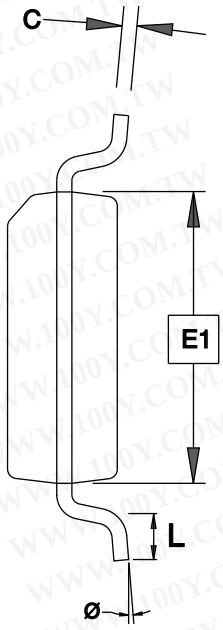
11. Packaging Information

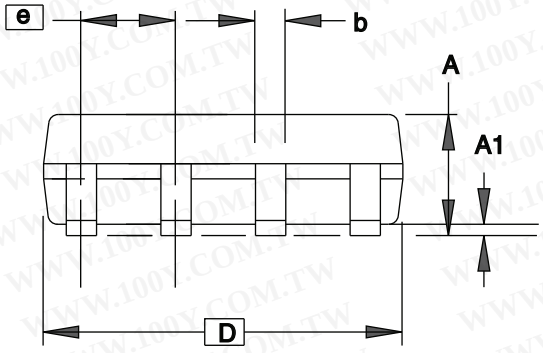
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

5/19/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	F

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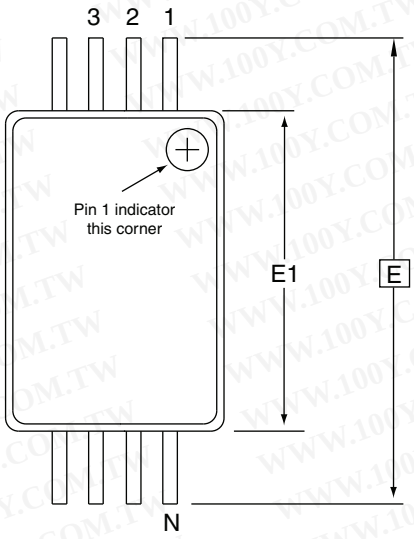
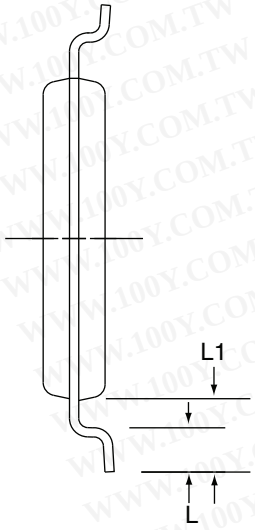
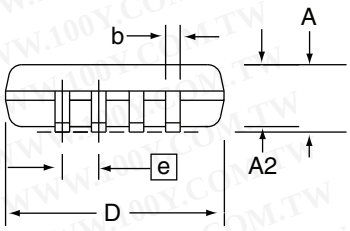
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/19/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8A2, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8A2	E

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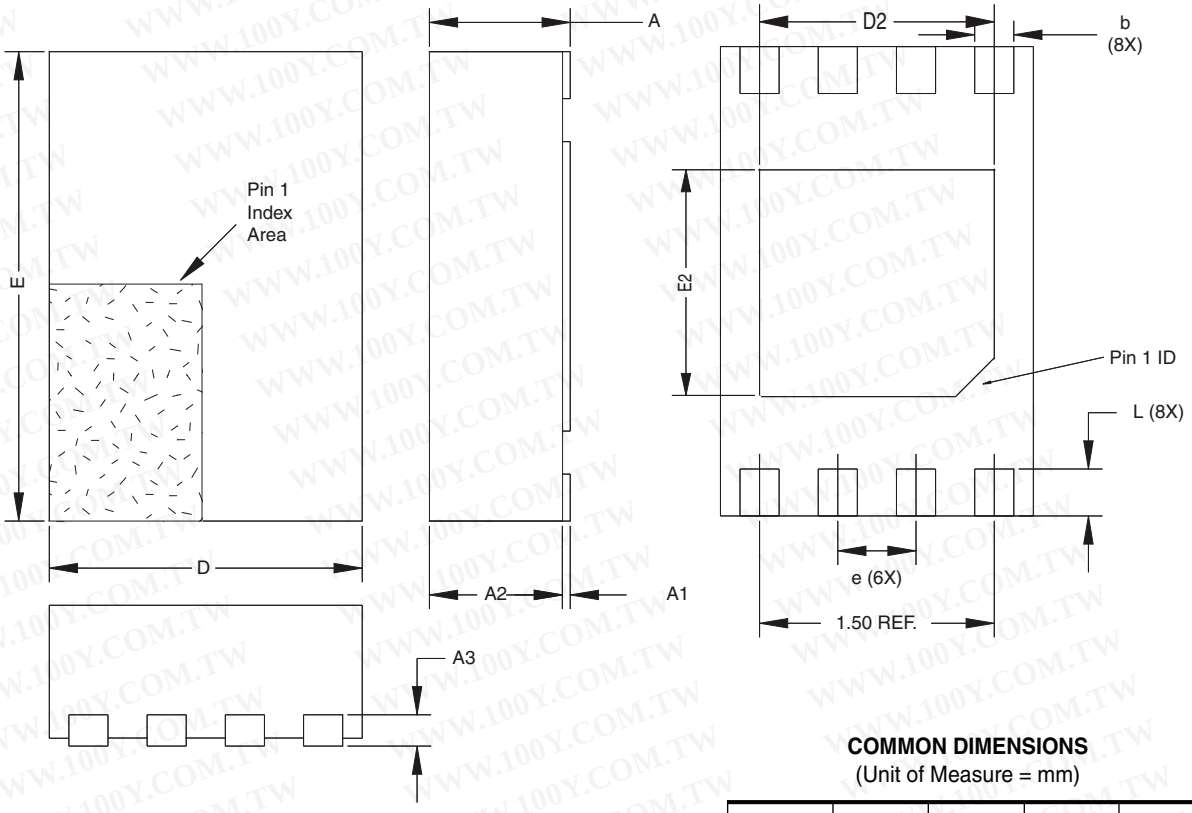
8Y6 – MLP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	–	–	1.40	
A	–	–	0.60	
A1	0.00	0.02	0.05	
A2	–	–	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

11/21/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8Y6, 8-lead, 2.0x3.0mm Body, 0.50mm Pitch, UltraThin Mini-MAP, Dual No Lead Package (Sawn)(UDFN)	YNZ	8Y6	E

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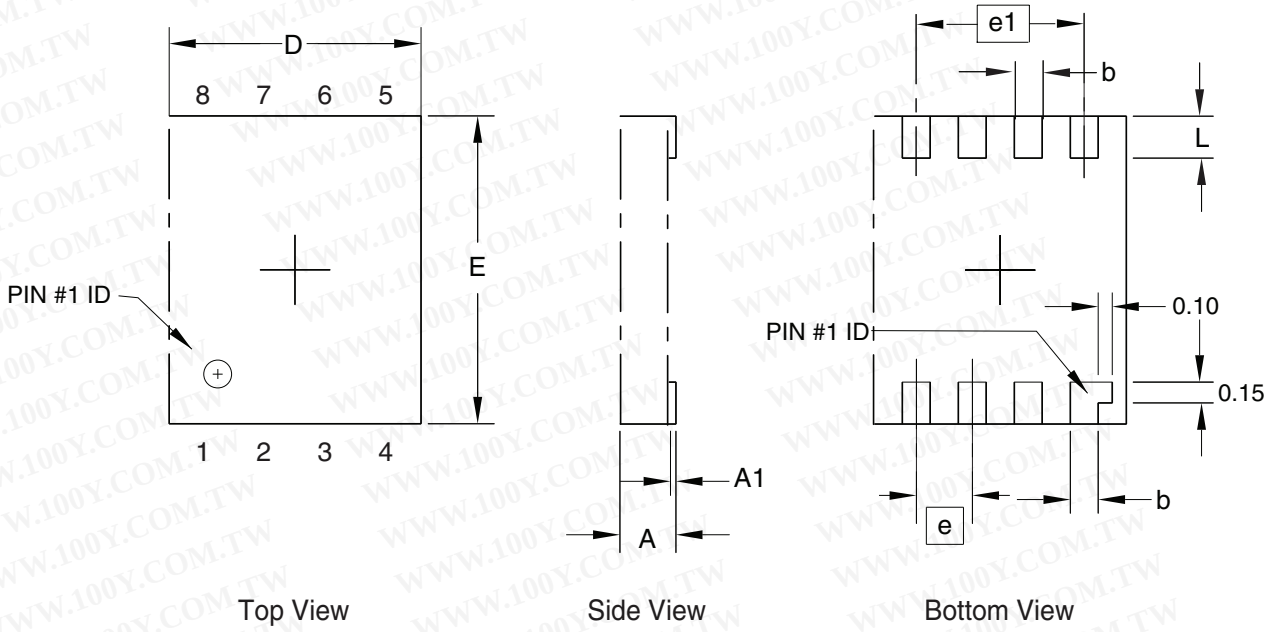
8ME1 – XDFN



Top View Side View Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e	0.40 TYP			
e1	1.20 REF			
L	0.26	0.30	0.35	

8/3/09

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8ME1, 8-lead (1.80 x 2.20mm Body) Extra Thin DFN (XDFN)	DTP	8ME1	A

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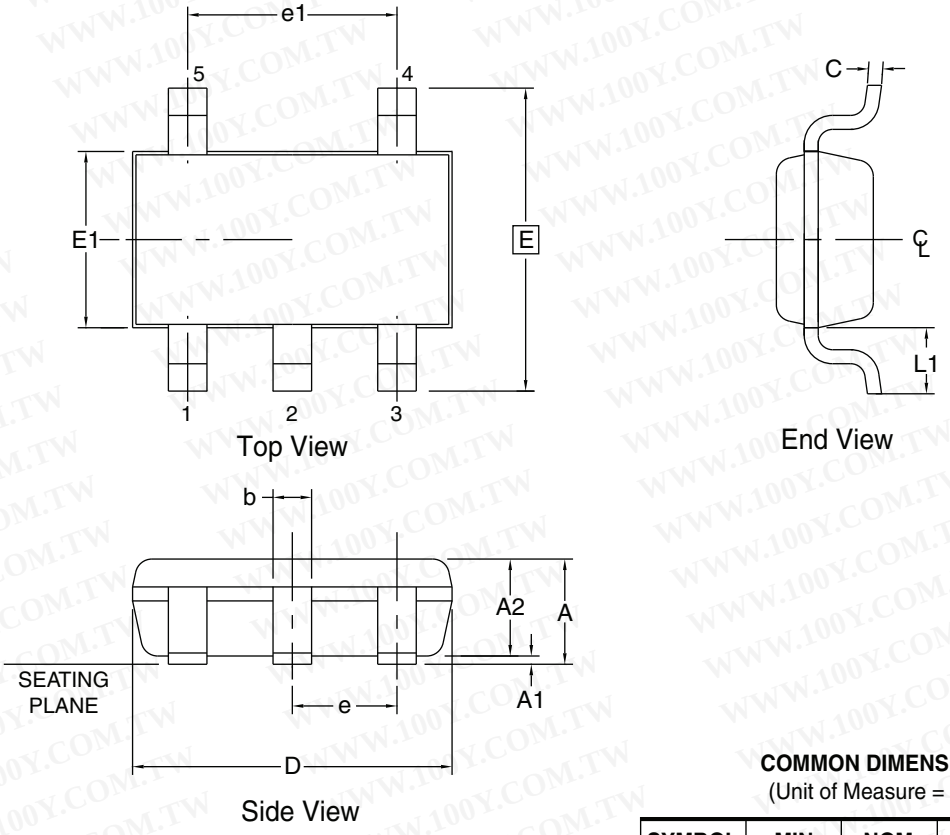
5TS1– SOT-23



Notes:
1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.15mm per end. Dimensions E1 does not include interlead flash or protrusion. Interlead flasg or protrusion shall not exceed 0.15mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are deteremined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.80mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07mm.
5. This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.10	
A1	0.00	–	0.10	
A2	0.70	0.90	1.00	
c	0.08	–	0.20	3
D		2.90 BSC		1, 2
E		2.80 BSC		1, 2
E1		1.60 BSC		1, 2
L1		0.60 REF		
e		0.95 BSC		
e1		1.90 BSC		
b	0.30	–	0.50	3, 4

11/05/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**5TS1**, 5-lead, 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	TSZ	5TS1	B

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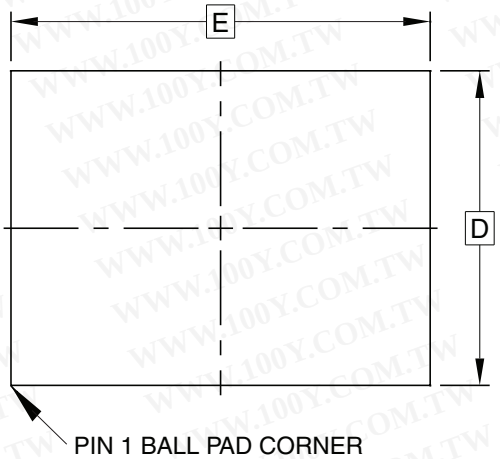
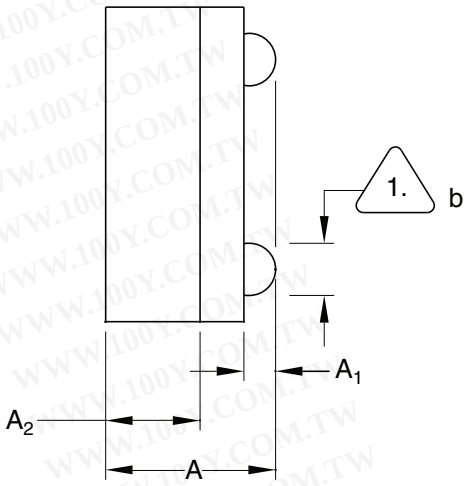
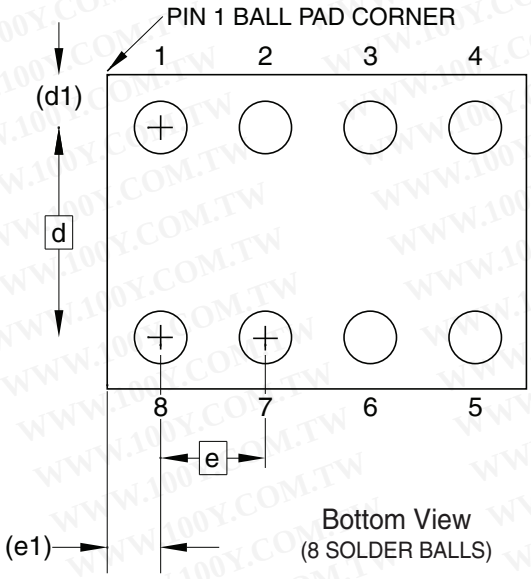
8U3-1 – VFBGA



Top View



End View



Bottom View
(8 SOLDER BALLS)

Notes:
1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.00 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

9/19/07

Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	8U3-1, 8-ball, 1.50 x 2.00mm Body, 0.50mm pitch, VFBGA Package (dBGA2)	PO8U3-1	C

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Revision History

Doc. Rev.	Date	Comments
5298B	6/2010	Update 8A2 and 8S1 package drawings Remove all PDIP device package references Add SOT23 in feature and description list, pin configuration with note and package drawing
5298A	4/2010	Initial document release