# EN39LV010
# 1 Megabit (128K x 8-bit ) 4 Kbyte Uniform Sector, CMOS 3.0 Volt-only Flash Memory

## FEATURES

- Single power supply operation
  - Full voltage range: 2.7-3.6 volt read and write operations for battery-powered applications.
  - Regulated voltage range: 3.0-3.6 volt read and write operations for high performance 3.3 volt microprocessors.
- High performance
  - Full voltage range: access times as fast as 70 ns
  - Regulated voltage range: access times as fast as 45ns
- Low power consumption (typical values at 5 MHz)
  - 7 mA typical active read current
  - 15 mA typical program/erase current
  - 1 µA typical standby current (standard access time to active mode)
- Flexible Sector Architecture:
  - Thirty-two 4 Kbyte sectors
- Sector protection:
  Hardware locking of sectors to prevent program or erase operations within individual sectors
- High performance program/erase speed
  - Byte program time: 8µs typical
  - Sector erase time: 90ms typical
- JEDEC Standard program and erase commands
- JEDEC standard $\overline{\text{DATA}}$ polling and toggle bits feature
- Single Sector and Chip Erase
- Embedded Erase and Program Algorithms
- Erase Suspend / Resume modes:
  Read or program another Sector during Erase Suspend Mode
- triple-metal double-poly triple-well CMOS Flash Technology
- Low Vcc write inhibit ≤ 2.5V
- Minimum 100K program/erase endurance cycles
- Package options
  - 4mm x 6mm 34-ball WFBGA
  - 8mm x 14mm 32-pin TSOP (Type 1)
  - 32-pin PLCC
- Industrial Temperature Range

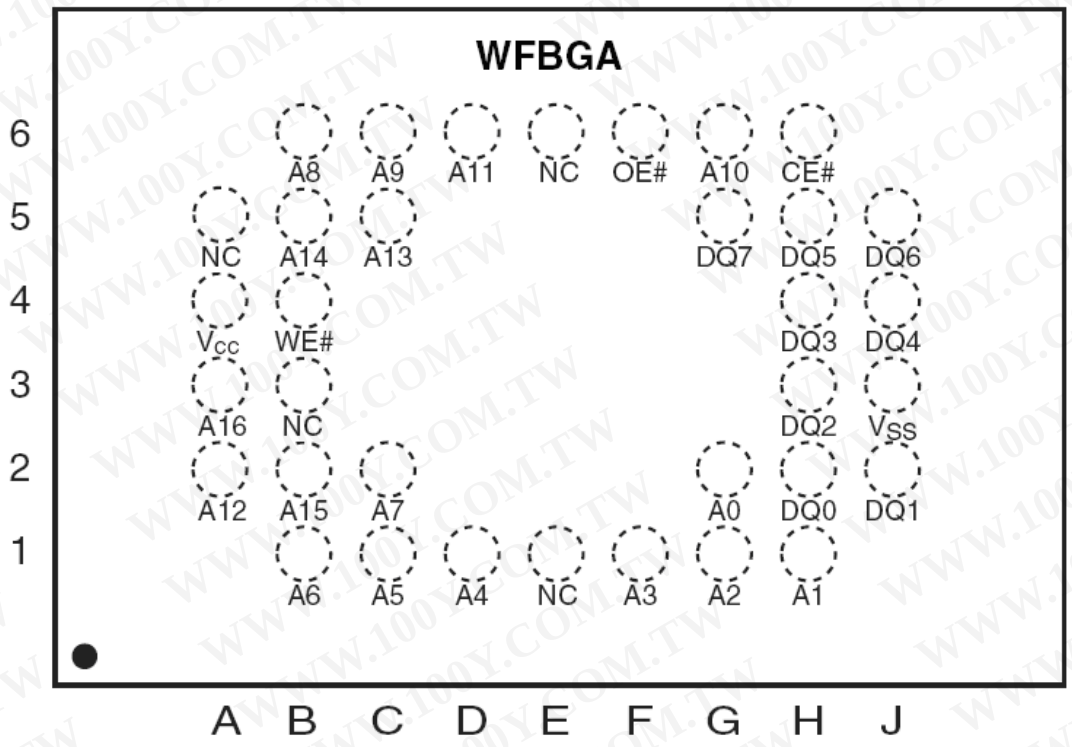
## GENERAL DESCRIPTION

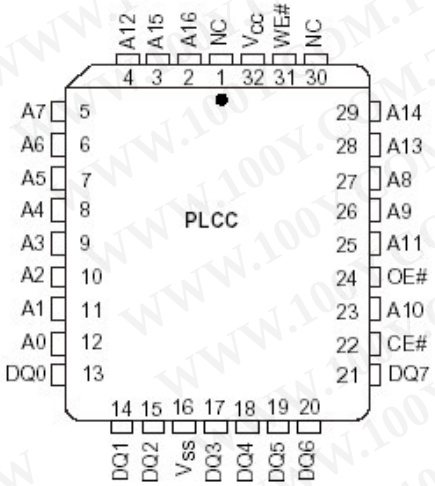
The EN39LV010 is a 1-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 131,072 bytes. Any byte can be programmed typically in 8µs.The EN39LV010 features 3.0V voltage read and write operation, with access times as fast as 45ns to eliminate the need for WAIT states in high-performance microprocessor systems.

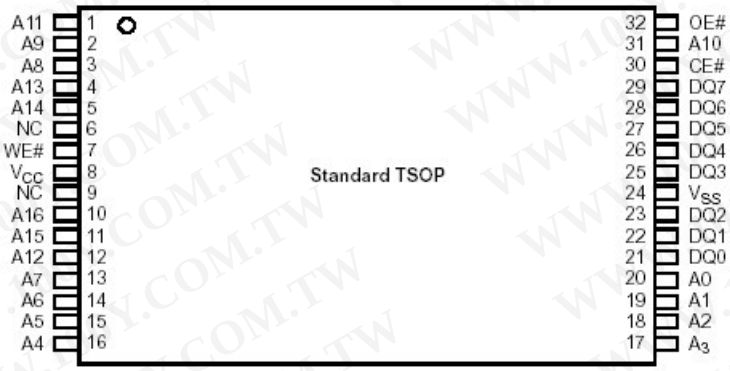
The EN39LV010 has separate Output Enable ($\overline{\text{OE}}$), Chip Enable ($\overline{\text{CE}}$), and Write Enable ($\overline{\text{WE}}$) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

## CONNECTION DIAGRAMS

TOP VIEW (balls facing down)



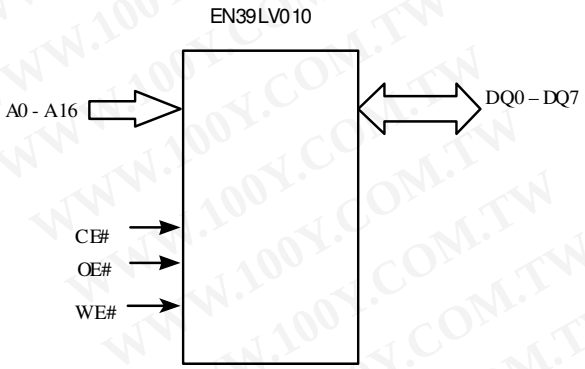



## TABLE 1. PIN DESCRIPTION

| Pin Name | Function |
|---|---|
| A0-A16 | Addresses |
| DQ0-DQ7 | 8 Data Inputs/Outputs |
| WE# | Write Enable |
| CE# | Chip Enable |
| OE# | Output Enable |
| Vcc | Supply Voltage |
| Vss | Ground |

## FIGURE 1. LOGIC DIAGRAM



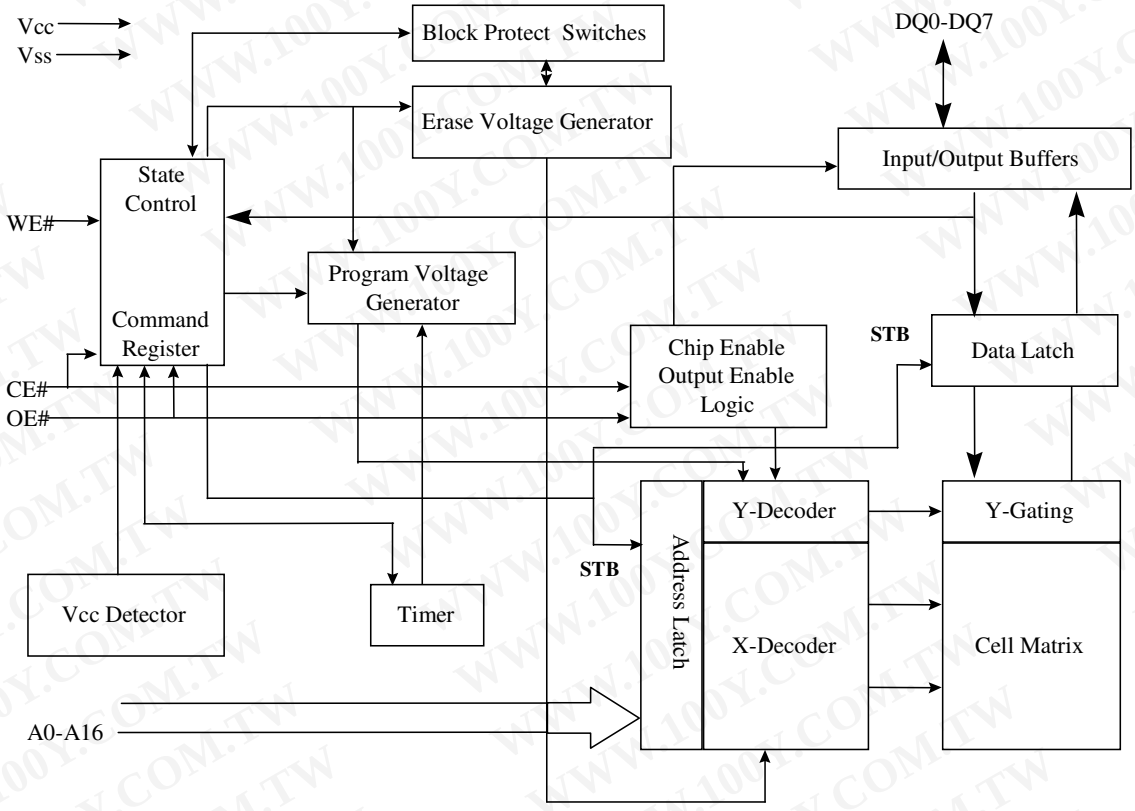

## TABLE 2. UNIFORM SECTOR ARCHITECTURE

| Sector | Address range | | SIZE (Kbytes) |
|---|---|---|---|
| 31 | 01F000h | 01FFFFh | 4 |
| 30 | 01E000h | 01EFFFh | 4 |
| 29 | 01D000h | 01DFFFh | 4 |
| 28 | 01C000h | 01CFFFh | 4 |
| 27 | 01B000h | 01BFFFh | 4 |
| 26 | 01A000h | 01AFFFh | 4 |
| 25 | 019000h | 019FFFh | 4 |
| 24 | 018000h | 018FFFh | 4 |
| 23 | 017000h | 017FFFh | 4 |
| 22 | 016000h | 016FFFh | 4 |
| 21 | 015000h | 015FFFh | 4 |
| 20 | 014000h | 014FFFh | 4 |
| 19 | 013000h | 013FFFh | 4 |
| 18 | 012000h | 012FFFh | 4 |
| 17 | 011000h | 011FFFh | 4 |
| 16 | 010000h | 010FFFh | 4 |
| 15 | 00F000h | 00FFFFh | 4 |
| 14 | 00E000h | 00EFFFh | 4 |
| 13 | 00D000h | 00DFFFh | 4 |
| 12 | 00C000h | 00CFFFh | 4 |
| 11 | 00B000h | 00BFFFh | 4 |
| 10 | 00A000h | 00AFFFh | 4 |
| 9 | 009000h | 009FFFh | 4 |
| 8 | 008000h | 008FFFh | 4 |
| 7 | 007000h | 007FFFh | 4 |
| 6 | 006000h | 006FFFh | 4 |
| 5 | 005000h | 005FFFh | 4 |
| 4 | 004000h | 004FFFh | 4 |
| 3 | 003000h | 003FFFh | 4 |
| 2 | 002000h | 002FFFh | 4 |
| 1 | 001000h | 001FFFh | 4 |
| 0 | 000000h | 000FFFh | 4 |

## PRODUCT SELECTOR GUIDE

| Product Number | | EN39LV010 | |
|---|---|---|---|
| Speed Option | Regulated Voltage Range: Vcc=3.0-3.6 V | **-45R** | |
| | Full Voltage Range: Vcc=2.7 – 3.6 V | | **-70** |
| Max Access Time, ns ($t_{acc}$) | | 45 | 70 |
| Max CE# Access, ns ($t_{ce}$) | | 45 | 70 |
| Max OE# Access, ns ($t_{oe}$) | | 25 | 30 |

## BLOCK DIAGRAM



## TABLE 3. OPERATING MODES

### 1M FLASH USER MODE TABLE

| Operation | CE# | OE# | WE# | A0-A16 | DQ0-DQ7 |
|---|---|---|---|---|---|
| Read | L | L | H | $A_{IN}$ | $D_{OUT}$ |
| Write | L | H | L | $A_{IN}$ | $D_{IN}$ |
| CMOS Standby | $V_{cc}$ ± 0.3V | X | X | X | High-Z |
| Output Disable | L | H | H | X | High-Z |
| Sector Protect[2] | L | H | L | Sector address, A6=L, A1=H, A0=L | $D_{IN}$ , $D_{OUT}$ |
| Sector Unprotect[2] | L | H | L | Sector address, A6=H, A1=H, A0=L | $D_{IN}$ , $D_{OUT}$ |

Notes:
1. L=logic low= $V_{IL}$, H=Logic High= $V_{IH}$, $V_{ID}$ =11 ± 0.5V, X=Don't Care (either L or H, but not floating!), $D_{IN}$=Data In, $D_{OUT}$=Data Out, $A_{IN}$=Address In
2. Sector protection/unprotection can be implemented by programming equipment.

## TABLE 4. DEVICE IDENTIFICTION (Autoselect Codes)

### 1M FLASH MANUFACTURER/DEVICE ID TABLE

| Description | CE# | OE# | WE# | A16 to A14 | A13 to A10 | A9[2] | A8 | A7 | A6 | A5 to A2 | A1 | A0 | DQ7 to DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer ID: Eon | L | L | H | X | X | $V_{ID}$ | H[1] | X | L | X | L | L | 1Ch |
| | | | | | | | L | | | | | | 7Fh |
| Device ID | L | L | H | X | X | $V_{ID}$ | X | X | L | X | L | H | D5h |
| Sector Protection Verification | L | L | H | SA | X | $V_{ID}$ | X | X | L | X | H | L | 01h (Protected) |
| | | | | | | | | | | | | | 00h (Unprotected) |

**Note:**
1. A8=H is recommended for manufacture ID check. If a manufacture ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = VID is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

# USER MODE DEFINITIONS

## Standby Mode

The EN39LV010 has a CMOS-compatible standby mode, which reduces the current to < 1µA (typical). It is placed in CMOS-compatible standby when the $\overline{CE}$ pin is at $V_{CC} \pm 0.3$. When in standby modes, the outputs are in a high-impedance state independent of the $\overline{OE}$ input.

## Read Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" additional details.

## Output Disable Mode

When the $\overline{CE}$ or $\overline{OE}$ pin is at a logic high level ($V_{IH}$), the output from the EN39LV010 is disabled. The output pins are placed in a high impedance state.

## Auto Select Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires $V_{ID}$ (11 V) on address pin A9. Address pins A8, A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require $V_{ID}$. See "Command Definitions" for details on using the autoselect mode.

## Write Mode

Write operations, including programming data and erasing sectors of memory, require the host system to write a command or command sequence to the device. Write cycles are initiated by placing the byte or word address on the device's address inputs while the data to be written is input on DQ[7:0]. The host system must drive the CE# and WE# pins Low and the OE# pin High for a valid write operation to take place. All addresses are latched on the falling edge of WE# and CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. The system is not required to provide further controls or timings. The device automatically provides internally generated program / erase pulses and verifies the programmed /erased cells'

margin. The host system can detect completion of a program or erase operation by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits.

The 'Command Definitions' section of this document provides details on the specific device commands implemented in the EN39LV010.

## Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection is intended only for programming equipment. This method requires $V_{ID}$ be applied to both OE# and A9 pin and non-standard microprocessor timings are used. This method is described in a separate document called EN39LV010 Supplement, which can be obtained by contacting a representative of Eon Silicon Solution, Inc.

## Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{acc}$ + 30ns. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output is latched and always available to the system. $ICC_4$ in the DC Characteristics table represents the automatic sleep more current specification.

## Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

### Low $V_{CC}$ Write Inhibit

When Vcc is less than $V_{LKO}$, the device does not accept any write cycles. This protects data during Vcc power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than $V_{LKO}$. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than $V_{LKO}$.

### Write Pulse "Glitch" protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

### Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH, or $\overline{WE}$ = VIH. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one. If $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ are all logical zero (not recommended usage), it will be considered a read.

### Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with $\overline{CE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IL}$ and $\overline{OE}$ = $V_{IH}$, the device will not accept commands on the rising edge of $\overline{WE}$.

# COMMAND DEFINITIONS

The operations of the EN39LV010 are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Sector Protection, Program, Sector Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 5). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

## Table 5. EN39LV010 Command Definitions

| Command Sequence | | Cycles | Bus Cycles | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1st Cycle | | 2nd Cycle | | 3rd Cycle | | 4th Cycle | | 5th Cycle | | 6th Cycle | |
| | | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Read | | 1 | RA | RD | | | | | | | | | | |
| Reset | | 1 | Xxx | F0 | | | | | | | | | | |
| Autoselect | Manufacturer ID | 4 | 555 | AA | 2AA | 55 | 555 | 90 | 000 | 7F | | | | |
| | | | | | | | | | 100 | 1C | | | | |
| | Device ID | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X01 | D5 | | | | |
| | Sector Protect Verify | 4 | 555 | AA | 2AA | 55 | 555 | 90 | (SA) X02 | 00/ 01 | | | | |
| Program | | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Chip Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| Sector Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| Erase Suspend | | 1 | xxx | B0 | | | | | | | | | | |
| Erase Resume | | 1 | xxx | 30 | | | | | | | | | | |

Address and Data values indicated in hex
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care
PD = Program Data: data to be programmed at location PA
SA = Sector Address: address of the Sector to be erased or verified. Address bits A16-A12 uniquely select any Sector.

## Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following an Erase Suspend command, Erase Suspend mode is entered. The system can read array data using the standard read timings, with the only difference in that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception.
The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See next section for details on Reset.

## Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires $V_{ID}$ on address bit A9 and is intended for PROM programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 4 any number of times, without needing another command sequence.

The system must write the reset command to exit the autoselect mode and return to reading array data.

## Programming Command

Programming the EN39LV010 is performed by using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever is last; data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first.

Programming status may be checked by sampling data on DQ7 ($\overline{DATA}$ polling) or on DQ6 (toggle bit). ). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a 0 to a 1. Only an erase operation can change a data from 0 to 1. When programming time limit is exceeded, DQ5 will produce a logical “1” and a Reset command can return the device to Read mode.

## Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Flowchart 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

## Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to "Write Operation Status" for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

### Erase Suspend / Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don't-cares when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information. The Autoselect command is not supported during Erase Suspend Mode.

The system must write the Erase Resume command (address bits are don't-care) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

## WRITE OPERATION STATUS

### DQ7: $\overline{\text{DATA}}$ Polling

The EN39LV010 provides $\overline{\text{DATA}}$ Polling on DQ7 to indicate to the host system the status of the embedded operations. The $\overline{\text{DATA}}$ Polling feature is active during the embedded Programming, Sector Erase, Chip Erase, Erase Suspend. (See Table 6)

When the embedded Programming is in progress, an attempt to read the device will produce the complement of the data last written to DQ7. Upon the completion of the embedded Programming, an attempt to read the device will produce the true data last written to DQ7. For the embedded Programming, $\overline{\text{DATA}}$ polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a "0" at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the "1" at the DQ7 output during the read. For Chip Erase, the $\overline{\text{DATA}}$ polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the six-cycle sequence. For Sector Erase, $\overline{\text{DATA}}$ polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse.

$\overline{DATA}$ Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, $\overline{DATA}$ polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable ($\overline{OE}$) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for $\overline{DATA}$ Polling (DQ7) is shown on Flowchart 5. The $\overline{DATA}$ Polling (DQ7) timing diagram is shown in Figure 8.

## DQ6: Toggle Bit I

The EN39LV010 provides a "Toggle Bit" on DQ6 to indicate to the host system the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by toggling $\overline{OE}$ or $\overline{CE}$) will result in DQ6 toggling between "zero" and "one". Once the embedded Program or Erase operation is complete, DQ6 will stop toggling and valid data will be read on the next successive attempts. During Byte Programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four-cycle sequence. For Chip Erase, the Toggle Bit is valid after the rising edge of the sixth-cycle sequence. For Sector Erase, the Toggle Bit is valid after the last rising edge of the Sector Erase $\overline{WE}$ pulse.

In Byte Programming, if the sector being written to is protected, DQ6 will toggles for about 2 µs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected blocks are protected, DQ6 will toggle for about 100 µs. The chip will then return to the read mode without changing data in all protected blocks.

Toggling either $\overline{CE}$ or $\overline{OE}$ will cause DQ6 to toggle.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

## DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a "1" on DQ5.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1." Under both these conditions, the system must issue the reset command to return the device to reading array data.

## DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be used to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip

erase command.) When sector erase starts, DQ3 switches from “0” to “1.” This device does not support multiple sector erase command sequences so it is not very meaningful since it immediately shows as a “1” after the first 30h command. Future devices may support this feature.

## DQ2: Erase Toggle Bit II

The “Toggle Bit” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 5 to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

## Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Flowchart 6).

## Write Operation Status

| Operation | | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 |
|---|---|---|---|---|---|---|
| Standard Mode | Embedded Program Algorithm | DQ7# | Toggle | 0 | N/A | No toggle |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle |
| Erase Suspend Mode | Reading within Erase Suspended Sector | 1 | No Toggle | 0 | N/A | Toggle |
| | Reading within Non-Erase Suspended Sector | Data | Data | Data | Data | Data |
| | Erase-Suspend Program | DQ7# | Toggle | 0 | N/A | N/A |

## Table 6. Status Register Bits

| DQ | Name | Logic Level | Definition |
|---|---|---|---|
| 7 | $\overline{\text{DATA}}$ POLLING | '1' | Erase Complete or erase Sector in Erase suspend |
| | | '0' | Erase On-Going |
| | | DQ7 | Program Complete or data of non-erase Sector during Erase Suspend |
| | | $\overline{\text{DQ7}}$ | Program On-Going |
| 6 | TOGGLE BIT | '-1-0-1-0-1-0-1-' | Erase or Program On-going |
| | | DQ6 | Read during Erase Suspend |
| | | '-1-1-1-1-1-1-1-' | Erase Complete |
| 5 | TIME OUT BIT | '1' | Program or Erase Error |
| | | '0' | Program or Erase On-going |
| 3 | ERASE TIME BIT | '1' | Erase operation start |
| | | '0' | Erase timeout period on-going |
| 2 | TOGGLE BIT | '-1-0-1-0-1-0-1-' | Chip Erase, Sector Erase or Read within Erase-Suspended sector. (When DQ5=1, Erase Error due to currently addressed Sector or Program on Erase-Suspended sector) |
| | | DQ2 | Read on addresses of non Erase-Suspend sectors |

**Notes:**

DQ7 $\overline{\text{DATA}}$ Polling: indicates the P/E status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6: Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

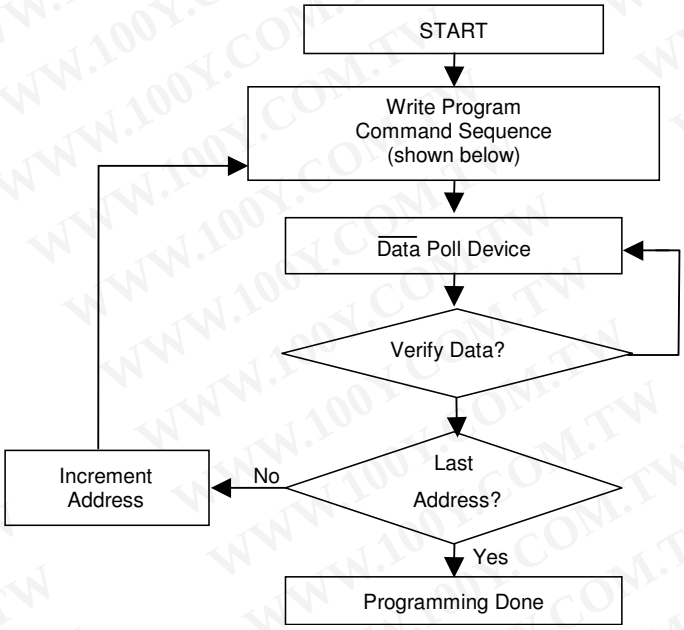
DQ5: Time Out Bit: set to "1" if failure in programming or erase

DQ3: Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

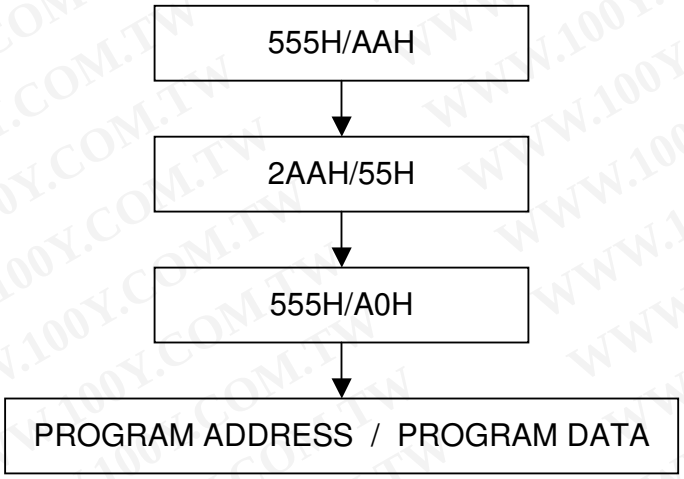
DQ2: Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

# EMBEDDED ALGORITHMS

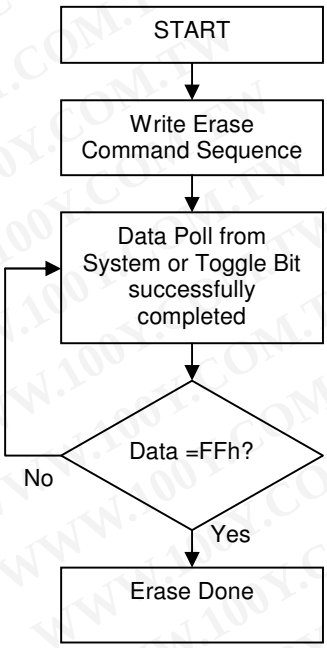
## Flowchart 1. Embedded Program



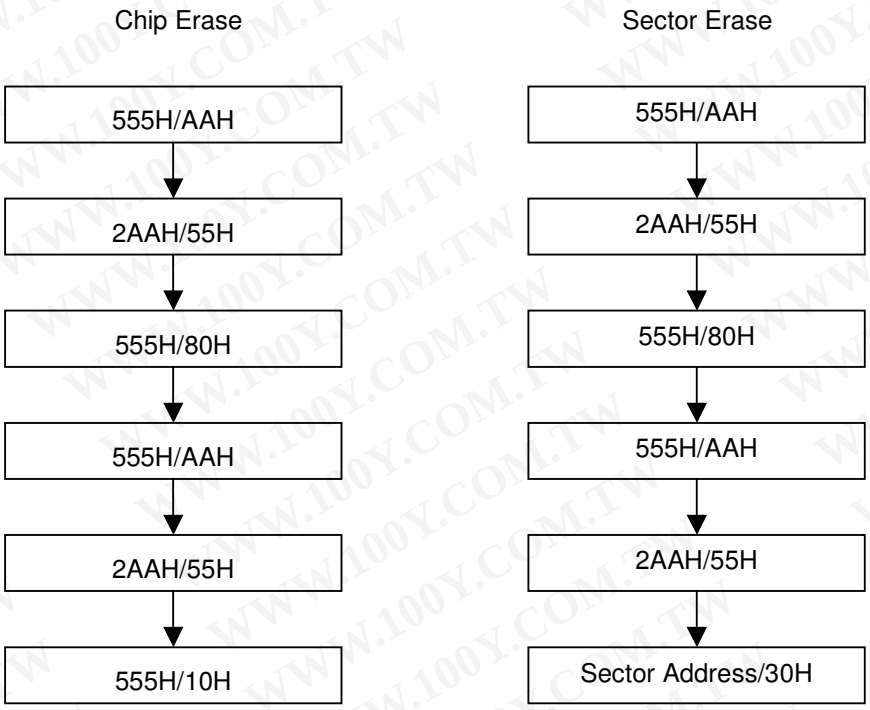

## Flowchart 2. Embedded Program Command Sequence



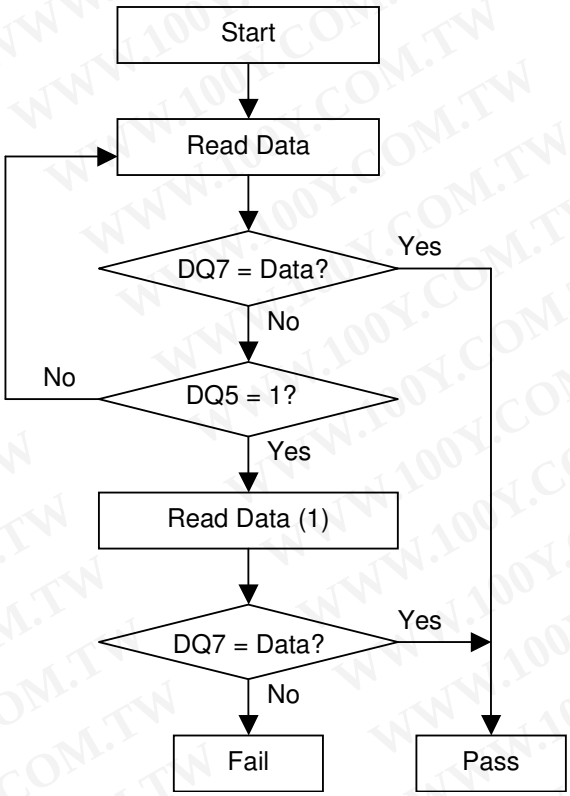
## Flowchart 3. Embedded Erase



## Flowchart 4. Embedded Erase Command Sequence

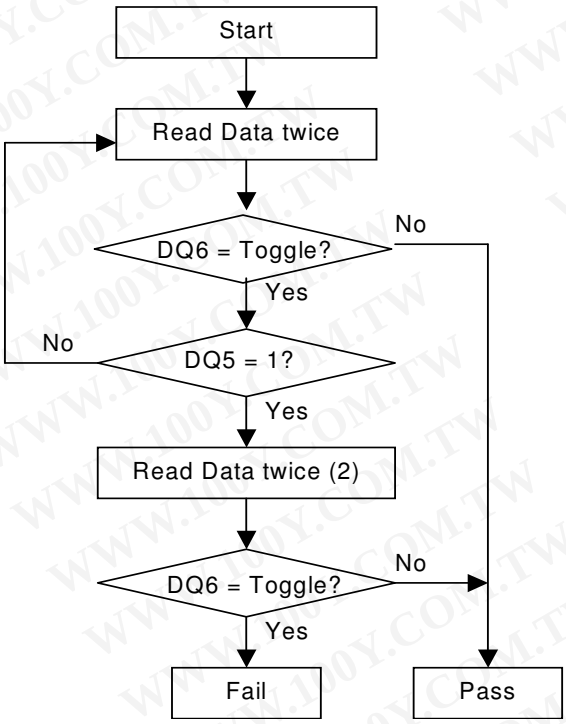


## Flowchart 5. $\overline{\text{DATA}}$ Polling Algorithm




Notes:
(1) This second read is necessary in case the first read was done at the exact instant when the status data was in transition.

## Flowchart 6. Toggle Bit Algorithm




Notes:
(2) This second set of reads is necessary in case the first set of reads was done at the exact instant when the status data was in transition.

## Table 7. DC Characteristics

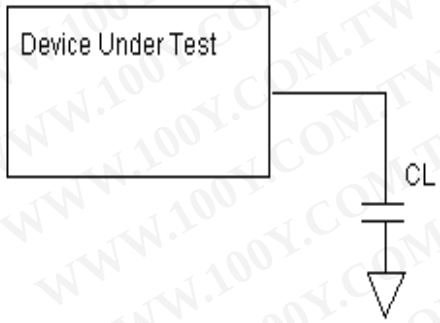
($T_a$ = - 40°C to 85°C; $V_{CC}$ = 2.7-3.6V)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | 0V≤ $V_{IN}$ ≤ Vcc | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | 0V≤ $V_{OUT}$ ≤ Vcc | | | ±1 | µA |
| $I_{CC1}$ | Supply Current (read)CMOS | CE# = $V_{IL}$; OE# = $V_{IH}$; f = 5MHz | | 7 | 12 | mA |
| $I_{CC2}$ | Supply Current (Standby - CMOS) | CE# = Vcc ± 0.3V | | 1 | 5.0 | µA |
| $I_{CC3}$ | Supply Current (Program or Erase) | Byte program, Sector or Chip Erase in progress | | 15 | 30 | mA |
| $I_{CC4}$ | Automatic Sleep Mode | $V_{IH}$ = Vcc ± 0.3 V<br>$V_{IL}$ = Vss ± 0.3 V | | 1 | 5.0 | µA |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 0.7 x Vcc | | Vcc ± 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4.0 mA | | | 0.45 | V |
| $V_{OH}$ | Output High Voltage CMOS | $I_{OH}$ = -100 µA, | Vcc - 0.4V | | | V |
| $V_{ID}$ | A9 Voltage (Electronic Signature) | | 10.5 | | 11.5 | V |
| $I_{ID}$ | A9 Current (Electronic Signature) | A9 = $V_{ID}$ | | | 100 | µA |
| $V_{LKO}$ | Supply voltage (Erase and Program lock-out) | | 2.3 | | 2.5 | V |

**Notes:**

1. BYTE# pin can also be GND ± 0.3V. BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.
2. Maximum $I_{CC}$ specifications are tested with Vcc = Vcc max.

## Test Conditions




## Test Specifications

| Test Conditions | -45R | -70 | Unit |
|---|---|---|---|
| Output Load Capacitance, $C_L$ | 30 | 100 | pF |
| Input Rise and Fall times | 5 | 5 | ns |
| Input Pulse Levels | 0.0-3.0 | 0.0-3.0 | V |
| Input timing measurement reference levels | 1.5 | 1.5 | V |
| Output timing measurement reference levels | 1.5 | 1.5 | V |

## Table 8. AC CHARACTERISTICS

### Read-only Operations Characteristics

| Parameter Symbols | | | Test Setup | | Speed Options | | |
|---|---|---|---|---|---|---|---|
| JEDEC | Standard | Description | | | -45R | -70 | Unit |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | Min | 45 | 70 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | $\overline{CE} = V_{IL}$<br>$\overline{OE} = V_{IL}$ | Max | 45 | 70 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable To Output Delay | $\overline{OE} = V_{IL}$ | Max | 45 | 70 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | Max | 25 | 30 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z | | Max | 10 | 20 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z | | Max | 10 | 20 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first | | Min | 0 | 0 | ns |

**Notes:**

For -45R, Vcc = 3.0V ~3.6V
Output Load : 30pF
Input Rise and Fall Times: 5ns
Input Rise Levels: 0.0 V to Vcc
Timing Measurement Reference Level, Input and Output: 1.5 V

For -70, Vcc = 2.7V~3.6V
Output Load: 100 pF
Input Rise and Fall Times: 5 ns
Input Pulse Levels: 0.0 V to Vcc
Timing Measurement Reference Level, Input and Output: 1.5 V

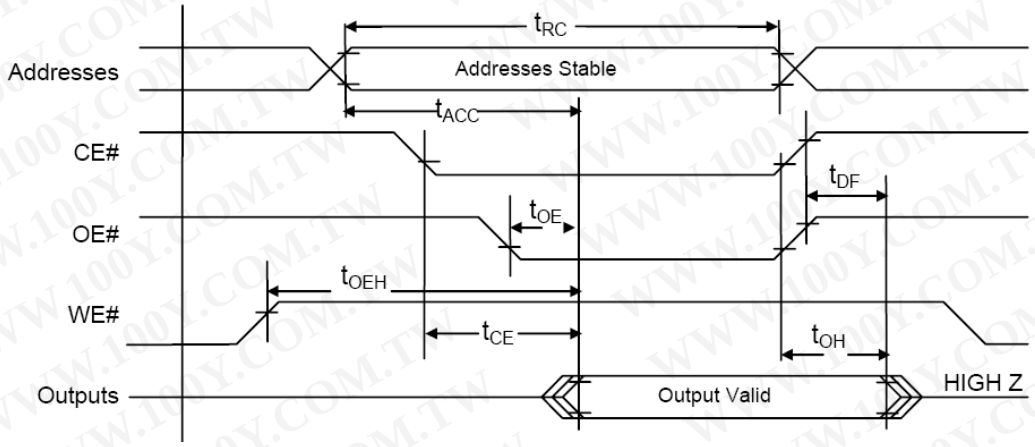



**Figure 5. AC Waveforms for READ Operations**

## Table 9. AC CHARACTERISTICS

### Write (Erase/Program) Operations

| Parameter Symbols | | | | | Speed Options | | |
|---|---|---|---|---|---|---|---|
| JEDEC | Standard | Description | | | -45R | -70 | Unit |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | Min | 45 | 70 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | 0 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min | 35 | 45 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min | 20 | 30 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | | Min | 0 | 0 | ns |
| | $t_{OEH}$ | Output Enable Hold Time | Read | MIn | 0 | 0 | ns |
| | | | Toggle and $\overline{DATA}$ Polling | Min | 10 | 10 | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time before Write ($\overline{OE}$ High to $\overline{WE}$ Low) | | Min | 0 | 0 | ns |
| $t_{ELWL}$ | $t_{CS}$ | $\overline{CE}$ SetupTime | | Min | 0 | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | $\overline{CE}$ Hold Time | | Min | 0 | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min | 25 | 35 | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | | Min | 20 | 20 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation | | Typ | 8 | 8 | µs |
| | | | | Max | 20 | 20 | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation | | Typ | 0.09 | 0.09 | s |
| | | | | Max | 0.5 | 0.5 | s |
| | $t_{VCS}$ | Vcc Setup Time | | Min | 50 | 50 | µs |
| | $t_{VIDR}$ | Rise Time to $V_{ID}$ | | Min | 500 | 500 | ns |

Notes: $t_{WC}$ is Not 100% tested.

## Table 10. AC CHARACTERISTICS
## Write (Erase/Program) Operations
**Alternate $\overline{CE}$ Controlled Writes**

| Parameter Symbols | | | | | Speed Options | | |
|---|---|---|---|---|---|---|---|
| JEDEC | Standard | Description | | | -45R | -70 | Unit |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | Min | 45 | 70 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min | 35 | 45 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | | Min | 20 | 30 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | | Min | 0 | 0 | ns |
| | $t_{OEH}$ | Output Enable Hold Time | Read | Min | 0 | 0 | ns |
| | | | Toggle and Data Polling | Min | 10 | 10 | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time before Write ($\overline{OE}$ High to $\overline{CE}$ Low) | | Min | 0 | 0 | ns |
| $t_{WLEL}$ | $t_{WS}$ | $\overline{WE}$ SetupTime | | Min | 0 | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | $\overline{WE}$ Hold Time | | Min | 0 | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | Write Pulse Width | | Min | 25 | 35 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | Write Pulse Width High | | Min | 20 | 20 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation | | Typ | 8 | 8 | µs |
| | | | | Max | 20 | 20 | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation | | Typ | 0.09 | 0.09 | s |
| | | | | Max | 0.5 | 0.5 | s |
| | $t_{VCS}$ | Vcc Setup Time | | Min | 50 | 50 | µs |
| | $t_{VIDR}$ | Rise Time to $V_{ID}$ | | Min | 500 | 500 | ns |

Notes: $t_{WC}$ is Not 100% tested.

## Table 11. ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Comments |
|---|---|---|---|---|
| | Typ | Max | Unit | |
| Sector Erase Time | 0.09 | 0.5 | sec | Excludes 00H programming prior to erasure |
| Chip Erase Time | 3 | 15 | sec | |
| Byte Programming Time | 8 | 20 | µs | Excludes system level overhead |
| Chip Programming Time | 0.8 | 2 | sec | |
| Erase/Program Endurance | 100K | | cycles | Minimum 100K cycles |

**Notes:**
1. Typical program and erase times assume the following conditions: room temperature, 3V and checkboard pattern programmed.
2. Maximum program and erase times assume the following conditions: worst case Vcc, 90°C and 100,000 cycles.

## Table 12. DATA RETENTION

| Parameter Description | Test Conditions | Min | Unit |
|---|---|---|---|
| Data Retention Time | 150℃ | 10 | Years |
| | 125℃ | 20 | Years |

## Table 13. TSOP PIN CAPACITANCE @ 25°C, 1.0MHz

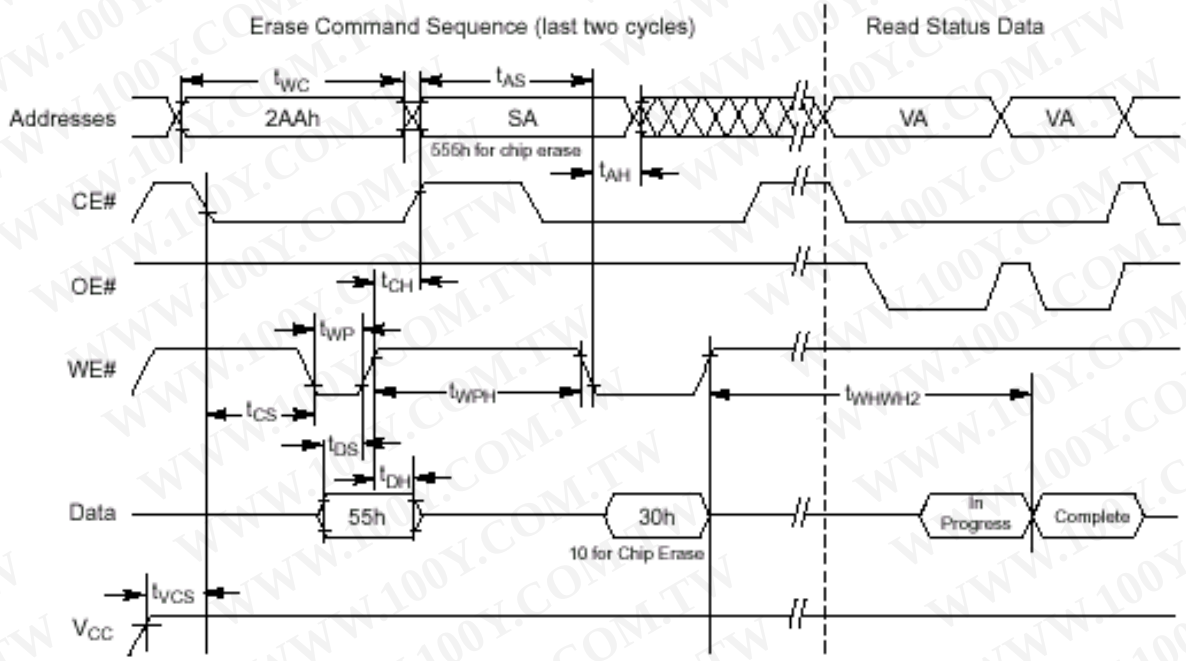
| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

## Table 14. 32-PIN PLCC PIN CAPACITANCE @ 25°C, 1.0MHz

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 8 | 12 | pF |

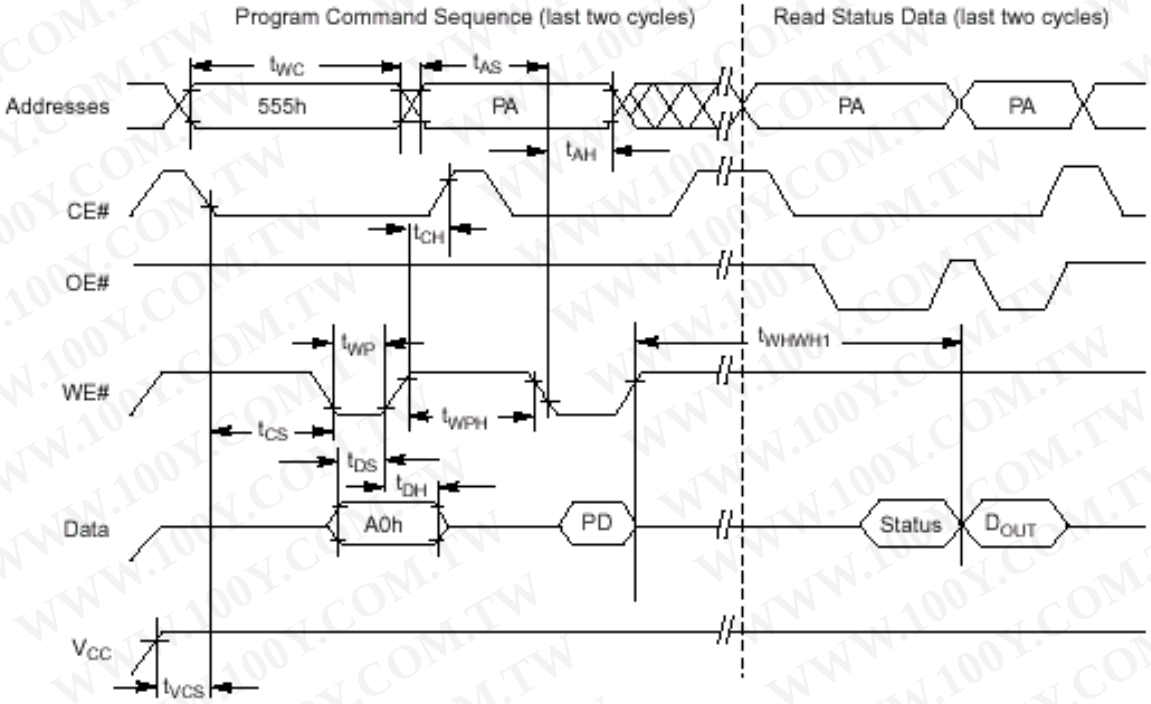
# AC CHARACTERISTICS

## Figure 6. AC Waveforms for Chip/Sector Erase Operations Timings



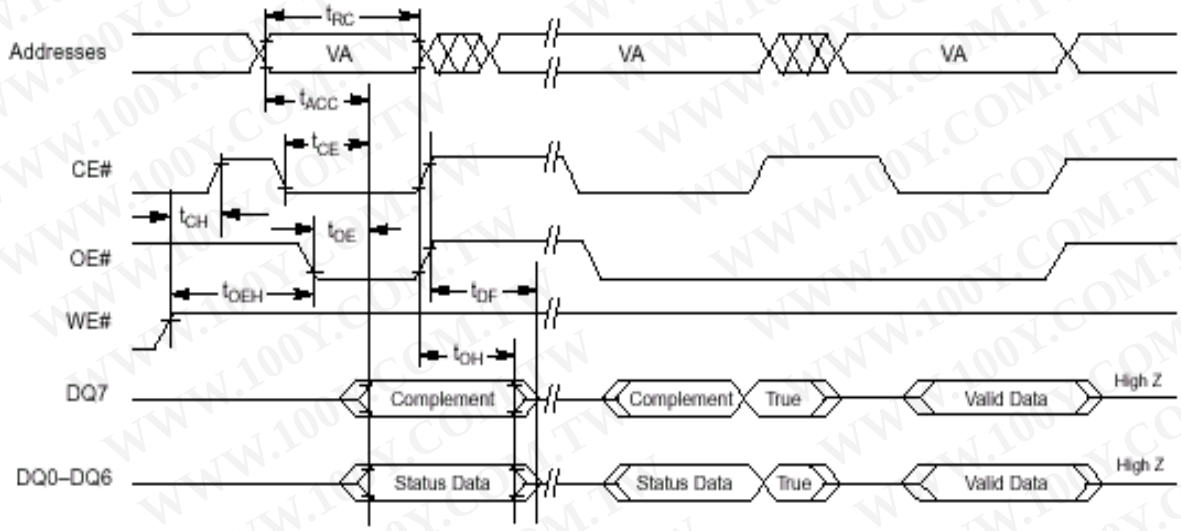

***Note:*** *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*

## Figure 7. Program Operation Timings



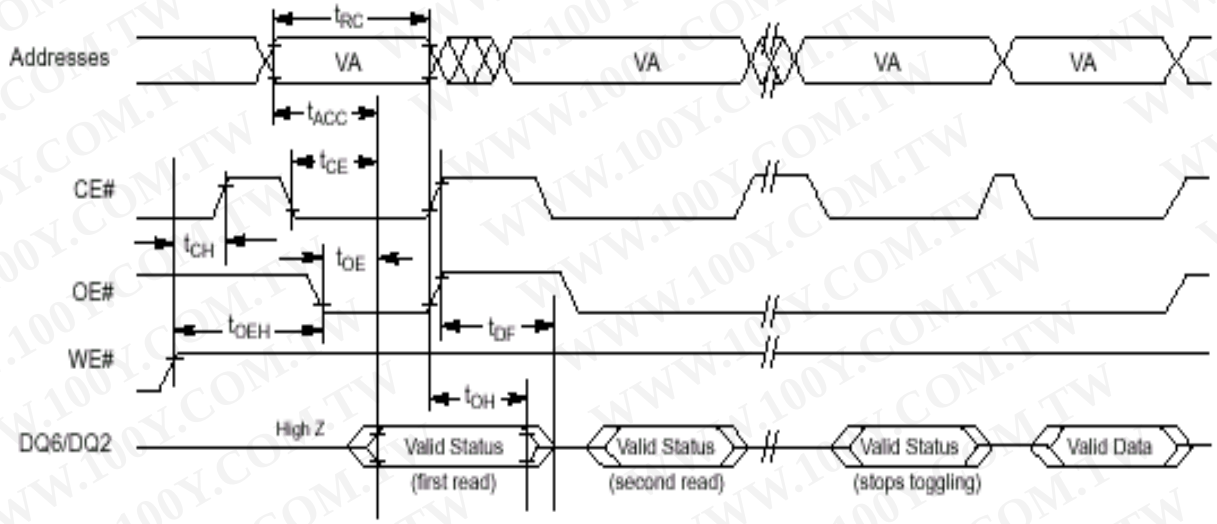

***Note:*** *PA = program address, PD = program data, $D_{OUT}$ is the true data at the program address.*

**Figure 8. AC Waveforms for /DATA Polling During Embedded Algorithm Operations**



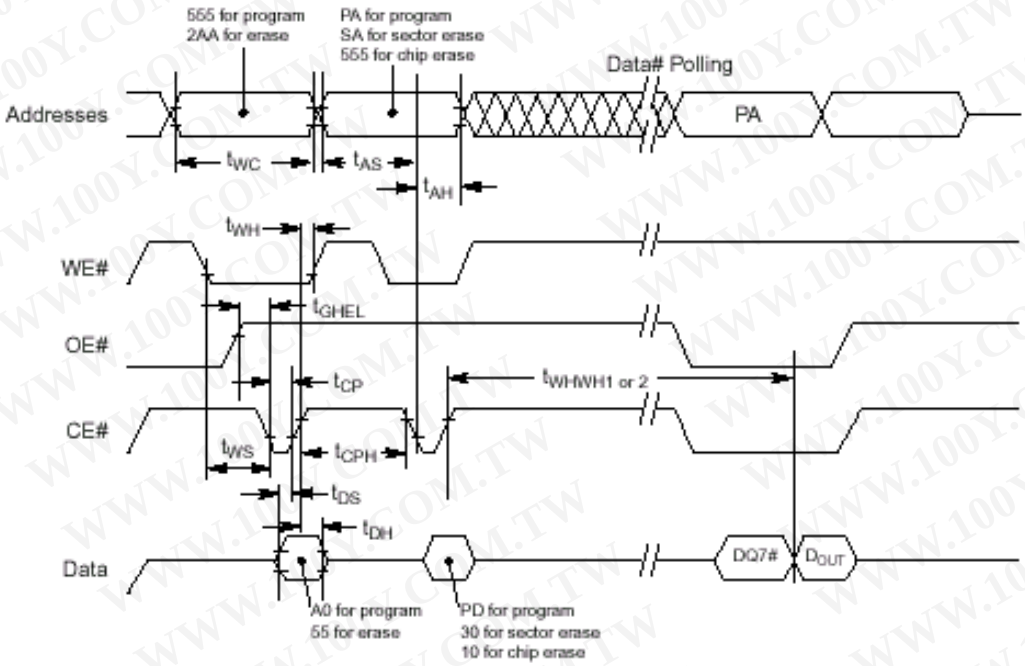

***Note:*** *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

**Figure 9. AC Waveforms for Toggle Bit During Embedded Algorithm Operations**




***Note:*** *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

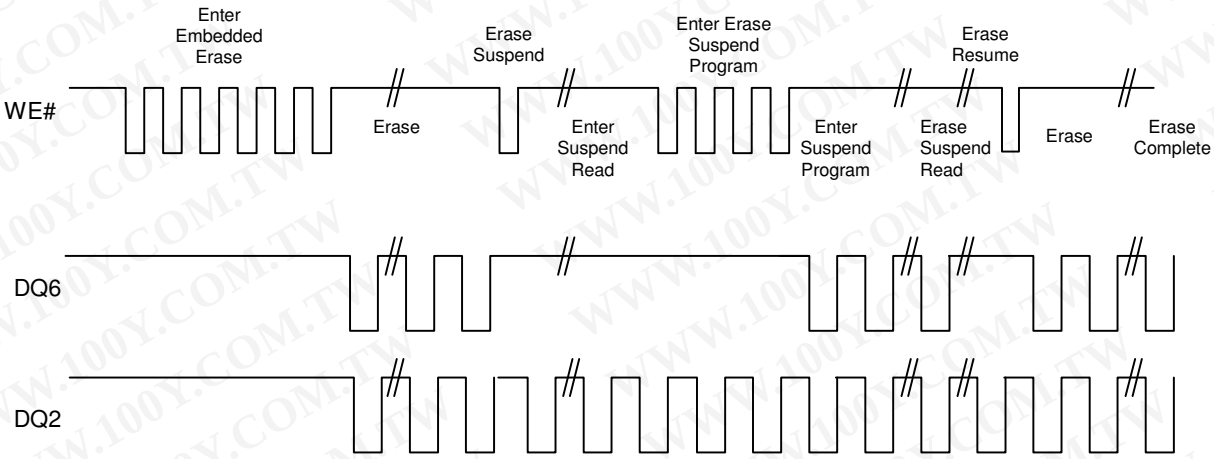
## Figure 10. Alternate CE# Controlled Write Operation Timings




***Notes:***

1. *PA = Program Address, PD = Program Data, DQ7# = complement of the data written to the device, $D_{OUT}$ is the data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*

## Figure 11. DQ2 vs. DQ6



## ABSOLUTE MAXIMUM RATINGS

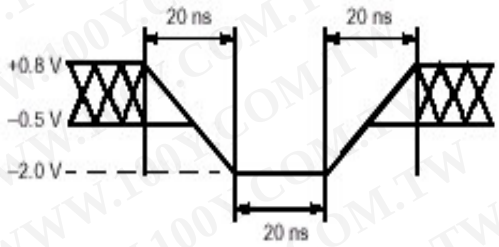
| Parameter | | Value | Unit |
|---|---|---|---|
| Storage Temperature | | -65 to +150 | °C |
| Plastic Packages | | -65 to +125 | °C |
| Ambient Temperature With Power Applied | | -55 to +125 | °C |
| Output Short Circuit Current[1] | | 200 | mA |
| Voltage with Respect to Ground | A9 and OE# [2] | -0.5 to +11.5 | V |
| | All other pins [3] | -0.5 to Vcc+0.5 | V |
| | Vcc | -0.5 to +4.0 | V |

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9 and OE# pins is –0.5V. During voltage transitions, A9 and OE# pins may undershoot $V_{SS}$ to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9 and OE# is 11.5V which may overshoot to 12.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot $V_{SS}$ to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is $V_{CC}$ + 0.5 V. During voltage transitions, outputs may overshoot to $V_{CC}$ + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

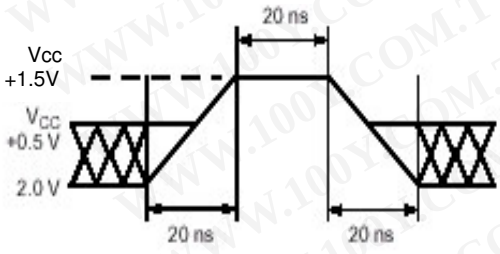
## RECOMMENDED OPERATING RANGES[1]

| Parameter | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Industrial Devices | -40 to 85 | °C |
| Operating Supply Voltage Vcc | Regulated Voltage Range: 3.0-3.6 | V |
| | Standard Voltage Range: 2.7 to 3.6 | |

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



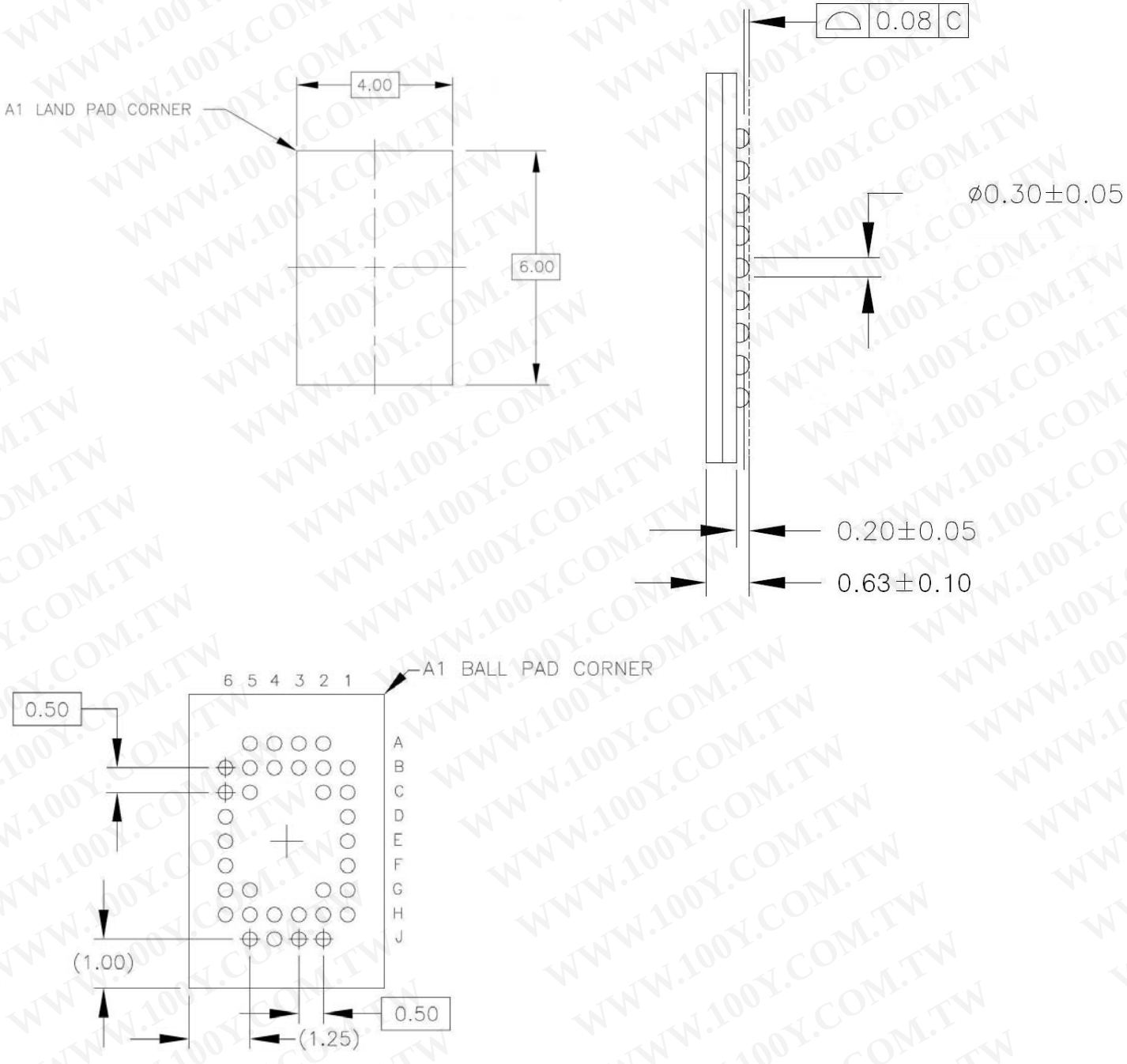

Maximum Negative Overshoot Waveform




Maximum Positive Overshoot Waveform

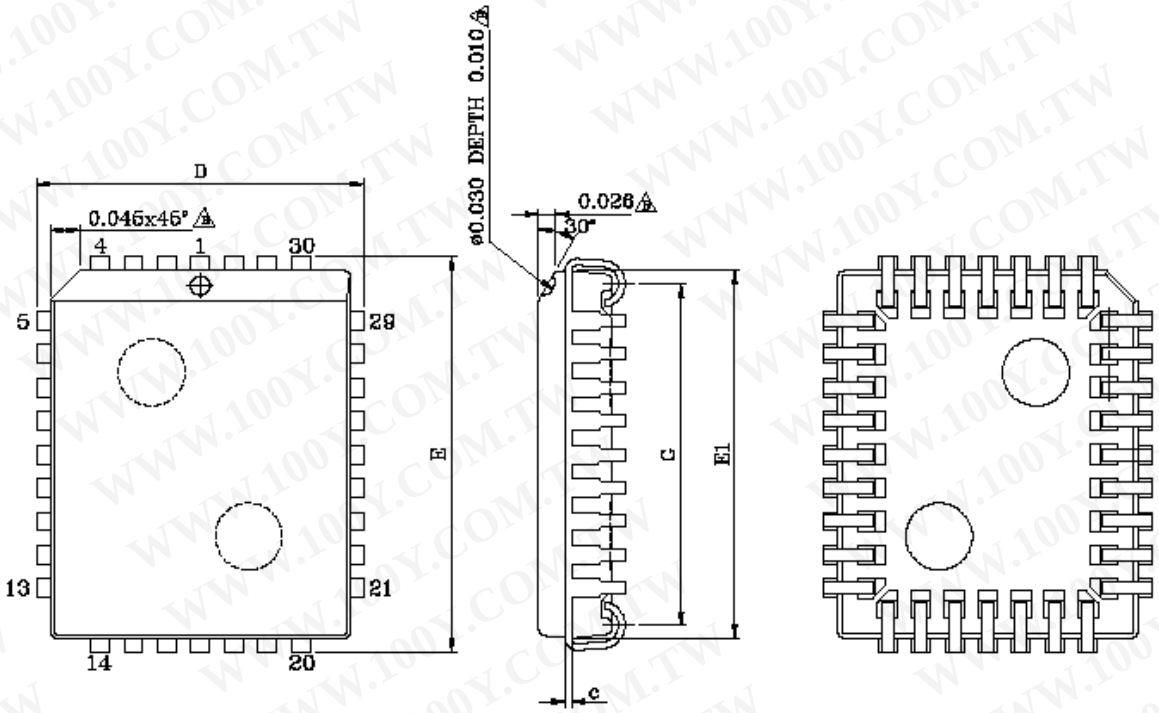
## PHYSICAL DIMENSIONS

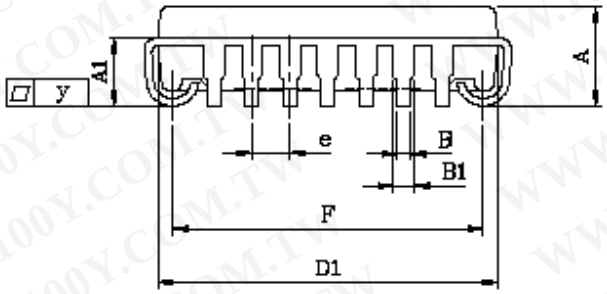
### 34-Ball Very-Very-Thin-Profile Fine Pitch Ball Grid Array (WFBGA)




**Note : Controlling dimensions are in millimeters (mm).**

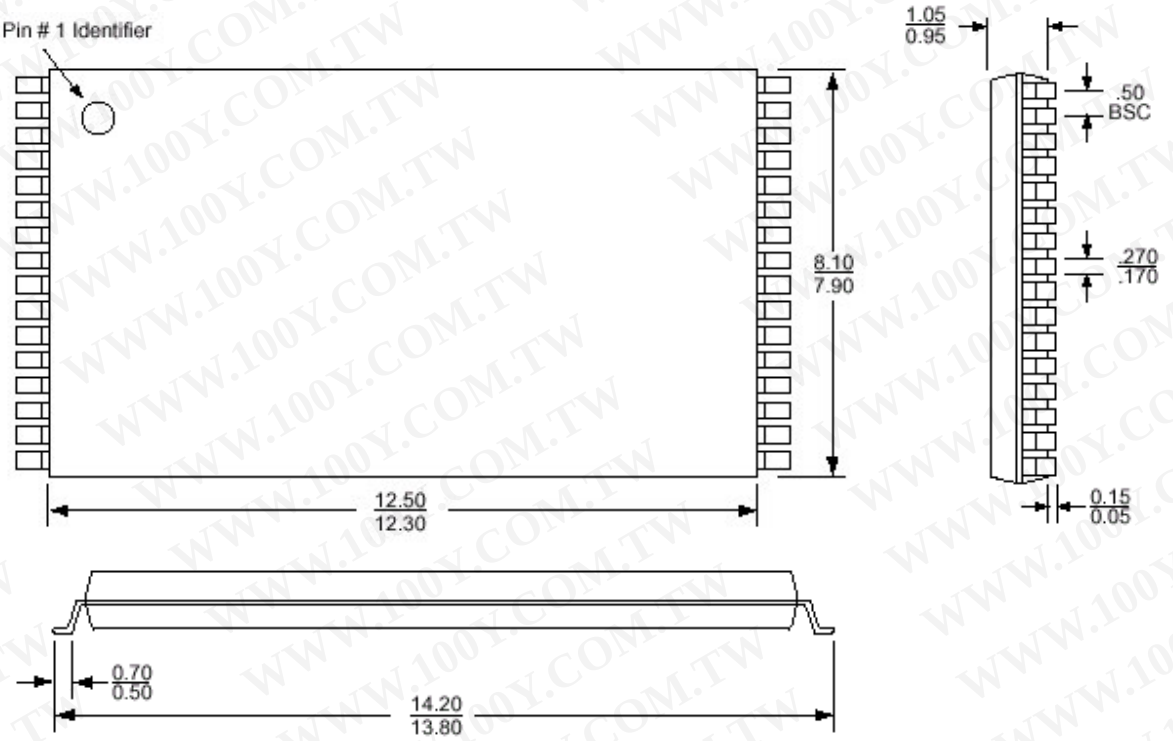
## PL 032 — 32-Pin Plastic Leaded Chip Carrier




| UNIT / SYMBOL | INCH(REF) | MM(BASE) |
|---|---|---|
| A | 0.130±0.008 | 3.302±0.203 |
| A1 | 0.080±0.006 | 2.032±0.152 |
| B | 0.018 $^{+0.004}_{-0.002}$ | 0.457 $^{+0.102}_{-0.051}$ |
| B1 | 0.028 $^{+0.004}_{-0.002}$ | 0.711 $^{+0.102}_{-0.051}$ |
| c | 0.010(TYP) | 0.254(TYP) |
| D | 0.490±0.005 | 12.446±0.127 |
| D1 | 0.450±0.003 | 11.430±0.076 |
| E | 0.590±0.005 | 14.986±0.127 |
| E1 | 0.550±0.003 | 13.970±0.076 |
| e | 0.050(TYP) | 1.270(TYP) |
| F | 0.410±0.010 | 10.414±0.254 |
| G | 0.510±0.010 | 12.954±0.254 |
| y | 0.003(MAX) | 0.076(MAX) |

## PHYSICAL DIMENSIONS (continued)
## 32L TSOP-1 8mm x 14mm




Note:
1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15mm at the package ends, and 0.25mm between leads.

## Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

## Eon products’ New Top Marking

cFeon

**cFeon Top Marking Example:**

**cFeon**
**Part Number: XXXX-XXX**
**Lot Number: XXXXX**
**Date Code: XXXXX**

## For More Information

Please contact your local sales office for additional information about Eon memory solutions.

## ORDERING INFORMATION

EN39LV010 — 70 S I P

**PACKAGING CONTENT**
(Blank) = Conventional
P = RoHS compliant

**TEMPERATURE RANGE**
I = Industrial (-40°C to +85°C)

**PACKAGE**
N = 34-Ball Very-Very-Thin-Profile Fine Pitch Ball Grid Array (WFBGA) 0.50mm pitch, 4mm x 6mm package
J = 32-pin Plastic PLCC
S = 32-pin 8mm x 14mm TSOP-1

**SPEED**
45R = 45ns Regulated range 3.0V~3.6V
70 = 70ns

**BASE PART NUMBER**
EN = Eon Silicon Solution Inc.
39 = 4K byte uniform sector
LV =FLASH, 3V Read, Program and Erase
010 = 1 Megabit (128K x 8)

## Revisions List

| Revision No | Description | Date |
|---|---|---|
| A | Initial release | 2009/1/23 |
| B | Modify program and erase time value in Table 11<br>Sector Erase time Max. 2→0.5sec.<br>Chip Erase time Typ. 0.25→3sec. Max. 2.5→15sec.<br>Byte Programming time Max. 200→20us.<br>Chip Programming time Typ. 1→0.8sec. Max. 1.6→2sec. | 2009/3/16 |