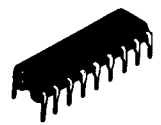
HM6148HLP Series

1024-word × 4-bit High Speed Static CMOS RAM

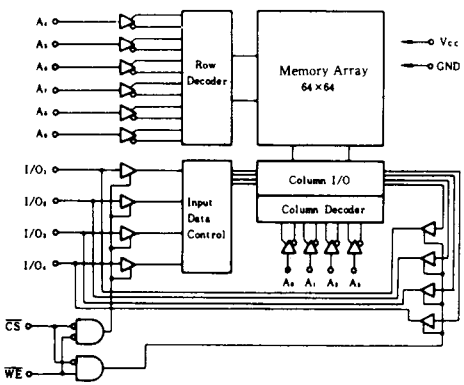


(DP-18)

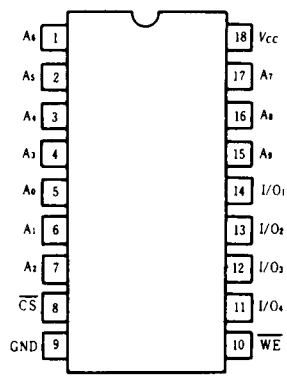
■ FEATURES

- Low Power Standby and Low Power Operation; Standby: 5μW (typ.), Operation: 175mW (typ.)
- Fast Access Time: 45/55ns (max)
- Capability of Battery Back Up Operation
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Three State Output
- Pin-Out Compatible with Intel 2148H

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage *	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature **	T_{bias}	−10 to +85	°C

* with respect to GND. V_{IL} min. = −3.5V (Pulse width = 20ns)
** under bias.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5*	—	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, GND=0V)

Parameter	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=max, V_{IN}=GND to V_{CC}	—	—	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2.0	μA
Operating Power Supply Current (1)	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	35	80	mA
Operating Power Supply Current (2)	I_{CC1}	min. cycle, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	50	100	mA
Standby Power Supply Current (1)	I_{SB}	$\overline{CS}$=V_{IH}	—	5	20	mA
Standby Power Supply Current (2)	I_{SB1}	$\overline{CS}$≥V_{CC}−0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}−0.2V	—	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V

* Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.

■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

Note) This parameter is sampled and not 100% tested.

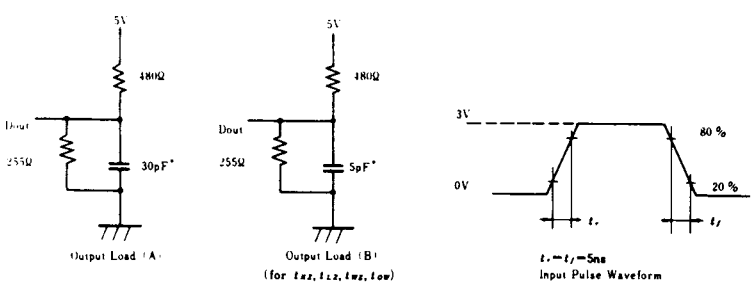
■ AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●RISE/FALL TIME

Item	Symbol	min	typ	max	Unit
Input Rise Time	t_r	—	5	100	ns
Input Fall Time	t_f	—	5	100	ns

●AC TEST CONDITIONS

Input pulse levels : GND to 3.0V
Input rise and fall times : 5ns
Input and Output timing reference levels : 1.5V
Output load : See Figure



* Including scope & jig.

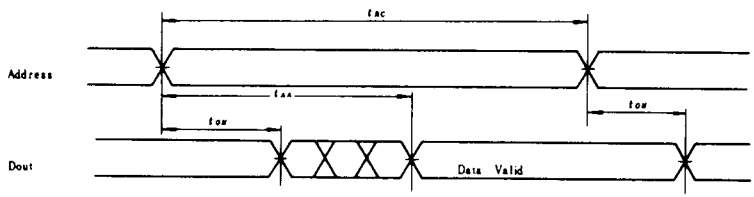
■AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V±10%, unless otherwise noted.)

●READ CYCLE

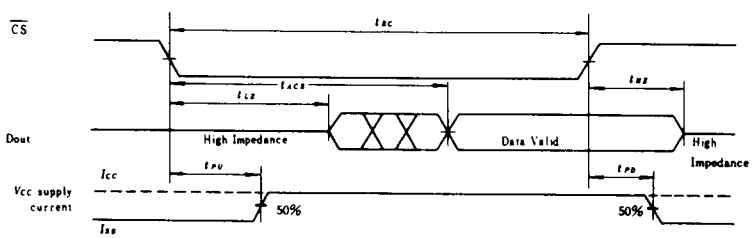
Item	Symbol	HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	45	—	55	—	ns
Address Access Time	t_{AA}	—	45	—	55	ns
Chip Select Access Time	t_{ACS}	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

* Transition is measured ±500mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

●TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



●TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

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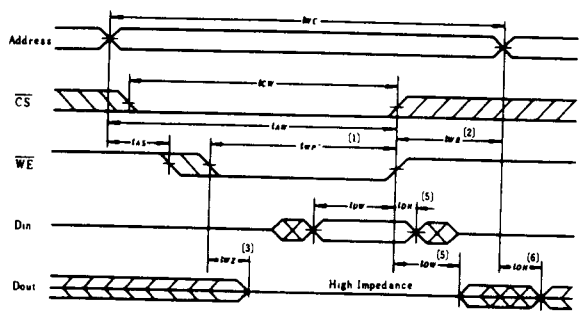
● WRITE CYCLE

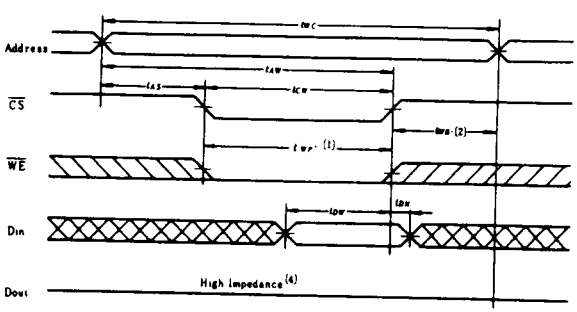
Item	Symbol	HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	45	—	55	—	ns
Chip Selection to End of Write	t_{CW}	40	—	50	—	ns
Address Valid to End of Write	t_{AW}	40	—	50	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	ns

* Transition is measured ±500mV from steady state voltage with Load B.
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ Controlled)



Notes of Timing Waveform of Write :
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} (1)	—	—	ns

Note) 1. t_{RC}=Read Cycle Time.

* V_{CC}=3.0V
** V_{CC}=2.0V

●LOW V_{CC} DATA RETENTION WAVEFORM