

**DESCRIPTION**

The HY62256A is a high-speed, low power and 32,786 x 8-bits CMOS Static Random Access Memory fabricated using Hyundai's high performance CMOS process technology. The HY62256A has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt. Using the CMOS technology, supply voltages from 2.0 to 5.5volt has little effect on supply current in the data retention mode. The HY62256A is suitable for use in low voltage operation and battery back-up application.

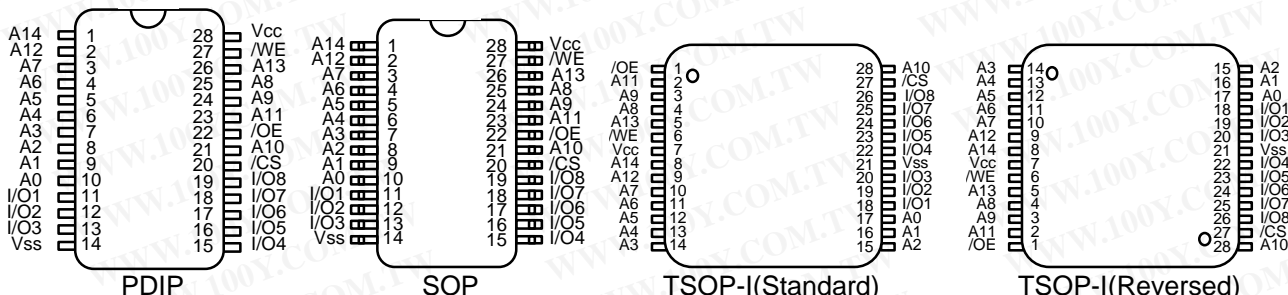
**FEATURES**

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
  - 2.0V(min.) data retention
- Standard pin configuration
  - 28 pin 600 mil PDIP
  - 28 pin 330mil SOP
  - 28 pin 8x13.4 mm TSOP-I (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)			Temperature (°C)
					L	LL	
HY62256A	5.0	55/70/85	50	1mA	100	25	0~70(Normal)

Note 1. Current value is max.

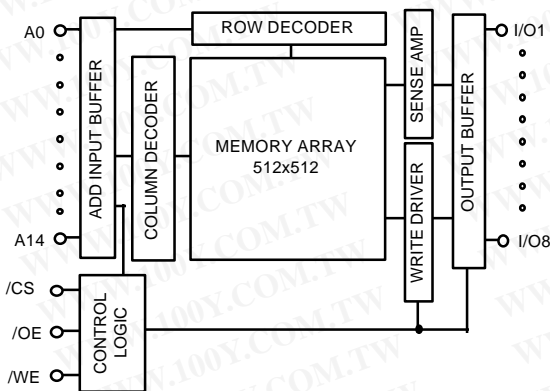
**PIN CONNECTION**



**PIN DESCRIPTION**

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

**BLOCK DIAGRAM**



### ORDERING INFORMATION

Part No.	Speed	Power	Package
HY62256AP	55/70/85		PDIP
HY62256ALP	55/70/85	L-part	PDIP
HY62256ALLP	55/70/85	LL-part	PDIP
HY62256AJ	55/70/85		SOP
HY62256ALJ	55/70/85	L-part	SOP
HY62256ALLJ	55/70/85	LL-part	SOP
HY62256AT1	55/70/85		TSOP-I Standard
HY62256ALT1	55/70/85	L-part	TSOP-I Standard
HY62256ALLT1	55/70/85	LL-part	TSOP-I Standard
HY62256AR1	55/70/85		TSOP-I Reversed
HY62256ALR1	55/70/85	L-part	TSOP-I Reversed
HY62256ALLR1	55/70/85	LL-part	TSOP-I Reversed

### ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit
V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub>	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
T <sub>A</sub>	Operating Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
P <sub>D</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	Data Output Current	50	mA
T <sub>SDER</sub>	Lead Soldering Temperature & Time	260 • 0	°C•sec

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

T<sub>A</sub>=0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5(1)	-	0.8	V

Note

- V<sub>IL</sub> = -3.0V for pulse width less than 30ns

### TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note :

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=Don't Care

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### DC CHARACTERISTICS

V<sub>CC</sub> = 5V±10%, T<sub>A</sub> = 0°C to 70°C (Normal) unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	1	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , /CS = V <sub>IH</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	μA	
I <sub>CC</sub>	Operating Power Supply Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	30	50	mA	
I <sub>CC1</sub>	Average Operating Current	/CS = V <sub>IL</sub> , Min. Duty Cycle = 100%, I <sub>I/O</sub> = 0mA	-	40	70	mA	
I <sub>SB</sub>	TTL Standby Current (TTL Inputs)	/CS = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	0.4	2	mA	
I <sub>SB1</sub>	CMOS Standby Current (CMOS Inputs)	/CS ≥ V <sub>CC</sub> - 0.2V	-	-	1	mA	
		V <sub>IN</sub> ≤ 0.2V or	L	-	2	100	μA
		V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	LL	-	1	25	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.4	-	-	V	

Note : Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C

### AC CHARACTERISTICS

V<sub>CC</sub> = 5V±10%, T<sub>A</sub> = 0°C to 70°C (Normal) unless otherwise specified.

#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	TRC	Read Cycle Time	55	-	70	-	85	-	ns
2	TAA	Address Access Time	-	55	-	70	-	85	ns
3	TACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	TOE	Output Enable to Output Valid	-	30	-	35	-	45	ns
5	TCLZ	Chip Select to Output in Low Z	5	-	5	-	5	-	ns
6	TOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	TCHZ	Chip Deselection to Output in High Z	0	20	0	30	0	30	ns
8	TOHZ	Out Disable to Output in High Z	0	20	0	30	0	30	ns
9	TOH	Output Hold from Address Change	5	-	5	-	5	-	ns
WRITE CYCLE									
10	TWC	Write Cycle Time	55	-	70	-	85	-	ns
11	TCW	Chip Selection to End of Write	50	-	65	-	75	-	ns
12	TAW	Address Valid to End of Write	50	-	65	-	75	-	ns
13	TAS	Address Set-up Time	0	-	0	-	0	-	ns
14	TWP	Write Pulse Width	40	-	50	-	55	-	ns
15	TWR	Write Recovery Time	0	-	0	-	0	-	ns
16	TWHZ	Write to Output in High Z	0	20	0	30	0	30	ns
17	TDW	Data to Write Time Overlap	25	-	35	-	40	-	ns
18	TDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	TOW	Output Active from End of Write	5	-	5	-	5	-	ns

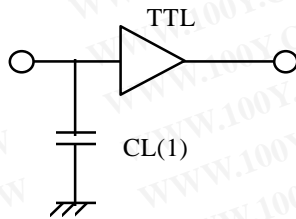
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### AC TEST CONDITIONS

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Normal) unless otherwise specified.

PARAMETER		VALUE
Input Pulse Level		0.8V to 2.4V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Levels		1.5V
Output Load	70/85/100ns	CL = 100pF + 1TTL Load
	55ns	CL = 50pF + 1TTL Load

### AC TEST LOADS



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Note : Including jig and scope capacitance

### CAPACITANCE

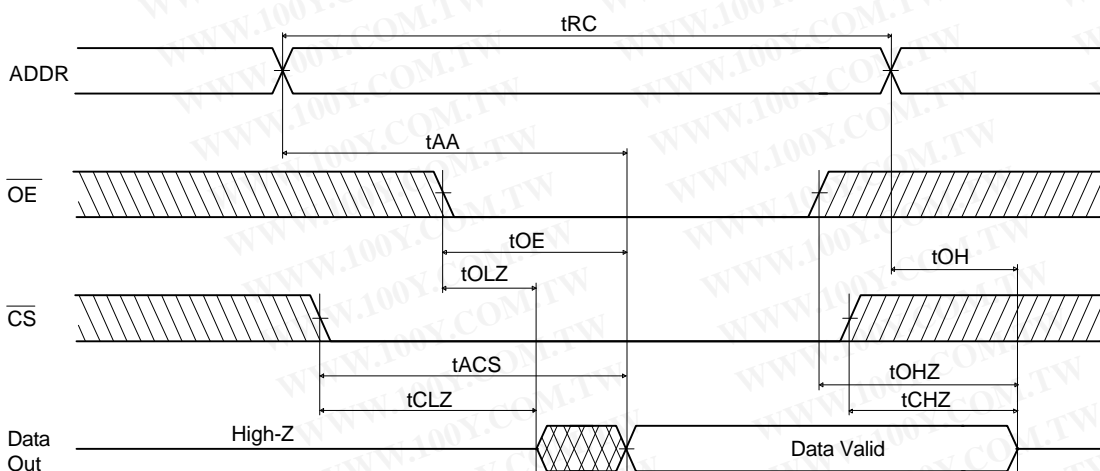
$T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$

Symbol	Parameter	Condition	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O} = 0V$	8	pF

Note : These parameters are sampled and not 100% tested

### TIMING DIAGRAM

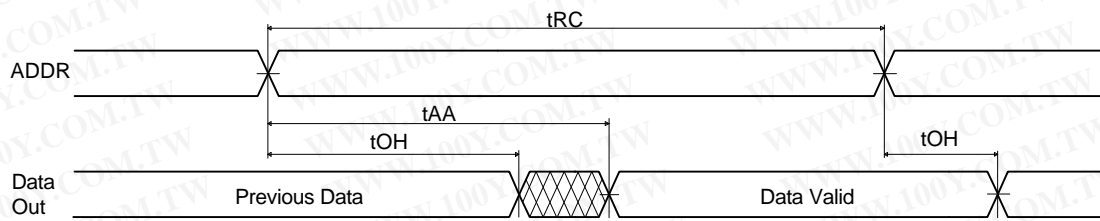
#### READ CYCLE 1



**Note(READ CYCLE):**

1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

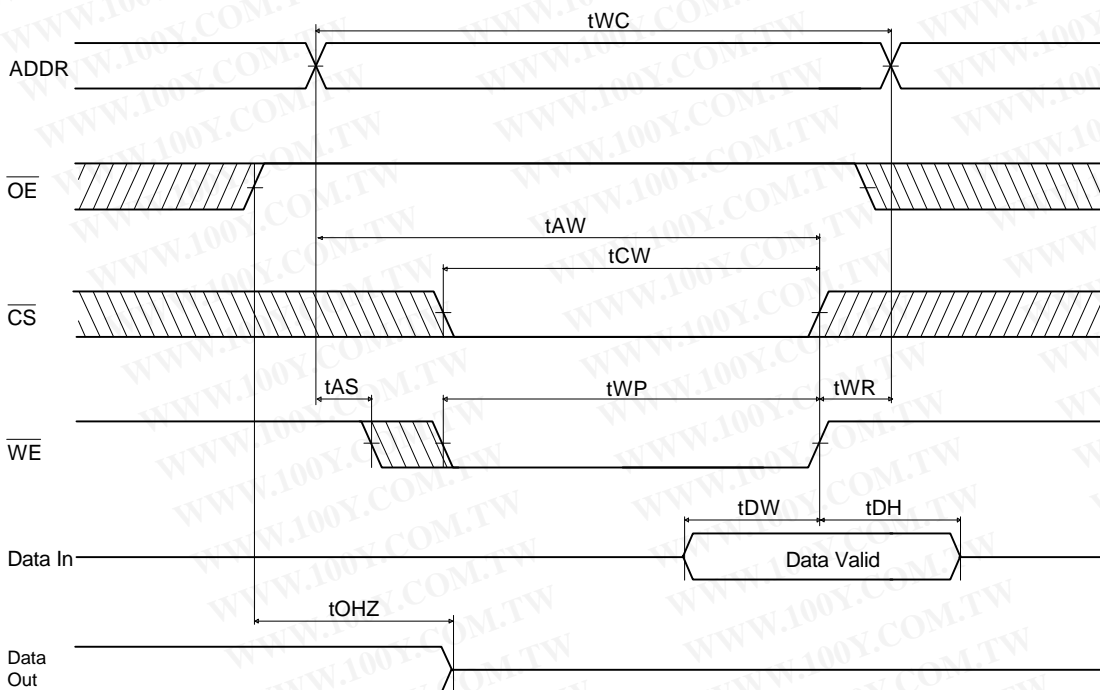
**READ CYCLE 2**



**Note(READ CYCLE):**

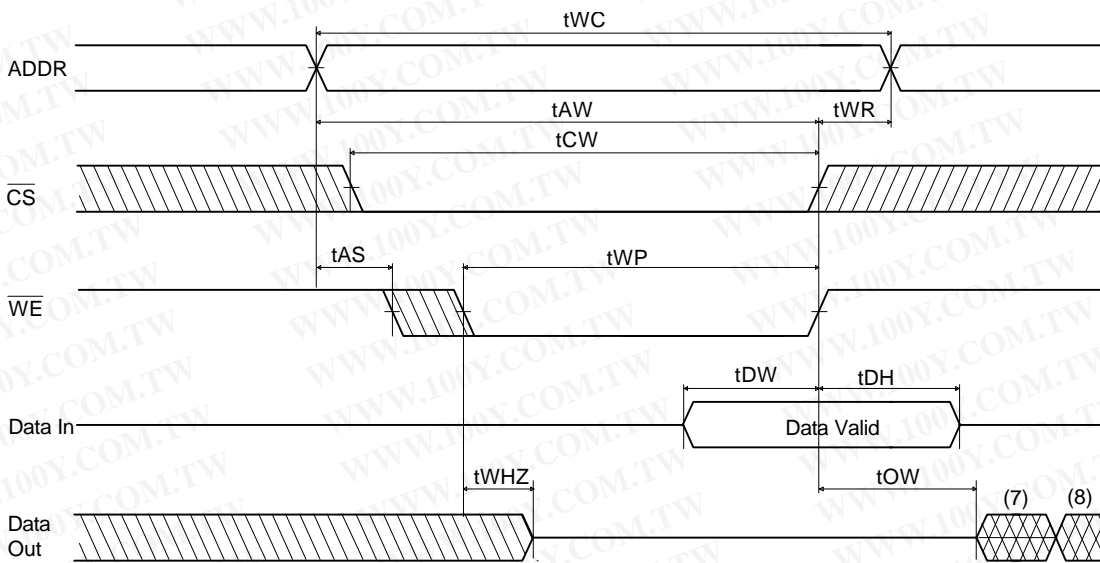
1. /WE is high for the read cycle.
2. Device is continuously selected /CS= VIL.
3. /OE =VIL.

**WRITE CYCLE 1(/OE Clocked)**



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### WRITE CYCLE 2 (/OE Low Fixed)



#### Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of latest written data in this write cycle.
8. DOUT is the read data of the new address.

### DATA RETENTION CHARACTERISTIC

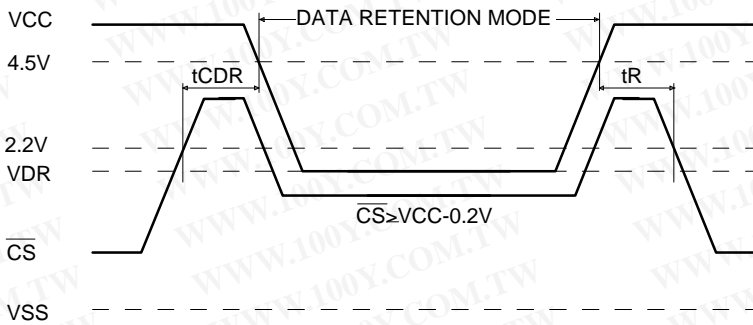
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDR	V <sub>cc</sub> for Data Retention	/CS ≥ V <sub>cc</sub> -0.2V, V <sub>ss</sub> ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	2	-	-	V
ICCDR	Data Retention Current	V <sub>cc</sub> = 3.0V, /CS ≥ V <sub>cc</sub> - 0.2V	L	1	50	uA
		V <sub>ss</sub> ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	LL	1	15(2)	uA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time		tRC(3)	-	-	ns

#### Notes

1. Typical values are under the condition of T<sub>A</sub> = 25°C.
2. 3uA max. at T<sub>A</sub>=0°C to 40 °C.
3. tRC is read cycle time.

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**Data Retention Timing Diagram**



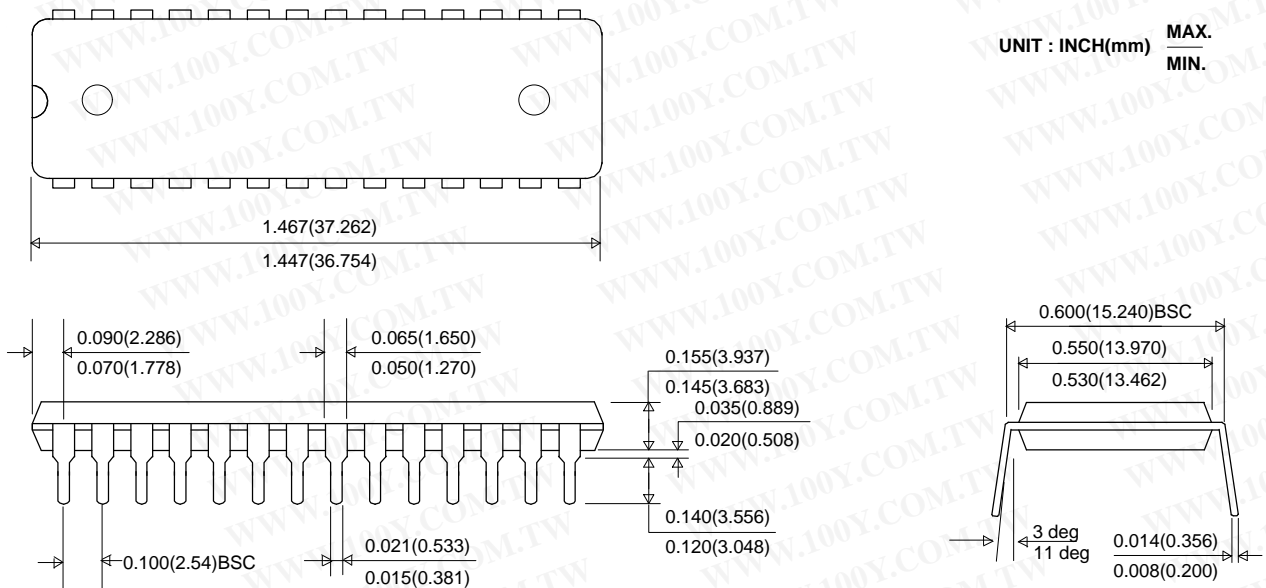
**RELIABILITY SPEC.**

TEST MODE		TEST SPEC.
ESD	HBM	≥2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

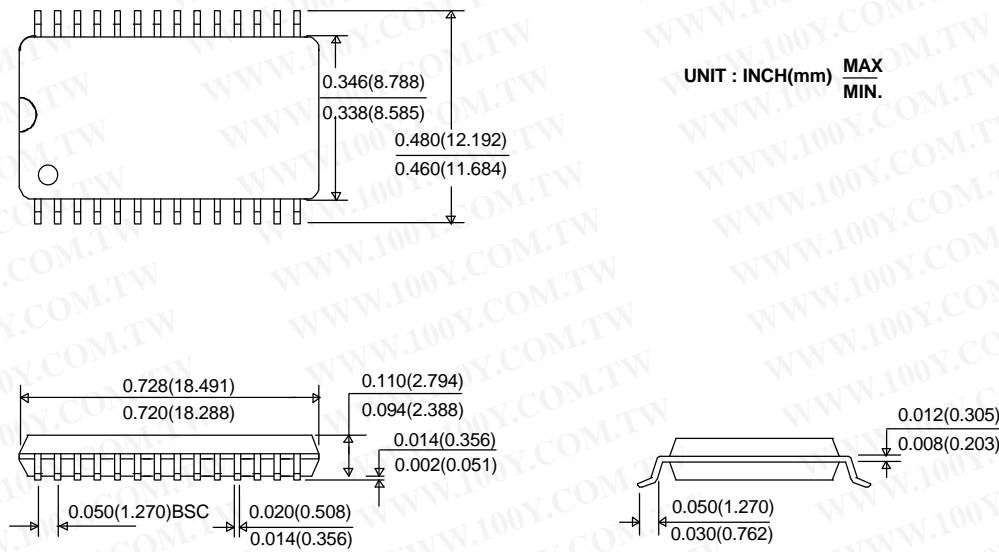
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**PACKAGE INFORMATION**

28pin 600mil Dual In-Line Package(P)

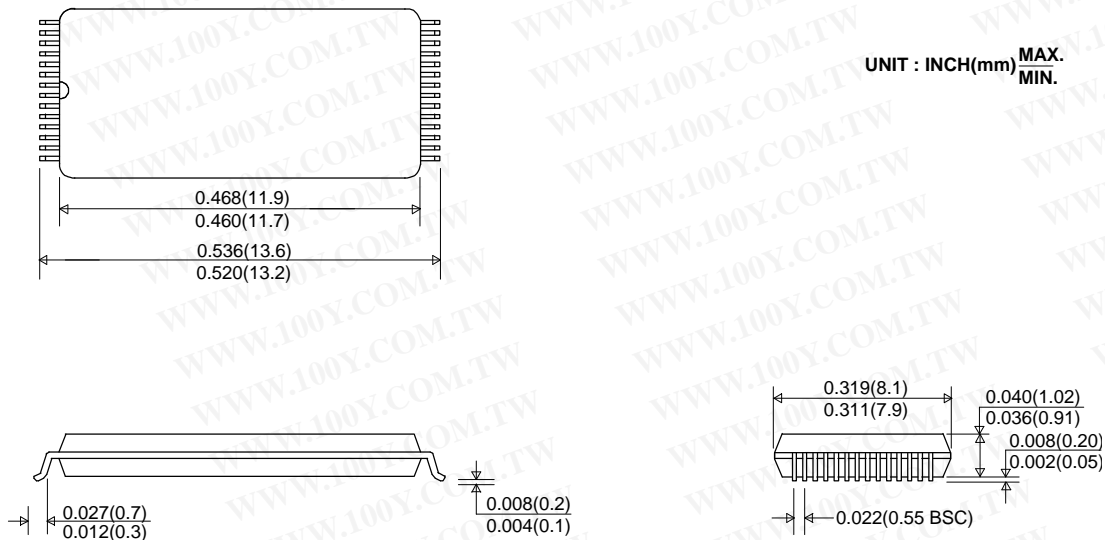


28pin 330mil Small Outline Package(J)



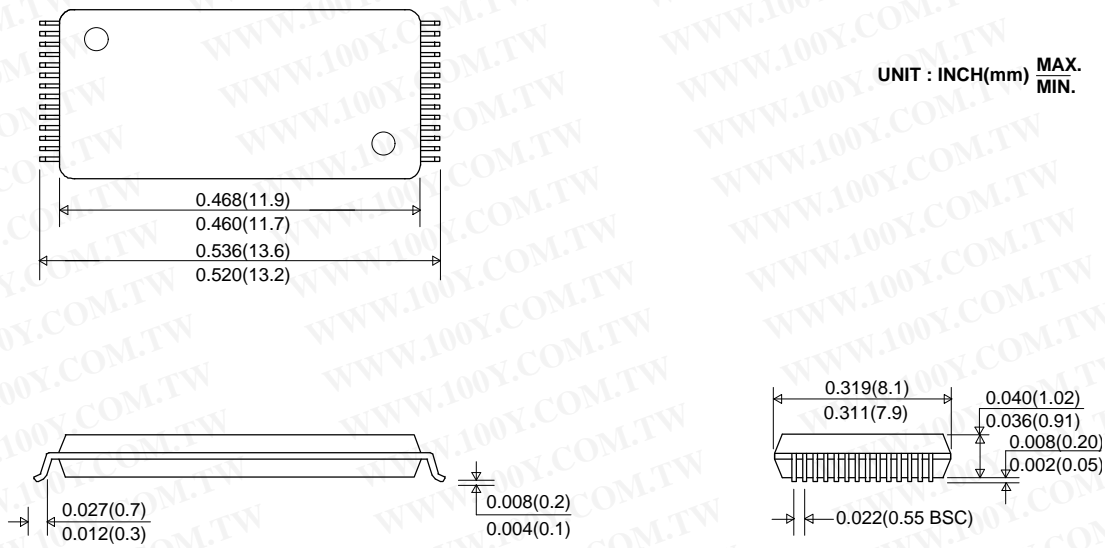
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28pin 8x13.4mm Thin Small Outline Package Standard(T1)





### 28pin 8x13.4mm Thin Small Outline Package Reversed(R1)



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