512K SPI Low Power Serial SRAM

Part Number	Vcc Range	MHz (max)	Density	Temp. Ranges	Package
IP12B512C-T	2.7 - 3.6V	20	512Kb	-20℃ to +70℃	TSSOP-8
IP12B512I-T	2.7 - 3.6V	20	512Kb	-40℃ to +85℃	TSSOP-8

Features:

- Max Clock 20MHz
- SPI-Compatible Interface (Mode0 and Mode3)
- Low-Power CMOS Technology:
  - Operating current: max. 2mA @ 1MHz
  - Standby current: typ. 10uA @ +25℃
- 65.536 x 8-bit Organisation
- 32-Byte Page
- Hold pin for pausing communication
- Sequential Read/Write
- Flexible operating modes
  - Byte read and write (BYTE)
  - Page mode (PAGE)
  - Pagestart Sequential mode (PSEQ)
  - Virtual chip mode (VRTM)
- Infinite read/writes to memory array
- Temperature range
  - -20℃ to +70℃ (Consumer grade)
  - -40℃ to +85℃ (Industrial grade)
- RoHS compliant package

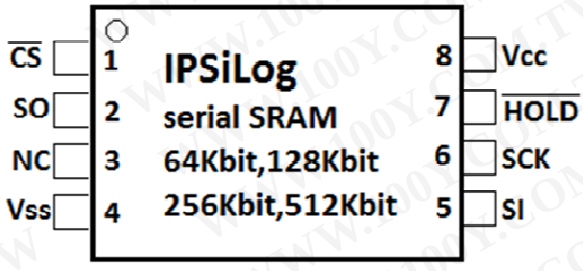
Description:

The IPSiLog Semiconductor GmbH serial SRAM family IP12xxxxx includes several integrated memory devices including this 512Kb serially accessed Static Random Access Memory, internally organized as 64K words by 8 bits each. The devices are designed and fabricated using state of the art advanced CMOS technology to provide both high-speed performance and low power. The devices operate with a single chip select (/CS) input and are accessed by a simple serial interface that is SPI-compatible. A single data in and data out line is used along with a clock to access data within the devices. The IP12xxxxx devices include a /HOLD pin that allows communication with the device to be paused without deselecting the device. While paused, input transitions except /CS pin will be ignored. The devices can operate over a temperature range of -20°C to +70°C (Consumer grade) and -40°C to +85°C (Industrial grade), both are available in space-saving 8-lead TSSOP package.

Pin Function Table

Pin Name	Pin Function
$\overline{CS}$	Chip Select Input
SO	Serial data Output
NC	---
Vss	Ground
SI	Serial data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
Vcc	Supply Voltage

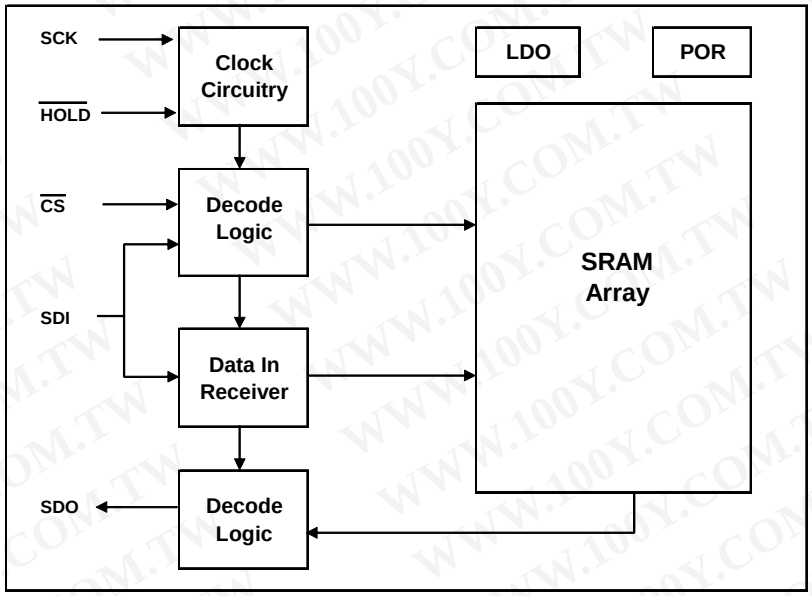
Package Outline



Functional pin description

Pin Name	Pin Function		Functional pin description
$\overline{\text{CS}}$	Chip Select Input	Input	A low level selects the device and a high level puts the device in standby mode. If /CS is brought high (device deselected), SO goes to high-impedance state. /CS must be driven low after power-up prior to any sequence being started.
SO	Serial data Output	Output	Data is shifted out bit by bit after each falling edge of SCK.
NC	---	---	-----
Vss	Ground	---	VSS is the reference for the VCC supply voltage.
SI	Serial data Input	Input	Receives instructions, addresses and data, latched on the rising edge of SCK.
SCK	Serial Clock Input	Input	Synchronizes all activities between the SRAM and controller. All incoming addresses, data and instructions are latched on the rising edge of SCK. Data out is updated on SO after the falling edge of SCK.
$\overline{\text{HOLD}}$	Hold Input	Input	A high level is required for normal operation. Once the device is selected and a serial sequence is started, this input may be taken low to pause serial communication without resetting the serial sequence. The pin must be brought low while SCK is low for immediate use. If SCK is not low, the Hold function will not be invoked until the next SCK high to low transition. The device must remain selected during this sequence. SO is high-impedance during the Hold time and SI and SCK are ignored. To resume operations, /HOLD must be pulled high while the SCK pin is low. Lowering the /HOLD input at any time will take the SO output to high-impedance. The Hold functionality can be disabled by bit0 of the STATUS register.
Vcc	Supply Voltage	---	During all operations, VCC must be held stable and within the specified valid range: VCC(min) to VCC(max).

Functional Block Diagram



Absolute Maximum Ratings †

VCC.....4.4V (for IP12B512x)
All inputs and outputs relative to VSS ..... -0.3V to VCC +0.3V
Storage temperature ..... -65℃ to +150℃
Operating temperature ..... -20℃ to +70℃ (for IP12B512C)
Operating temperature ..... -40℃ to +85℃ (for IP12B512I)
Soldering temperature and time ..... 260℃, 10sec
ESD protection on all pins..... 2kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those indicated in the operating section of this specification, is not implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Min.	Typ	Max	Unit	Test Condition
Supply Voltage	Vcc	2.7	3.0	3.6	V	IP12B512x-T
Input High Voltage	VIH	0.7 * Vcc	---	Vcc +0.3	V	---
Input Low Voltage	VIL	-0.3	---	0.2 * Vcc	V	---
Output High Voltage	VOH	Vcc - 0.5	---	---	V	IOH = -0.4mA
Output Low Voltage	VOL	---	---	0.2	V	IP12B512x-T, IOL = 1.0mA
Input Leakage Current	ILI	---	---	+- 0.5	uA	CS = Vcc, Vin =0 to Vcc
Output Leakage Current	ILO	---	---	+- 0.5	uA	CS = Vcc, Vout =0 to Vcc
Read/Write Operating Current	Icc1	---	---	2	mA	F = 1MHz, Iout = 0
	Icc2	---	---	7	mA	F = 10MHz, Iout = 0
	Icc3	---	---	12	mA	F = fmax, Iout = 0
Standby Current	ISB1	---	10 Note1	15	uA	CS = Vcc , Vin = Vss or Vcc @25℃
	ISB2	---	---	150	uA	CS = Vcc , Vin = Vss or Vcc @85℃
Input Capacitance	CIN	---	---	6 Note2	pF	Vin = 0V, F = 1MHz, Ta = 25℃
I/O Capacitance	CIO	---	---	6 Note2	pF	Vin = 0V, F = 1MHz, Ta = 25℃

Note1: Typical values are measured at Vcc=VccTyp and 25℃ and are not 100% tested

Note2: Characterized value, not tested in production

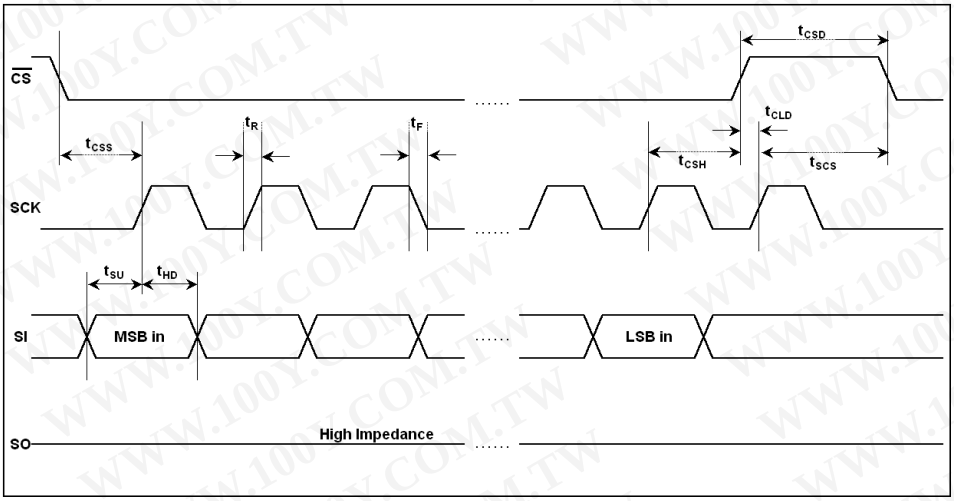
Timing test conditions

Item	
Input Pulse Level	0.1* Vcc to 0.9* Vcc
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5* Vcc
Output Load	CL = 100pF
Operating Temperature (IP12B512C)	-20℃ to +70℃
Operating Temperature (IP12B512I)	-40℃ to +85℃

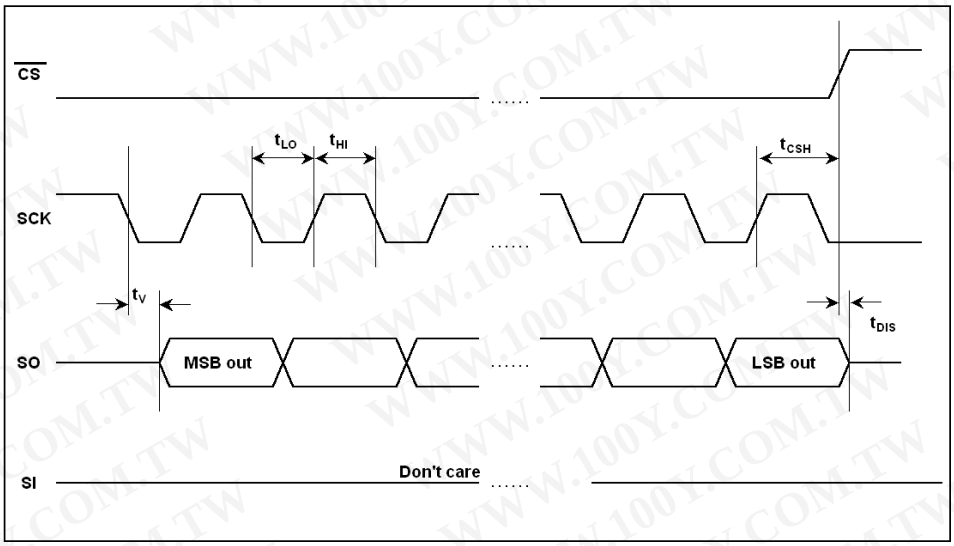
Timing (over specified temperature range)

Item	Symbol	Min.	Max.	Unit	Test Condition
Clock Frequency	fCLK	---	20	MHz	Vcc = 3.0V
Clock Rise Time	tR	---	2	us	
Clock Fall Time	tF	---	2	us	
Clock High Time	tHI	25	---	ns	
Clock Low Time	tLO	25	---	ns	
Clock Delay Time	tCLD	25	---	ns	
CS Setup Time	tCSS	25	---	ns	
CS Hold Time	tCSH	50	---	ns	
CS Disable Time	tCSD	25	---	ns	
SCK to CS	tSCS	5	---	ns	
Data Setup Time	tSU	10	---	ns	
Data Hold Time	tHD	10	---	ns	
Output Valid From Clock Low	tV	---	25	ns	
Output Hold Time	tHO	0	---	ns	
Output Disable Time	tDIS	---	20	ns	
HOLD Setup Time	tHS	10	---	ns	
HOLD Hold Time	tHH	10	---	ns	
HOLD Low to Output High-Z	tHZ	10	---	ns	
HOLD High to Output Valid	tHV	---	50	ns	

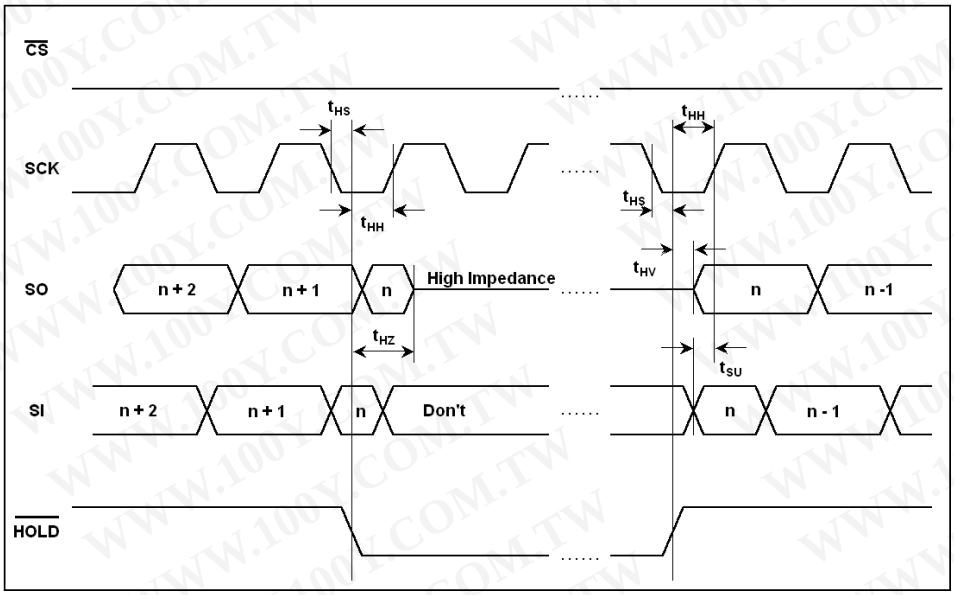
Serial Input Timing



Serial Output Timing



Hold timing



Description of Functional Operation

Basic Operation

The 512Kb serial SRAM is designed to interface directly with a standard 4wire Serial Peripheral Interface (SPI) implemented in many standard micro-controllers. If the device has no SPI-Hardware interface, the necessary protocol can be applied using standard I/O-port by programming (Software-SPI). The serial SRAM contains an 8-bit instruction register and is accessed via the SI pin. The /CS pin must be low and the /HOLD pin must be high for the entire operation. Data is clocked in, starting on the first rising edge of SCK after /CS goes low. If the clock line is shared by several devices, the user can assert the /HOLD input and put the device into a Hold mode. After releasing the /HOLD pin, the operation will resume from the point where it was held. The transfer sequence for all instructions, addresses and data is MSB first, LSB last.

Instruction Set

Instruction Name	Instruction Format (binary)	Instruction Format (hex)	Description
READ	0000 0011	0x03	Read memory data beginning at selected address
WRITE	0000 0010	0x02	Write memory data beginning at selected address
RDSR	0000 0101	0x05	Read status register
WRSR	0000 0001	0x01	Write status register
RDMI	0000 1110	0x0E	Read Memory Size

READ Operations

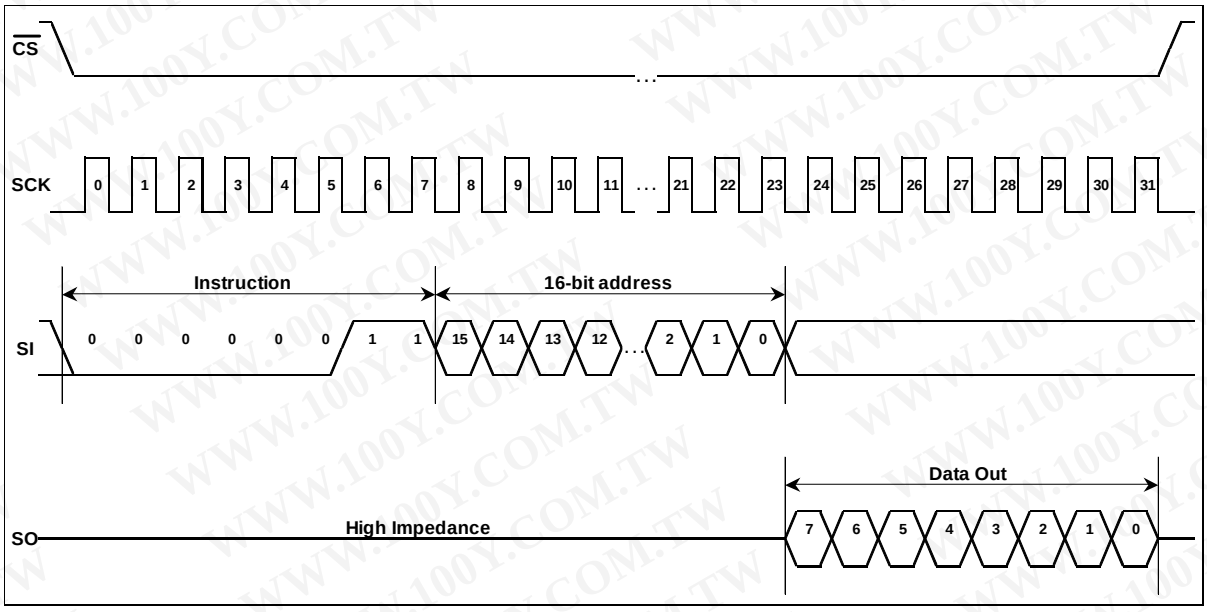
The serial SRAM READ is selected by pulling /CS low. First, the 8-bit READ instruction is transmitted to the device followed by the 16-bit address with the first bit as MSB. After the READ instruction and addresses are sent, the data stored at that address in memory is shifted out on the SO pin after the output valid time from the clock edge.

If operating in page mode, after the initial byte of data is shifted out, the data stored at the next memory location on the page can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each byte of data is read out. This can be continued for the entire page length of 32 bytes. At the end of the page, the addresses pointer wraps back to the 0 byte address within the page and the operation can be continuously looped over the 32 bytes of the same page.

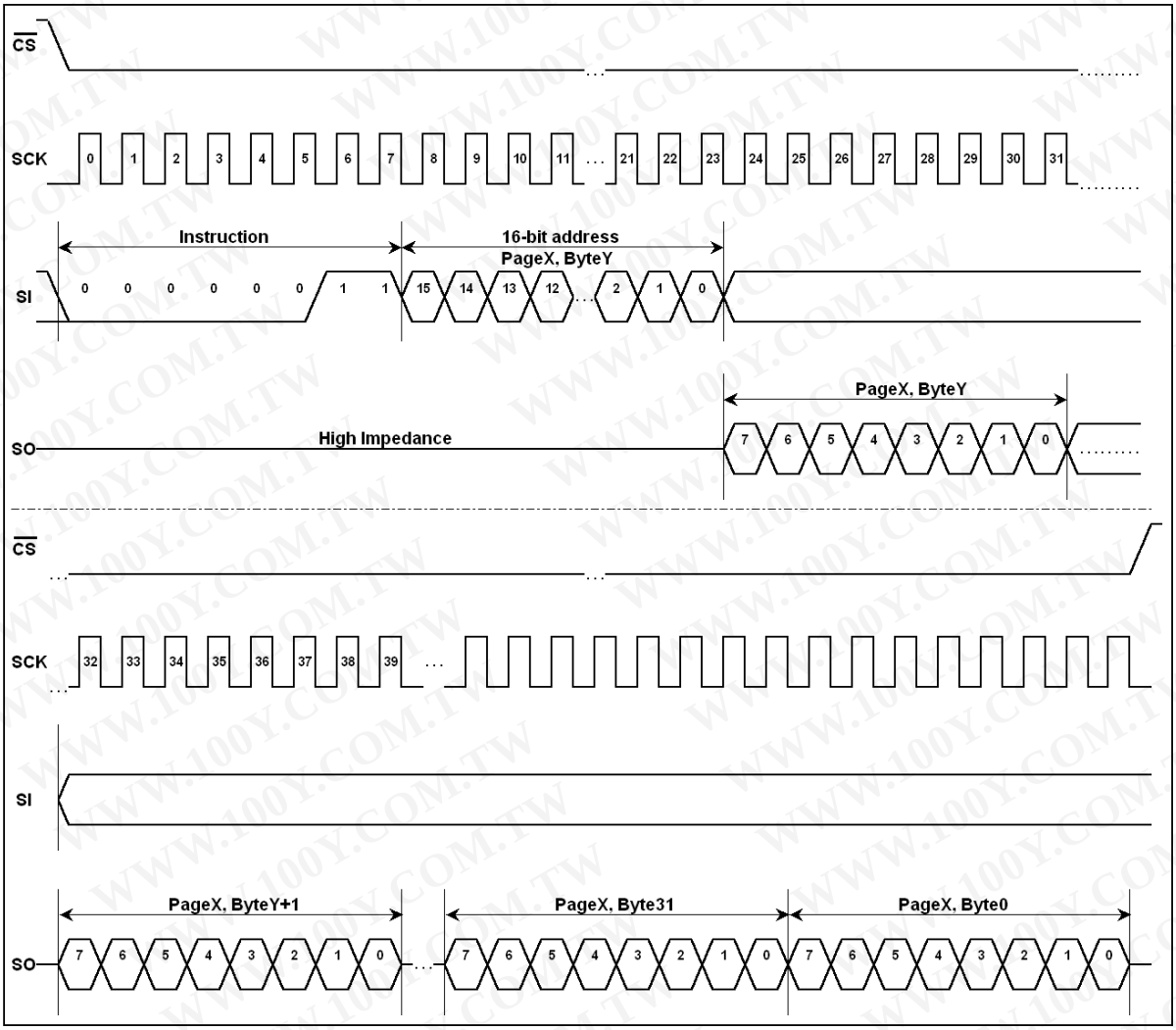
If operating in pagestart sequential (PSEQ) mode, the operation is always starting at the address 00h of the selected page by default. After the initial byte of data is shifted out, the data stored at the next memory location can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is read out. This can be continued for the entire array and when the highest address is reached (FFFFh), the address counter wraps to the address 0000h. This allows the pagestart sequential (PSEQ) read cycle to be continued indefinitely. All READ operations are terminated by pulling /CS high.

If operating in virtual chip (VRTM) mode, after the initial byte of data is shifted out, the data stored at the next memory location can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is read out. This can be continued for the entire array and when the highest address is reached (FFFFh), the address counter wraps to the address that was selected as the starting address of the virtual chip command. This allows the virtual chip (VRTM) read cycle to be continued indefinitely within the selected start-address and the highest address of the full array. All READ operations are terminated by pulling /CS high.

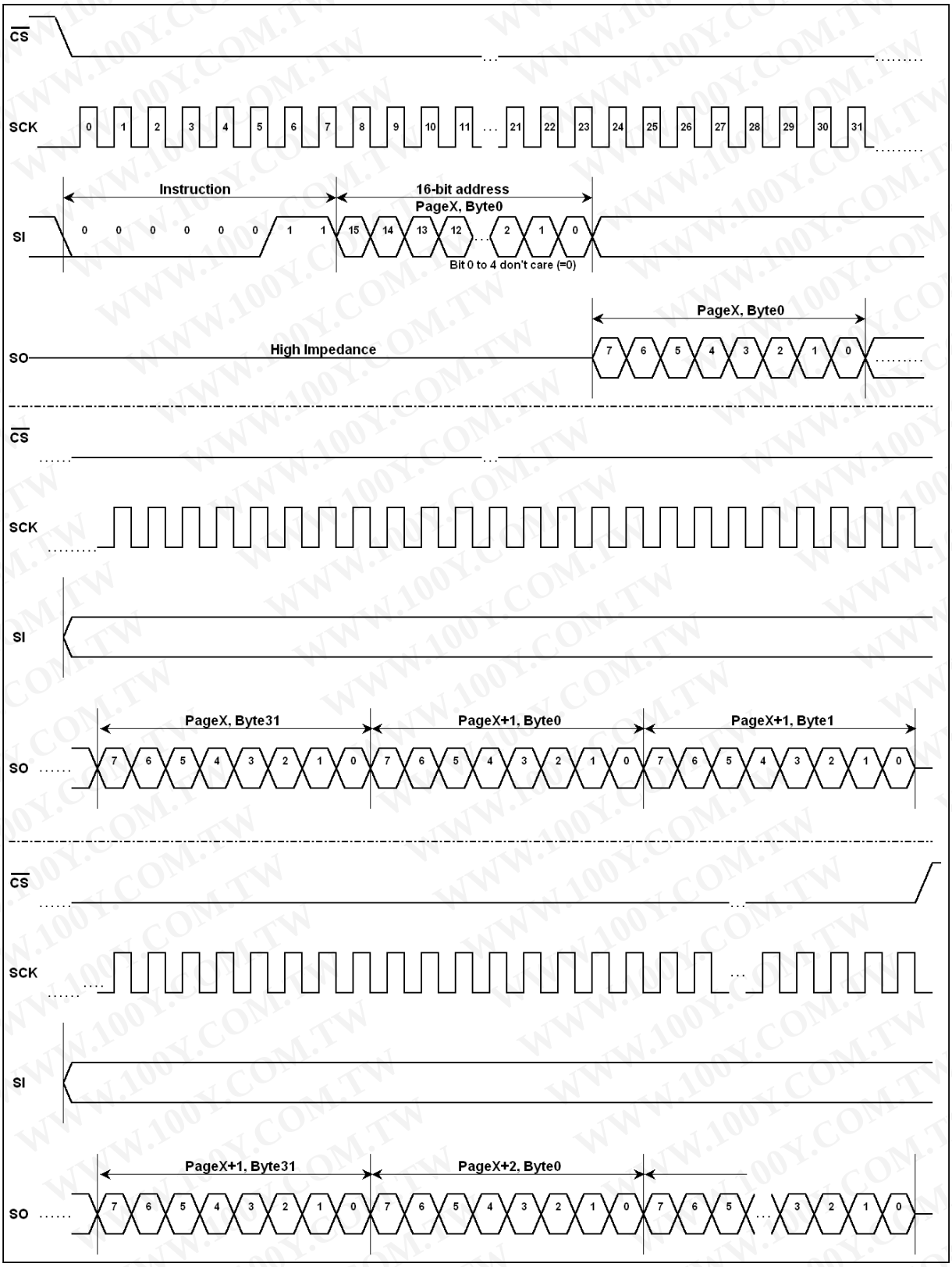
Byte Read Sequence



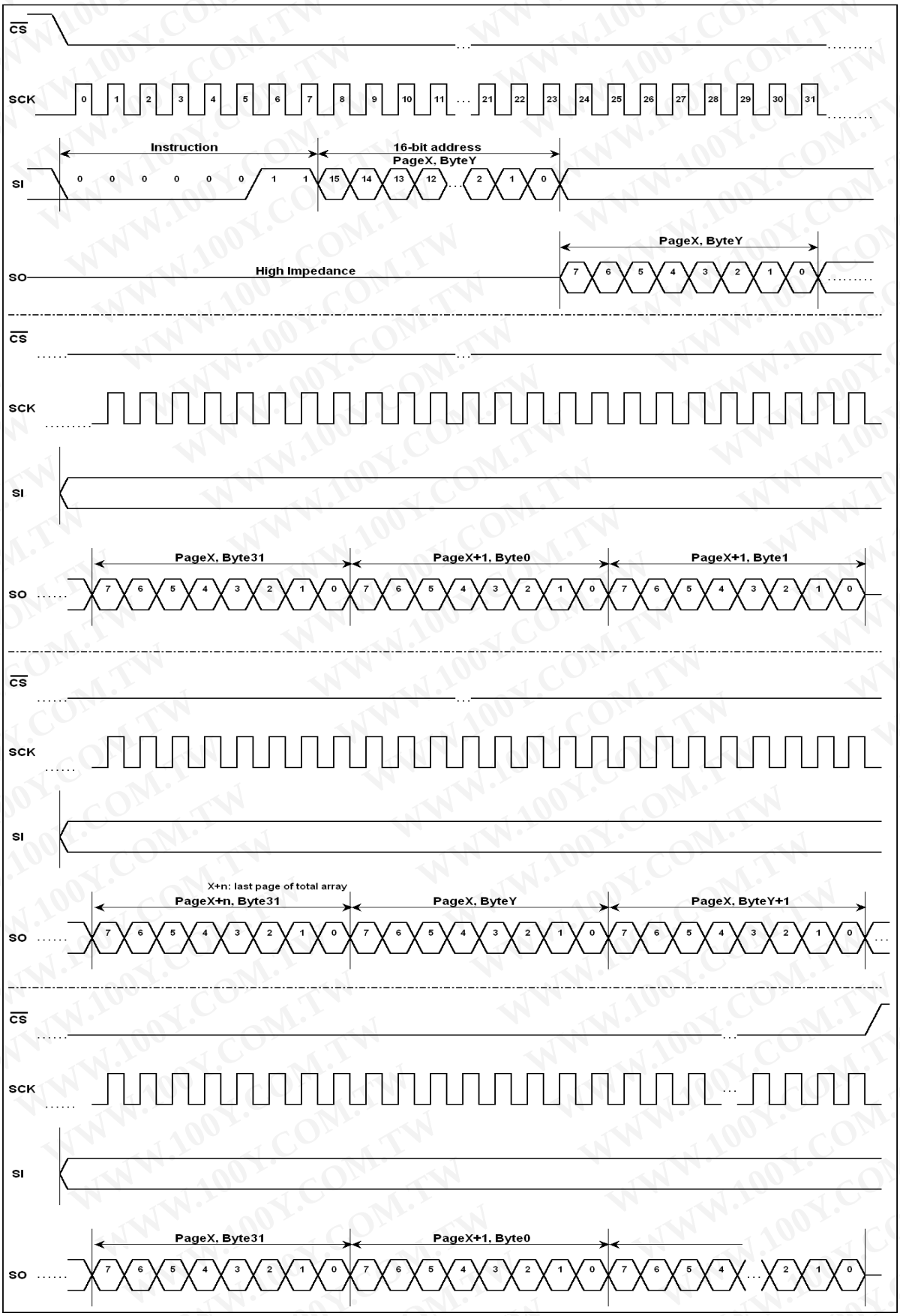
Page Read Sequence



Pagestart Sequential (PSEQ) Read Sequence



Virtual Chip (VRTM) Read Sequence



Write Operations

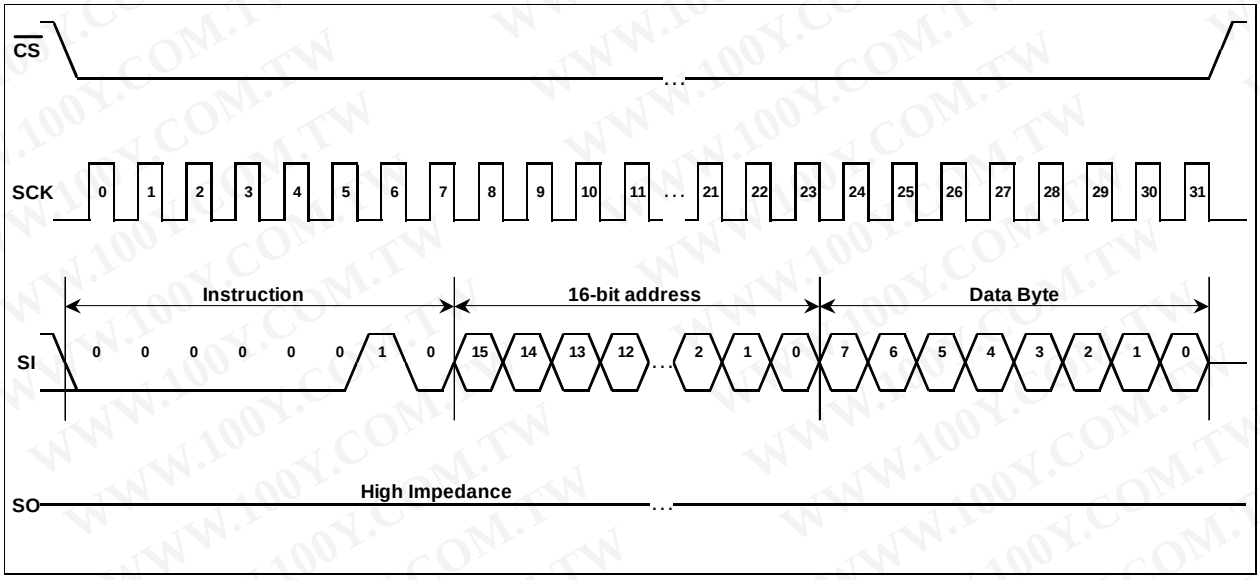
The serial SRAM WRITE is selected by enabling /CS low. First, the 8-bit WRITE instruction is transmitted to the device followed by the 16-bit address with the first bit as MSB. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial byte of data is shifted in, additional data bytes can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each byte of data is written in. This can be continued for the entire page length of 32 bytes long. At the end of the page, the addresses pointer will be wrapped to the 0 byte address within the page and the operation can be continuously looped over the 32 bytes of the same page. The new data will replace data already stored in the memory locations.

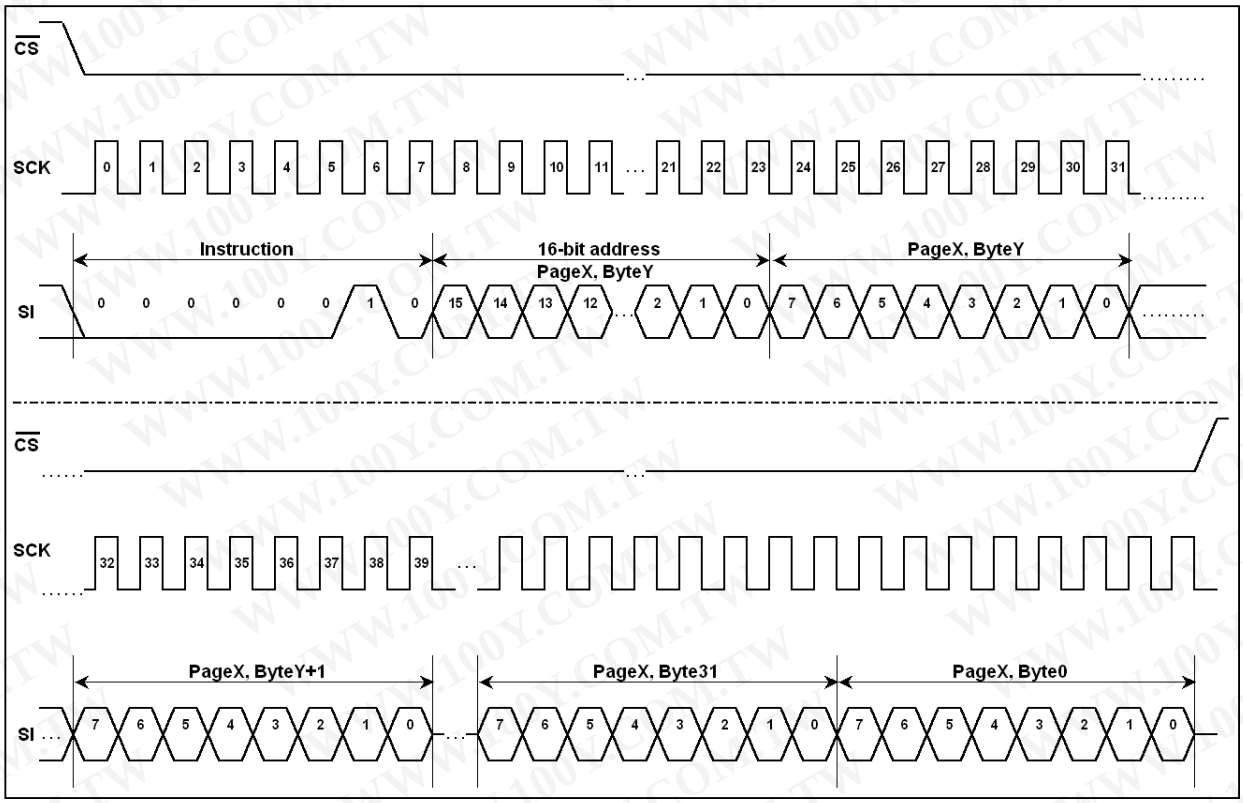
If operating in pagestart sequencial (PSEQ) mode, the operation is always starting at the address 00h of the selected page by default. After the initial byte of data is shifted in, additional data bytes can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is read out. This can be continued for the entire array and when the highest address is reached (FFFFh), the address counter wraps to the address 0000h. This allows the pagestart sequencial (PSEQ) write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

If operating in virtual chip (VRTM) mode, after the initial byte of data is shifted in, additional data bytes can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is read out. This can be continued for the entire array and when the highest address is reached (FFFFh), the address counter wraps to the address that was selected as the starting address of the virtual chip command. This allows the virtual chip write cycle to be continued indefinitely within the selected start-address and the highest address of the full array. Again, the new data will replace data already stored in the memory locations.
All WRITE operations are terminated by pulling /CS high.

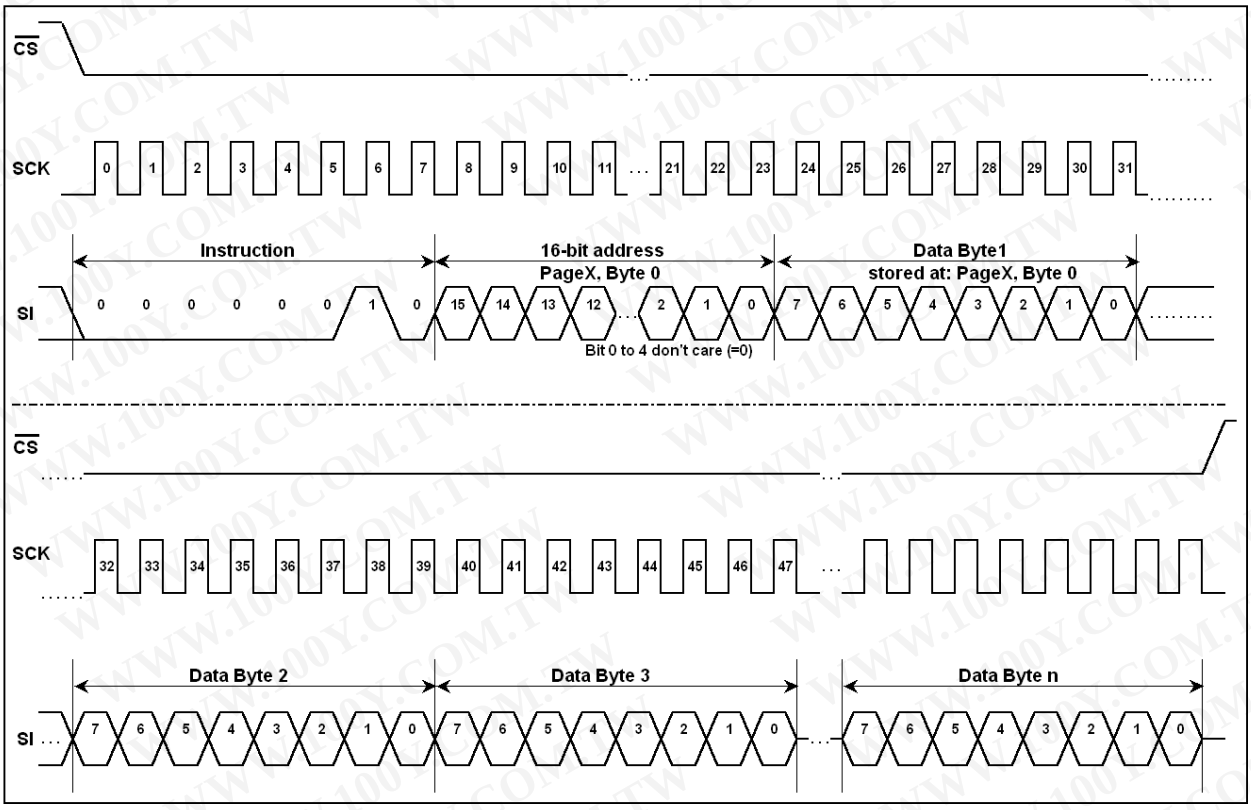
Byte Write Sequence



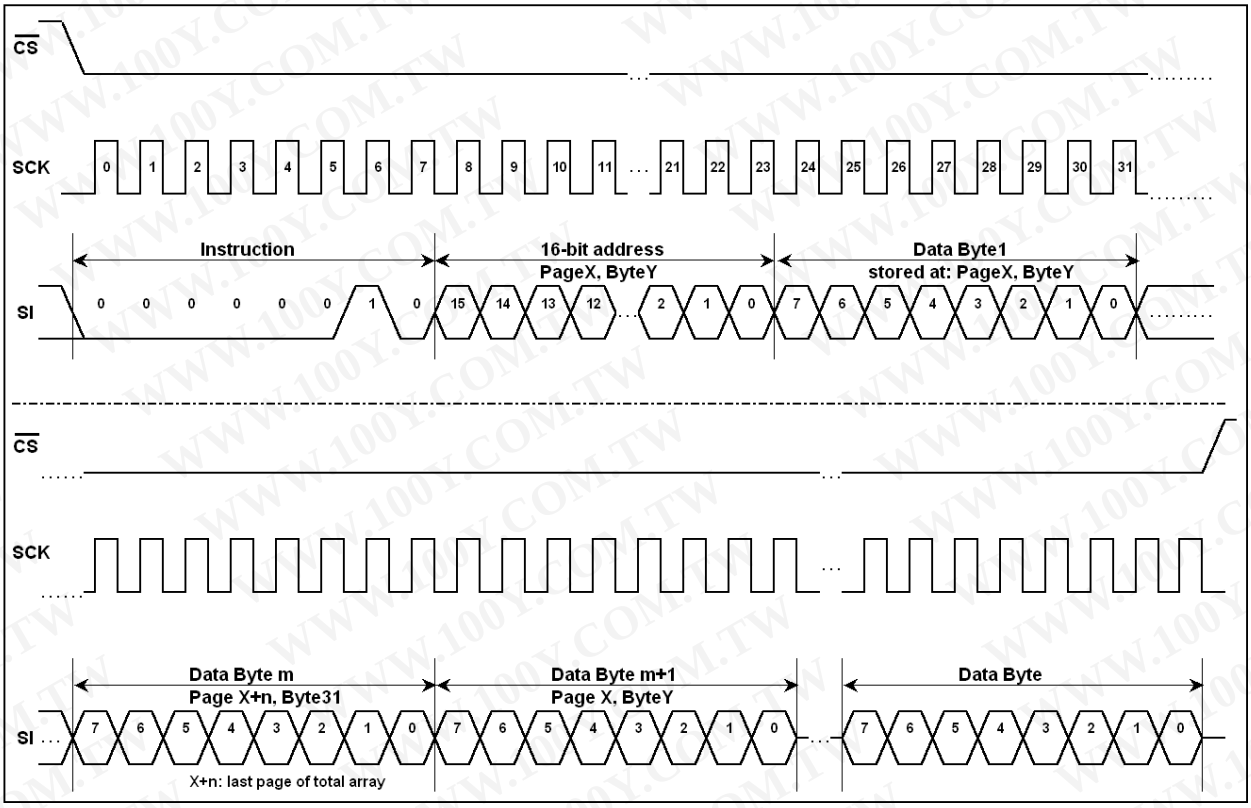
Page Write Sequence



Pagestart Sequencial (PSEQ) Write Sequence



Virtual chip (VRTM) Write Sequence



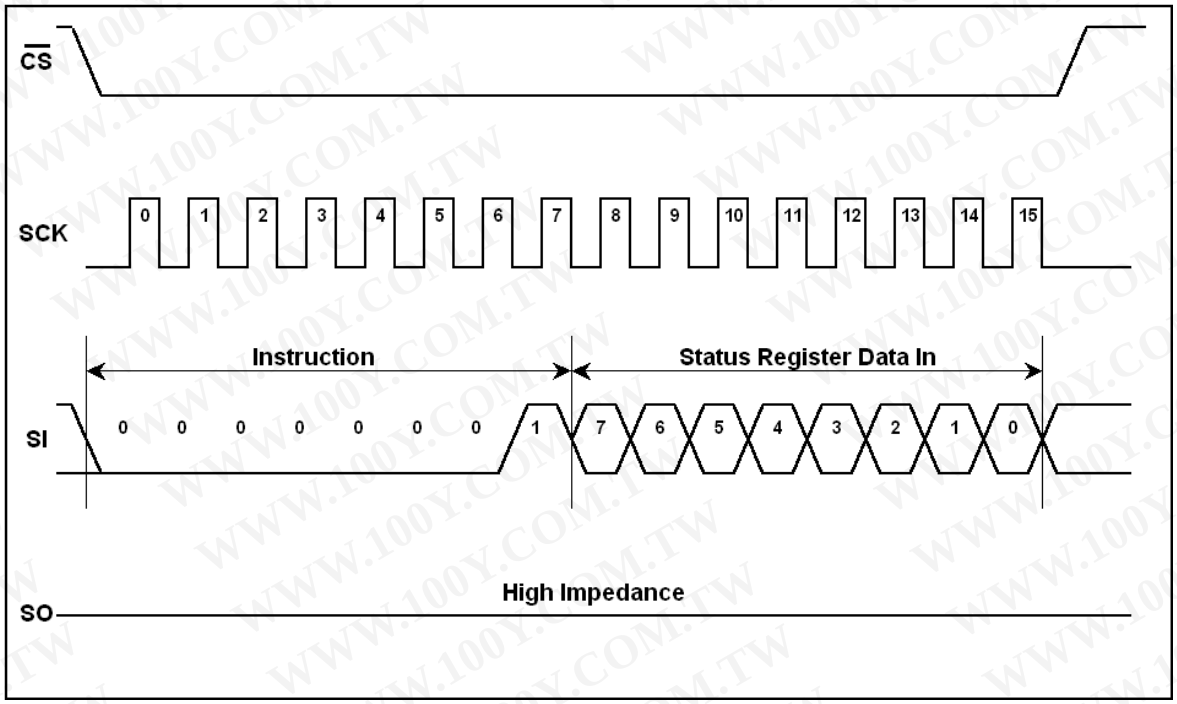
Status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
MODE		Reserved **0**	Reserved **0**	Reserved **0**	Reserved **0**	Reserved **0**	HOLD	
0	**0**	= Byte Mode (default)					**0**	= Hold (default)
0	**1**	= Virtual chip Mode (VRTM)					**1**	= No Hold
1	**0**	= Page Mode						
1	**1**	= Pagestart Sequencial (PSEQ) Mode						

WRITE Status Register Instruction (WRSR)

This instruction provides the ability to write the status register and select among several operating modes. Several of the register bits must be set to a low '0' if any of the other bits are written. The timing sequence to write to the status register is shown below, followed by the organization of the status register.

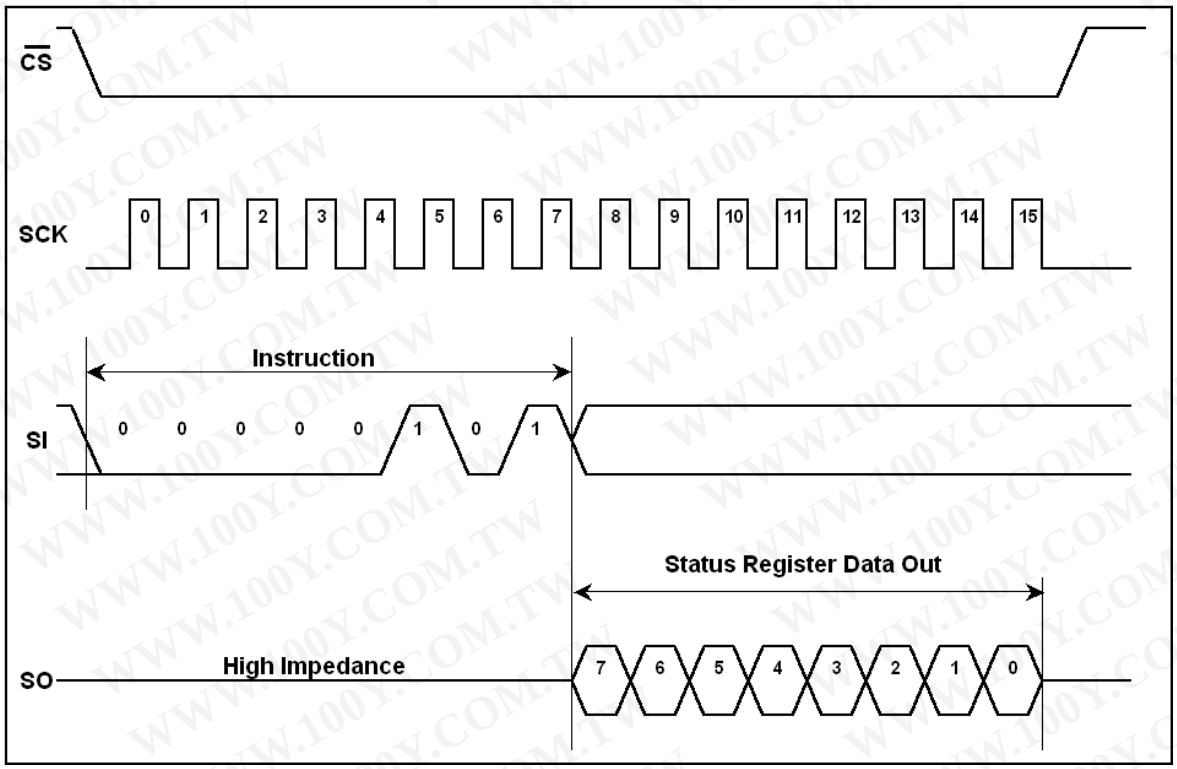
Write Status Register Sequence



READ Status Register Instruction (RDSR)

This instruction provides the ability to read the Status register. The register may be read at any time by performing the following timing sequence.

READ Status Register Sequence



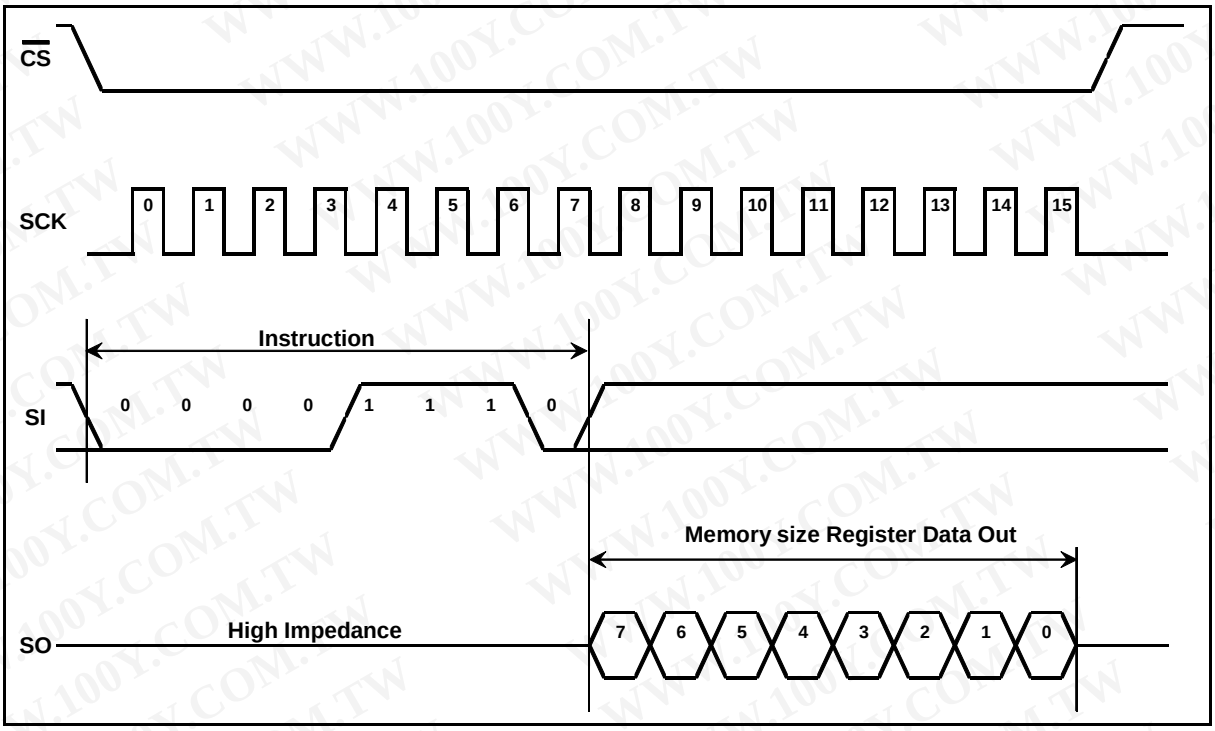
Memory size register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Reserved	Reserved	Reserved	Reserved	Memory size				
read	read	read	read	read	read	read	read	
				0	**0**	**0**	**0**	64Kbit
				0	**0**	**0**	**1**	128Kbit
				0	**0**	**1**	**0**	256Kbit
				0	**0**	**1**	**1**	512Kbit

READ Memory size Register Instruction (RDMI)

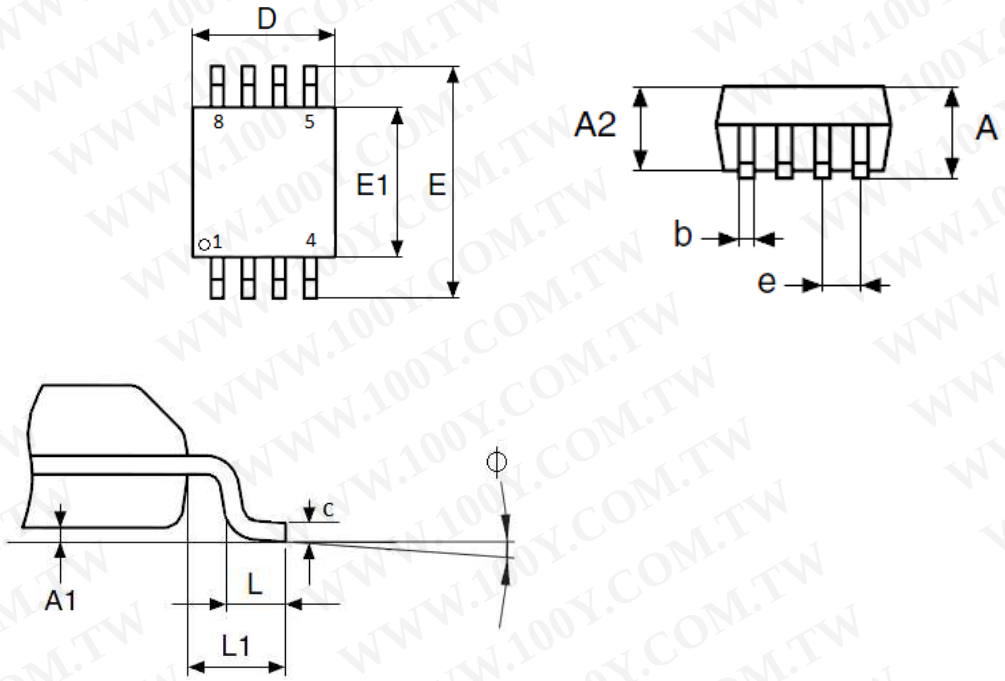
This instruction provides the ability to read the Memory size register. The register may be read at any time by performing the following timing sequence.

READ Memory size Register Sequence



Packaging information

8 – Lead Plastic Thin Shrink Small Outline – 4.4mm TSSOP



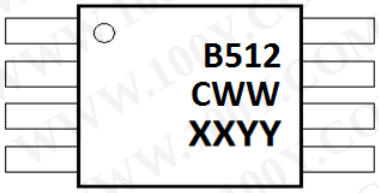
Parameter	Symbol	Min.	Nom.	Max.
Number of Pins	N		8	
Lead Pitch	e		0.65 BSC	
Overall hight	A	---	---	1.1
Molded Package Thickness	A2	0.85	---	0.95
Standoff	A1	0.05	---	0.15
Overall width	E	6.3	6.4	6.5
Molded Package Width	E1	4.3	4.4	4.5
Molded Package Length	D	2.9	3.0	3.1
Foot Lenght	L	0.5	0.6	0.7
Footprint	L1		1.0 REF	
Foot Angle	ϕ	0°	---	8°
Lead Thickness	c	0.13	---	0.18
Lead Width	b	0.19	---	0.25

Units: [mm]

BSC: Basic Dimension. Theoretically exact value without tolerances.
REF: Reference Dimension, usually without tolerance, for information purpose only.

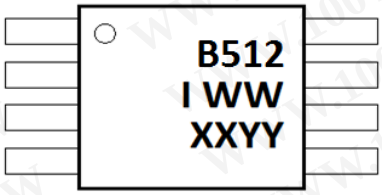
Package Marking Information

Example:



B: Vcc Range 2.7 - 3.6V
512: Memory Size 512Kbit
C: Temp Range -20℃ to +70℃
WW: Week code (week of Januar 1 is "01")
XX: Traceability code
YY: Year code (last two digits of calendar year)

Example:



B: Vcc Range 2.7 - 3.6V
512: Memory Size 512Kbit
I: Temp Range -40℃ to +85℃
WW: Week code (week of Januar 1 is "01")
XX: Traceability code
YY: Year code (last two digits of calendar year)

Ordering Information

Ordering Number	Vcc Range	Density	Temp. Ranges	Packages	Shipping Method
IP12B512C-TR	2.7 - 3.6V	512Kb	-20℃ to +70℃	TSSOP-8	Tape & Reel
IP12B512C-TU	2.7 - 3.6V	512Kb	-20℃ to +70℃	TSSOP-8	Tube
IP12B512I-TR	2.7 - 3.6V	512Kb	-40℃ to +85℃	TSSOP-8	Tape & Reel
IP12B512I-TU	2.7 - 3.6V	512Kb	-40℃ to +85℃	TSSOP-8	Tube

Revision History

Revision #	Date	Change description
1.0	March 2011	Initial productive release

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