

## Description

The μPD27C1024A is a 1,048,576-bit ultraviolet erasable and electrically programmable ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 65,536 words by 16 bits and operates from a single +5-volt power supply. All inputs and outputs are TTL-compatible.

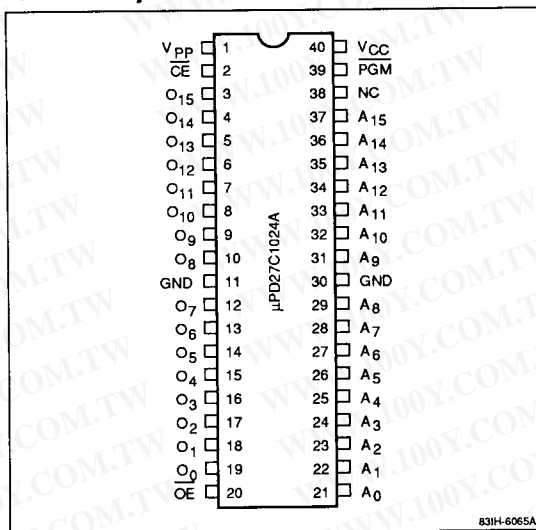
The μPD27C1024A is available in a 40-pin ceramic DIP with quartz window.

## Features

- 65,536 x 16-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed word and page programming
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- Advanced CMOS technology
- 40-pin cerdip packaging with quartz window

## Pin Configuration

### 40-Pin Cerdip



## Ordering Information

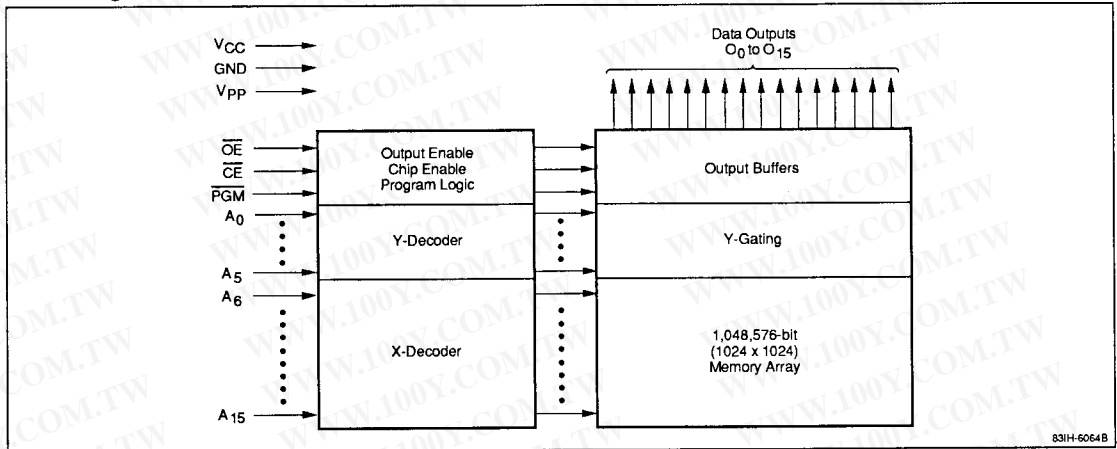
Part Number	Access Time (max)	Package
μPD27C1024AD-12	120 ns	40-pin cerdip with quartz window
D-15	150 ns	
D-20	200 ns	

## Pin Identification

Symbol	Function
A <sub>0</sub> - A <sub>15</sub>	Address inputs
O <sub>0</sub> - O <sub>15</sub>	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
PGM	Program
GND	Ground
V <sub>CC</sub>	+5-volt power supply
V <sub>PP</sub>	Program voltage
NC	No connection

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Block Diagram



Absolute Maximum Ratings

Operating temperature, T <sub>OPR</sub>	-10 to +80°C
Storage temperature, T <sub>STG</sub>	-65 to +125°C
Output voltage, V <sub>OUT</sub>	-0.6 to +7.0 V
Input voltage, V <sub>IN</sub>	-0.6 to V <sub>CC</sub> + 0.3 V
Input voltage, A <sub>9</sub>	-0.6 to +13.5 V
Supply voltage, V <sub>CC</sub>	-0.6 to +7.0 V
Supply voltage, V <sub>PP</sub>	-0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T<sub>A</sub> = 25°C; f = 1 MHz; V<sub>IN</sub> and V<sub>OUT</sub> = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C <sub>IN</sub>			14	pF
Output capacitance	C <sub>OUT</sub>			16	pF

Truth Table

Function	$\overline{CE}$	$\overline{OE}$	PGM	V <sub>PP</sub>	V <sub>CC</sub>	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	5.0 V	5.0 V	D <sub>OUT</sub>
Output disable	V <sub>IL</sub>	V <sub>IH</sub>	X	5.0 V	5.0 V	High-Z
Standby	V <sub>IH</sub>	X	X	5.0 V	5.0 V	High-Z
Page data latch	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	12.5 V	6.5 V	D <sub>IN</sub>
Page program	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	12.5 V	6.5 V	High-Z
Word program	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	12.5 V	6.5 V	D <sub>IN</sub>
Program verify	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	12.5 V	6.5 V	D <sub>OUT</sub>
Program inhibit	X	V <sub>IL</sub>	V <sub>IL</sub>	12.5 V	6.5 V	High-Z
	X	V <sub>IH</sub>	V <sub>IH</sub>			

Notes:

- (1) X = V<sub>IL</sub> or V<sub>IH</sub>.
- (2) In read operation,  $\overline{PGM}$  must be set to V<sub>IH</sub> at all times, or for at least 2 μs before  $\overline{OE}$  or  $\overline{CE}$  returns to V<sub>IH</sub>.

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
<b>Read Operation or Standby</b>					
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{PP}$	$V_{CC} - 0.6$	$V_{CC}$	$V_{CC} + 0.6$	V
Input voltage, high	$V_{IH}$	2.0		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	0		70	°C
<b>Programming Operation</b>					
Supply voltage	$V_{CC}$	6.25	6.5	6.75	V
	$V_{PP}$	12.2	12.5	12.8	V
Input voltage, high	$V_{IH}$	2.0		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	20	25	30	°C

### DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{ V} \pm 10\%$ ;  $V_{PP} = V_{CC} \pm 0.6\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Read Operation</b>						
Output voltage, high	$V_{OH1}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
	$V_{OH2}$	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu\text{A}$
Output voltage, low	$V_{OL}$			0.45	V	$I_{OL} = 2.1\ \text{mA}$
Output leakage current	$I_{LO}$	-10		10	$\mu\text{A}$	$V_{OUT} = 0$ to $V_{CC}$ ; $\overline{OE} = V_{IH}$
Input leakage current	$I_{LI}$	-10		10	$\mu\text{A}$	$V_{IN} = 0$ to $V_{CC}$
$V_{PP}$ current	$I_{PP}$		1	100	$\mu\text{A}$	$V_{PP} = V_{CC}$
$V_{CC}$ current (active)	$I_{CCA1}$			15	mA	$\overline{CE} = V_{IL}$ ; $V_{IN} = V_{IH}$
	$I_{CCA2}$			50	mA	$f = 8.4\ \text{MHz}$ ; $I_{OUT} = 0\ \text{mA}$
$V_{CC}$ current (standby)	$I_{CCS1}$			1	mA	$\overline{CE} = V_{IH}$ min
	$I_{CCS2}$		1	100	$\mu\text{A}$	$\overline{CE} \geq V_{CC} - 0.2\ \text{V}$ ; $V_{IN} = 0$ to $V_{CC}$

### DC Characteristics (cont)

$T_A = 25 \pm 5^\circ\text{C}$ ;  $V_{CC} = +6.5\text{ V} \pm 0.25$ ;  $V_{PP} = +12.5\text{ V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Programming Operation</b>						
Output voltage, high	$V_{OH}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
Output voltage, low	$V_{OL}$			0.45	V	$I_{OL} = 2.1\ \text{mA}$
Input leakage current	$I_{LI}$	-10		10	$\mu\text{A}$	$V_{IN} = 0$ to $V_{CC}$
$V_{PP}$ current	$I_{PP}$			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
$V_{CC}$ current	$I_{CC}$			30	mA	

**AC Characteristics**

$T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V} \pm 10\%; V_{PP} = V_{CC} \pm 0.6 \text{ V}$

Parameter	Symbol	μPD27C1024A-12		μPD27C1024A-15		μPD27C1024A-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
<b>Read Operation</b>									
Address to output delay	$t_{ACC}$		120		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	$t_{CE}$		120		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	$t_{OE}$		60		70		70	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	$t_{DF}$	0	50	0	55	0	55	ns	$\overline{CE} = V_{IL}$
Address to output hold	$t_{OH}$	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

**AC Characteristics (cont)**

$T_A = 25 \pm 5^\circ\text{C}; V_{CC} = +6.5 \text{ V} \pm 0.25; V_{PP} = +12.5 \text{ V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Page Programming Operation</b>						
Address setup time	$t_{AS}$	2			μs	
$\overline{CE}$ setup time	$t_{CES}$	2			μs	
Data setup time	$t_{DS}$	2			μs	
Address hold time	$t_{AH}$	2			μs	
	$t_{AHL}$	2			μs	
	$t_{AHV}$	0			μs	
Data hold time	$t_{DH}$	2			μs	
$\overline{OE}$ to output float time	$t_{DF}$	0		130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2			μs	
$V_{CC}$ setup time	$t_{VCS}$	2			μs	
Program pulse width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	$t_{OES}$	2			μs	
$\overline{OE}$ to output delay	$t_{OE}$			150	ns	
$\overline{OE}$ pulse width during data latch	$t_{LW}$	1			μs	
PGM setup time	$t_{PGMS}$	2			μs	
$\overline{CE}$ hold time	$t_{CEH}$	2			μs	
$\overline{OE}$ hold time	$t_{OEH}$	2			μs	

### AC Characteristics (cont)

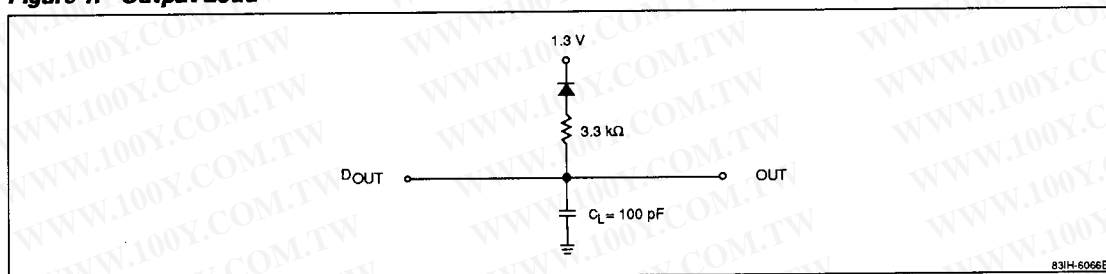
$T_A = 25 \pm 5^\circ\text{C}$ ;  $V_{CC} = +6.5\text{ V} \pm 0.25$ ;  $V_{PP} = +12.5\text{ V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Word Programming Operation</b>						
Address setup time	$t_{AS}$	2			$\mu\text{s}$	
$\overline{\text{OE}}$ setup time	$t_{OES}$	2			$\mu\text{s}$	
Data setup time	$t_{DS}$	2			$\mu\text{s}$	
Address hold time	$t_{AH}$	2			$\mu\text{s}$	
Data hold time	$t_{DH}$	2			$\mu\text{s}$	
$\overline{\text{OE}}$ to output float time	$t_{DF}$	0		130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2			$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2			$\mu\text{s}$	
Program pulse width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{\text{CE}}$ setup time	$t_{CES}$	2			$\mu\text{s}$	
$\overline{\text{OE}}$ to output delay	$t_{OE}$			150	ns	

#### Notes:

- (1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times  $\leq 20$  ns. See figure 1 for output load.

**Figure 1. Output Load**



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## PROGRAMMING

Before programming the μPD27C1024A, erase all data; this sets all data bits high. The μPD27C1024A is originally shipped in this condition. To begin programming, first raise  $V_{CC}$  to  $+6.5\text{ V} \pm 0.25$ , and then raise  $V_{PP}$  to  $12.5\text{ V} \pm 0.3$ . At this point, data to be programmed can be directly input in 16-bit format through the data bus. Programming causes relevant bits to go low.

### Word Programming

For word programming,  $\overline{CE}$  should be set low and  $\overline{OE}$  high to start programming at the initial address. A 0.1-ms pulse is applied to  $\overline{PGM}$ , as shown in the word programming portion of the timing waveforms, and  $\overline{OE}$  goes low to verify the 16 bits prior to making a program/no program decision. If the word is not programmed, another 0.1-ms pulse is applied to  $\overline{PGM}$ , up to a maximum of 10 times, before the next address is input. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both  $V_{CC}$  and  $V_{PP}$  to  $+5.0\text{ V} \pm 10\%$  and verify all data again.

### Page Programming

To begin page programming,  $\overline{CE}$  and  $\overline{PGM}$  should be set high and  $\overline{OE}$  pulsed low twice to latch the addressed two-word, one-page data.  $\overline{CE}$  and  $\overline{OE}$  subsequently go high and a 0.1-ms program pulse is applied to  $\overline{PGM}$ , as shown in the page programming portion of the timing waveforms. Immediately thereafter,  $\overline{CE}$  and  $\overline{OE}$  go low to verify the data prior to a program/no program decision being made. If the two words of page data are not programmed, another 0.1-ms pulse is applied to  $\overline{PGM}$ , up to a maximum of 10 times. If the page is not programmed in 10 tries, reject the device as a program failure.

### Program Inhibit

The program inhibit option can be used in either word or page operation to program one of multiple μPD27C1024A devices whose  $\overline{CE}$  pins are independent and  $\overline{OE}$ ,  $V_{PP}$ , and  $O_0$  through  $O_{15}$  pins are connected in parallel. For word programming,  $\overline{OE}$  must be high and  $\overline{CE}$  of the device to be programmed low. For page programming, both  $\overline{OE}$  and  $\overline{CE}$  must be high. Applying a low-level TTL pulse to  $\overline{PGM}$  of the device to be programmed and a high-level TTL pulse to the  $\overline{PGM}$  pins of the other devices enables the one device to be programmed while the others are inhibited.

### Program Verification

To verify that the device is correctly programmed, execute a normal read cycle with a high logic level applied to the  $\overline{PGM}$  pin and a low logic level applied to the  $\overline{CE}$  and  $\overline{OE}$  pins of the device to be verified. A high should be applied to the  $\overline{CE}$  or  $\overline{OE}$  pin of all other devices.

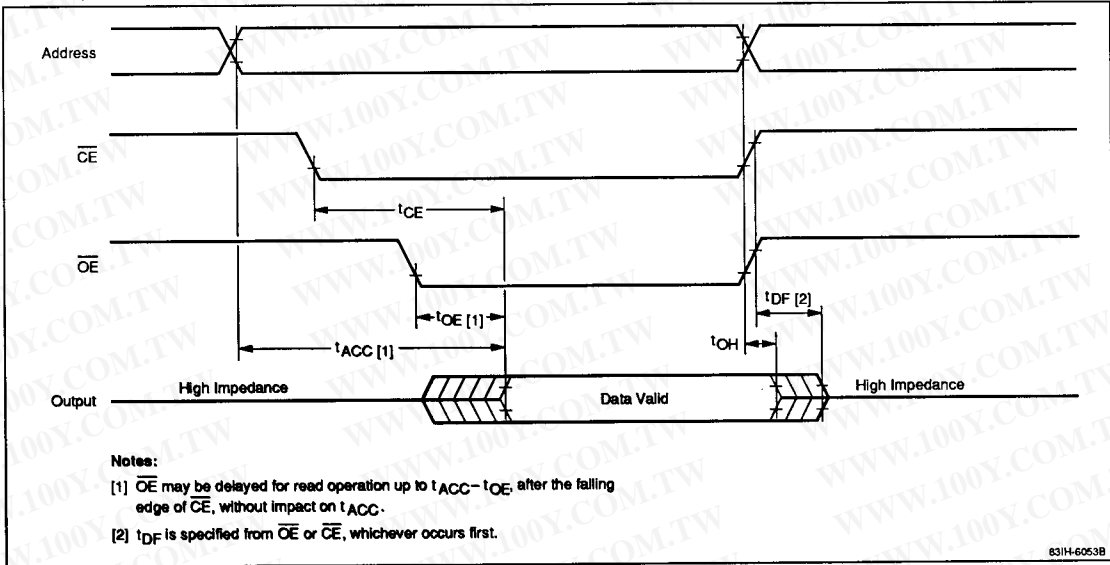
### Erase

Erase data on the μPD27C1024A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm<sup>2</sup> (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data. Using an ultraviolet lamp rated at 12,000 μW/cm<sup>2</sup>, it takes approximately 20 minutes to complete erasure. Place the μPD27C1024A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

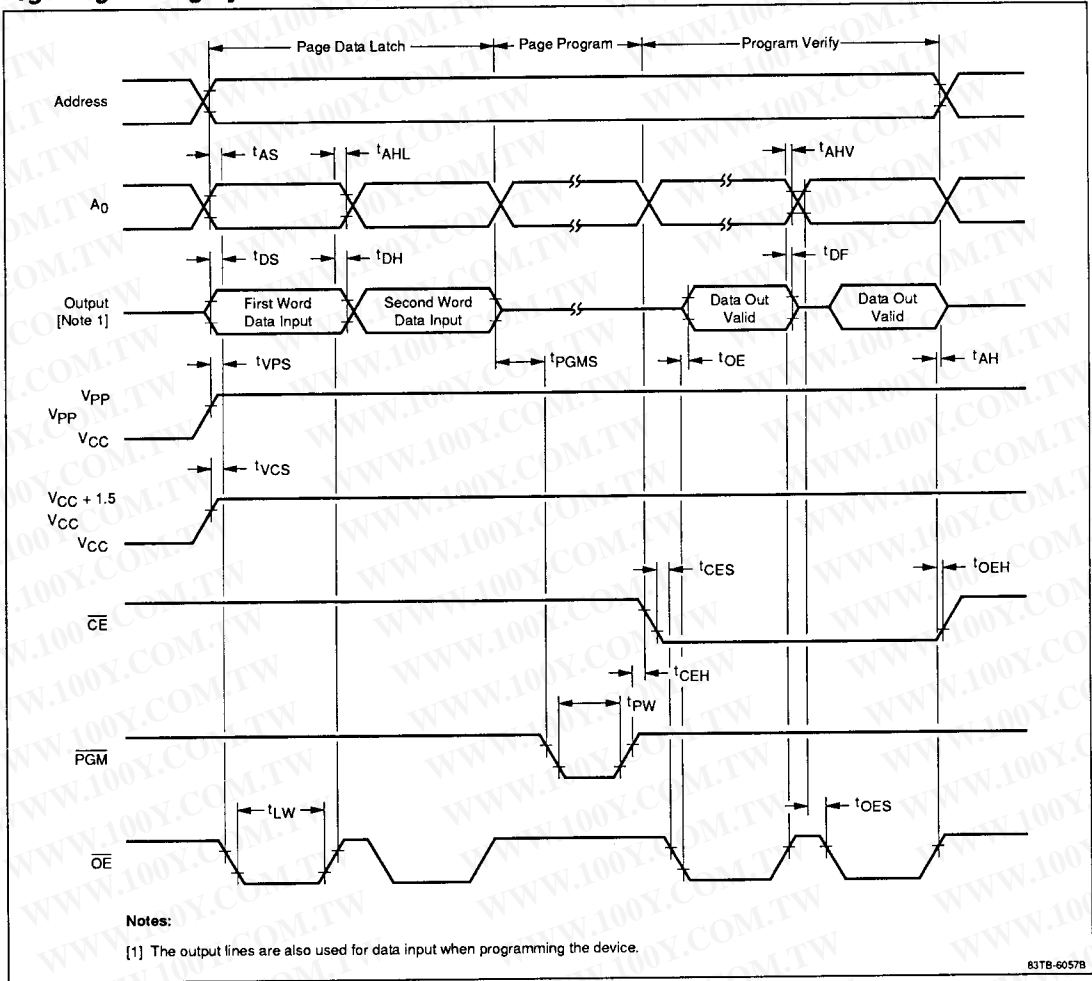
### Timing Waveforms

#### Read Cycle



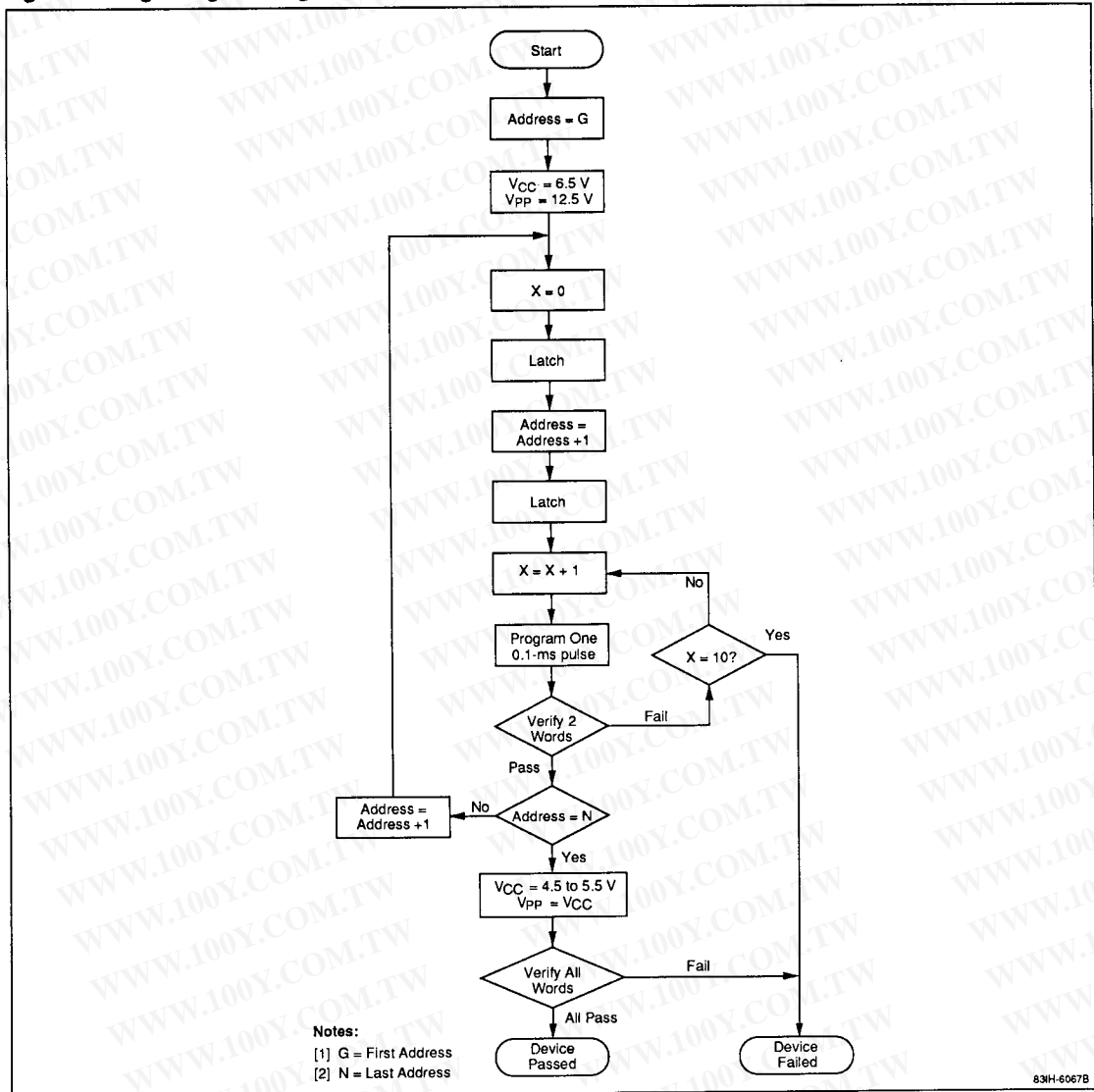
Timing Waveforms (cont)

Page Programming Cycle



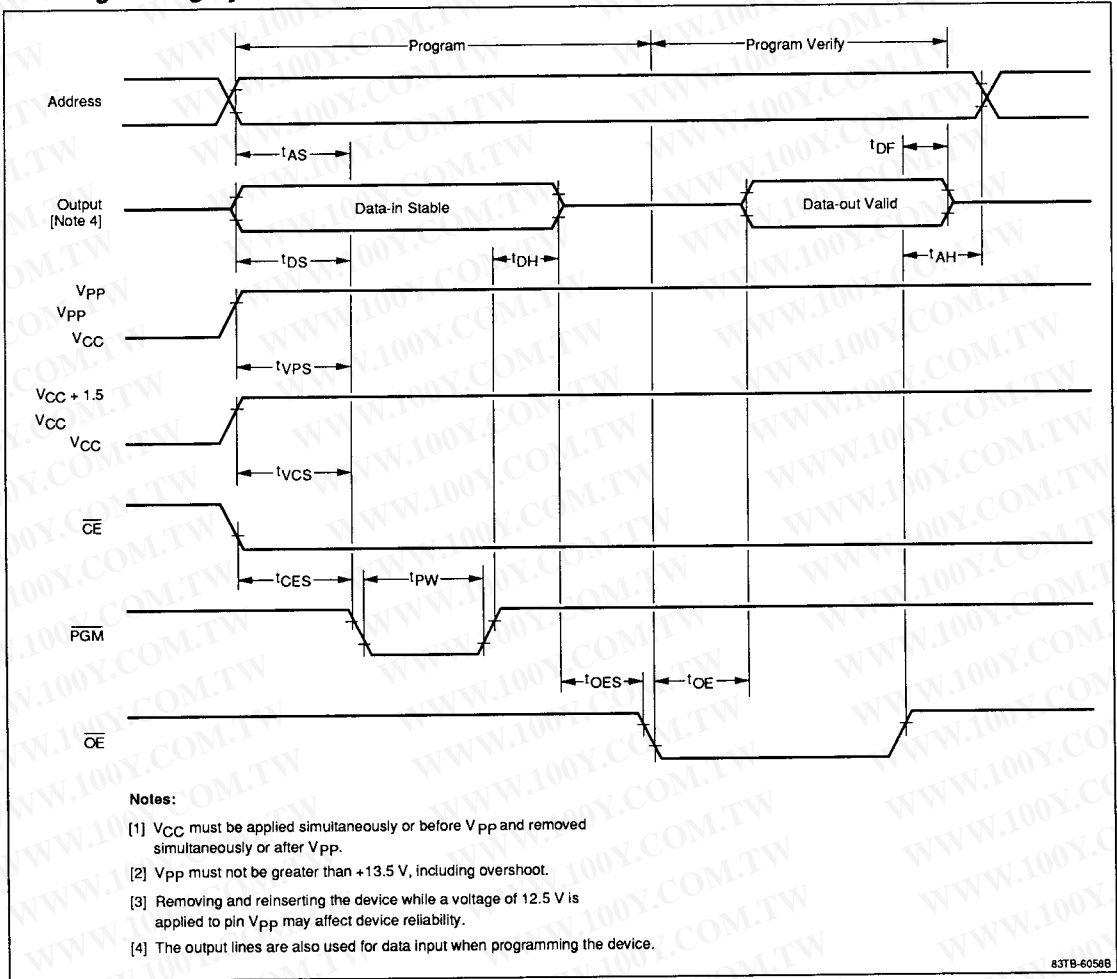


**Figure 2. Page Programming Flowchart**



Timing Waveforms (cont)

Word Programming Cycle

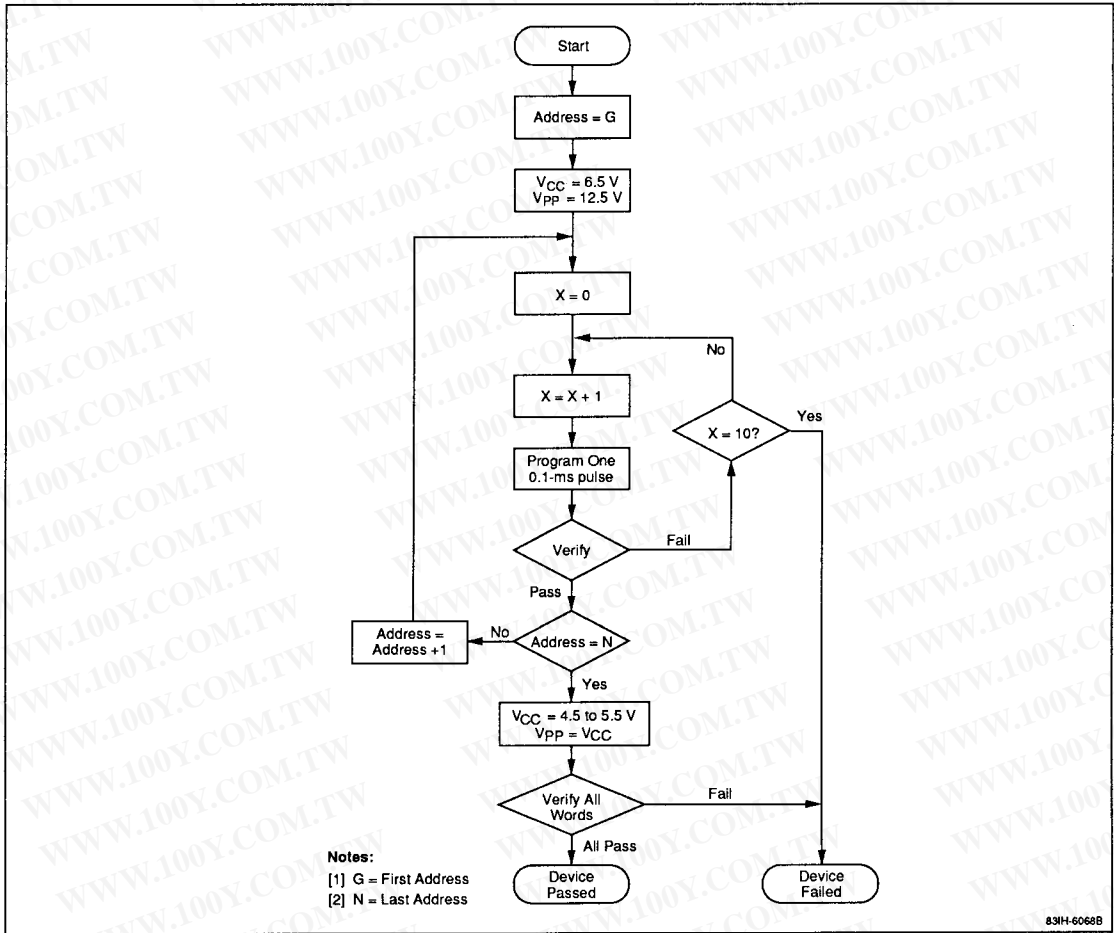


Notes:

- [1] VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.
- [2] VPP must not be greater than +13.5 V, including overshoot.
- [3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin VPP may affect device reliability.
- [4] The output lines are also used for data input when programming the device.

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**Figure 3 Word Programming Flowchart**



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