

# MOS INTEGRATED CIRCUIT $\mu PD43256B$

#### 256K-BIT CMOS STATIC RAM 32K-WORD BY 8-BIT

#### Description

The  $\mu$ PD43256B is a high speed, low power, and 262, 144 bits (32,768 words by 8 bits) CMOS static RAM. Battery backup is available (L, LL, A, and B versions). And A and B versions are wide voltage operations. The  $\mu$ PD43256B is packed in 28-pin plastic DIP, 28-pin plastic SOP and 28-pin plastic TSOP (I).

#### **Features**

- 32,768 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Wide voltage range (A version: Vcc = 3.0 to 5.5 V, B version: Vcc = 2.7 to 5.5 V)
- 2 V data retention
- OE input for easy application

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Standby supply current µA (MAX.)	Data retention supply current Note 1 $\mu$ A (MAX.)
μPD43256B-L	70, 85	4.5 to 5.5	0 to 70	50	C(3)
μPD43256B-LL	70, 85		COMIT	15	2
μPD43256B-A	85, 100 <sup>Note 2</sup> , 120 <sup>Note 2</sup>	3.0 to 5.5	Y.COM.TW	WWW	1001.COM.T.
μPD43256B-B <sup>Note 2</sup>	100, 120, 150	2.7 to 5.5	OY.COM.TW	W	100X.

Notes 1. TA  $\leq$  40 °C, Vcc = 3 V

2. Access time: 85 ns (MAX.) (Vcc = 4.5 to 5.5 V)

#### Version X and P

This data sheet can be applied to the version X and P. Each version is identified with its lot number. Letter X in the fifth character position in a lot number signifies version X, letter P, version P.



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The information in this document is subject to change without notice.

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# Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark	
μPD43256BCZ-70L	28-pin plastic	70	4.5 to 5.5	0 to 70	L Version	
μPD43256BCZ-85L	DIP (600 mil)	85	WWW.r	Y.CONT. TV		
μPD43256BCZ-70LL	WW.100	70	M.M.Yo	COM	LL Version	
μPD43256BCZ-85LL	1 100 x.	85	WWW.1	OM.I		
μPD43256BGU-70L	28-pin plastic	70		$100  { m y} \cdot { m COM}$	L Version	
μPD43256BGU-85L	SOP (450 mil)	85	MMM	100Y.COM	IW	
μPD43256BGU-70LL	WWW.	70	MM	1100 X.CO	LL Version	
μPD43256BGU-85LL	WWW.10	C 85	WW W	W. T. COD	WTD	
μPD43256BGU-A85	WW.1	85	3.0 to 5.5	AM:Inc CO	A Version	
μPD43256BGU-A10	W.	100		WW.100 T C	OW.	
μPD43256BGU-A12	M W	120	L. I	W.1001.	OM.TV	
μPD43256BGU-B10	MM	100	2.7 to 5.5	VW 100X.	B Version	
μPD43256BGU-B12	WW	120	WILL	WW 100Y	.Co. IV	
μPD43256BGU-B15	N WY	150	TW	WWW. 100	V.CO.	N
μPD43256BGW-70LL-9JL	28-pin plastic	70	4.5 to 5.5	MWW.100	LL Version	
$\mu$ PD43256BGW-85LL-9JL	TSOP (I)	85	OM:1	WW.10	COM	
μPD43256BGW-A85-9JL	(8 × 13.4 mm) (Normal bent)	85	3.0 to 5.5	L.W.	A Version	
μPD43256BGW-A10-9JL	(Normal Belli)	100	WT.MO	N. M.	100Y. COM.T	IN
μPD43256BGW-A12-9JL	WTT	120	I.CO. TW	MM	100Y.COM	
μPD43256BGW-B10-9JL	Mr.	100	2.7 to 5.5	MM	B Version	WT
μPD43256BGW-B12-9JL	OW.	120	ON COM	WW I	W. T. COM	
μPD43256BGW-B15-9JL	OMIT	150	In COW'I	ou atV	M. Tuo CO	W.I.
μPD43256BGW-70LL-9KL	28-pin plastic	70	4.5 to 5.5		LL Version	
$\mu$ PD43256BGW-85LL-9KL	TSOP (I)	85	100Y.	LM M	1,100 Y	
μPD43256BGW-A85-9KL	(8 × 13.4 mm) (Reverse bent)	85	3.0 to 5.5	TW	A Version	
μPD43256BGW-A10-9KL	(Novolog Bolle)	100	N. T. COM	WTD	MAMATIOOX	
μPD43256BGW-A12-9KL	COM.	120	W. In CO	TW	WWW.	
μPD43256BGW-B10-9KL	001. COW.1	100	2.7 to 5.5	W. T	B Version	
μPD43256BGW-B12-9KL	100X.COM.	120	WW.1001.	OW.T.	VV 100	
μPD43256BGW-B15-9KL	1100Y.COM	150	1007.0	WT.MO-	W TW.10	

MM.100X.CC

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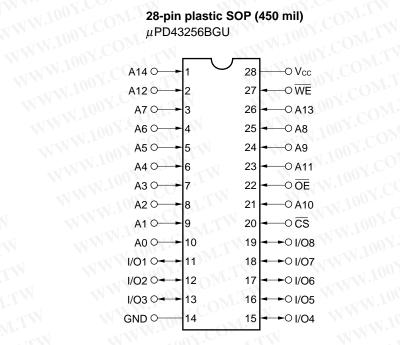
## Pin Configuration (Marking Side) WWW.100Y.C WWW.100Y.COM.TV

## VW.100Y.COM.TW 28-pin plastic DIP (600 mil) μPD43256BCZ

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WWW

#### 100Y.COM.TW 28-pin plastic SOP (450 mil) μPD43256BGU



A0 - A14 : Address inputs I/O1 - I/O8: Data inputs/outputs

CS : Chip Select WE : Write Enable OE : Output Enable Vcc : Power supply

**GND** : Ground

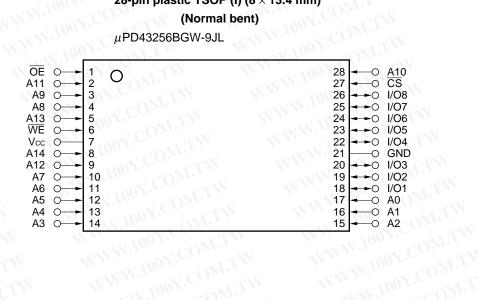
> 勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100v.com.tw

> > MMM.100X.COT



### W.100Y.COM.TW 28-pin plastic TSOP (I) $(8 \times 13.4 \text{ mm})$ (Normal bent)

μPD43256BGW-9JL



### 100Y.COM.TW 28-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)

WWW.100Y.COM.T

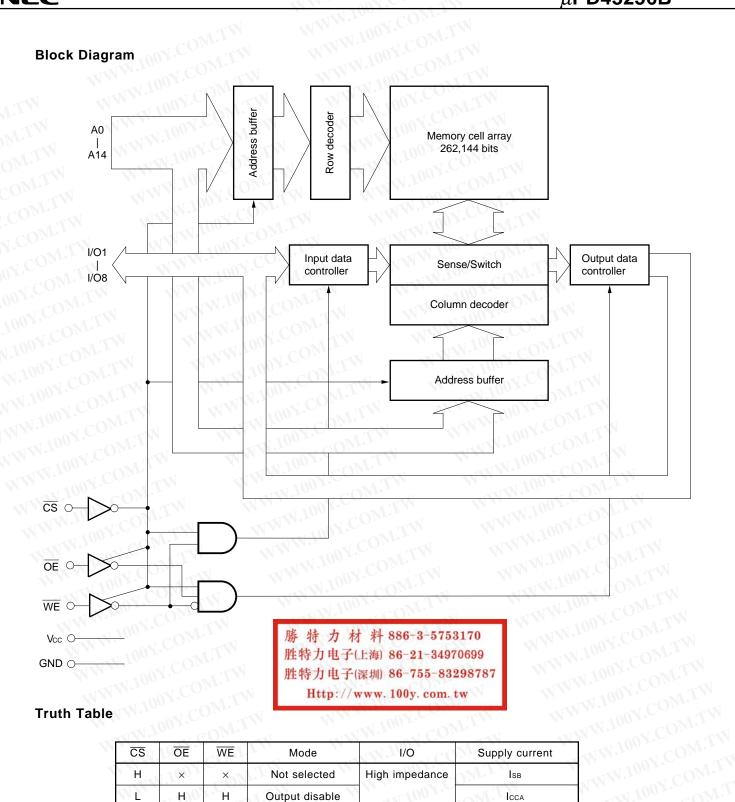
	MM. 100	μPD43256BGW-9KL	COM.TW _
	O 1 - O OE - O A11 - O A9 - O A8		A10 O = 28 CS O = 27 I/O8 O = 26 I/O7 O = 25
MM.TooX'COM.	5 - A13 6 - WE 7 - Vcc O 8 - A14	NWW.100	1/06 ○ → 24   1/05 ○ → 23   1/04 ○ → 22   GND ○ — 21
	9	WWW.I	I/O3 ○ → 20 I/O2 ○ → 19 I/O1 ○ → 18
	12 13 	WWW.	A0 O 17 A1 O 16 A2 O 15
<ul><li>A7</li><li>A6</li><li>A5</li><li>A4</li></ul>	10 11 12 13	MAMA:	1/O2 O 19 1/O1 O 18 A0 O 17 A1 O 16

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WWW

	ŌĒ	WE	Mode	1/0	Supply current
H	×	×	Not selected	High impedance	lsв
L	H00	Н	Output disable	W.1007.	Icca
L	×100	N.E	Write	Din	
LIVE	L	HC	Read	Dout	

Remark ×: Don't care WWW.100Y.COM.TW



# Electrical Characteristics

#### **Absolute Maximum Ratings**

Parameter	Symbol	Rating	Un
Supply voltage	Vcc	-0.5 <sup>Note</sup> to +7.0	V
Input/Output voltage	VT	-0.5 <sup>Note</sup> to Vcc + 0.5	V
Operating ambient temperature	TA	0 to 70	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

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Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **Recommended Operating Conditions**

Parameter	Symbol	μPD432 μPD432	256B-L 256B-LL	N μPD43	μPD43256B-A		256B-B	Unit
WWW. 100Y. CO. WITH	WWW	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	OM.T
Supply voltage	Vcc	4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	ViH	2.2	Vcc + 0.5	2.2	Vcc + 0.5	2.2	Vcc + 0.5	V
Low level input voltage	VIL	-0.3Note	+0.8	-0.3 <sup>Note</sup>	+0.5	-0.3Note	+0.5	V
Operating ambient temperature	TA	0	70	0	70	0	70	°C

-3.0 V (MIN.) (Pulse width 50 ns) WWW.1001 WWW.100Y.COM.

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#### DC Characteristics (Recommended operating conditions unless otherwise noted) (1/2)

WWW.

W. Too	COM	O.V.O. WWW. DOV.C	μΡΕ	43250	6B-L	μPD	43256	B-LL	
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Unit
Input leakage current	lu N	Vin = 0 V to Vcc	-1.0	17.	+1.0	-1.0		+1.0	μΑ
I/O leakage current	ILO	$V_{I/O} = 0 \text{ V to Vcc}$ $\overline{OE} = V_{IH} \text{ or } \overline{CS} = V_{IH} \text{ or } \overline{WE} = V_{IL}$	-1.0	$M_{i,j}$	+1.0	-1.0		+1.0	μΑ
Operating supply current	Icca1	CS = V <sub>I</sub> L, Minimum cycle time, I <sub>I/O</sub> = 0 mA	07.C		45	N		45	mA
	Icca2	CS = VIL, II/O = 0 mA	00	CO	10	N		10	
	Іссаз	$\label{eq:control_control_control} \begin{split} \overline{\text{CS}} &\leq 0.2 \text{ V, Cycle} = 1 \text{ MHz,} \\ I_{\text{I/O}} &= 0 \text{ mA} \\ V_{\text{IL}} &\leq 0.2 \text{ V, V}_{\text{IH}} \geq \text{Vcc} - 0.2 \text{ V} \end{split}$	1.100	Y.C.	10	TW	ĺ	10	
Standby supply current	Isa	CS = ViH	M.r.	M	3		N	3	mA
	I <sub>SB1</sub>	<u>CS</u> ≥ Vcc – 0.2 V	M.	1.0	50	Mr.	0.5	15	μΑ
High level output voltage	V <sub>OH1</sub>	Iон = −1.0 mA	2.4	Too	V.C	2.4	TW		V
	V <sub>OH2</sub>	Iон = −0.1 mA	Vcc-0.5	1.70		Vcc-0.5	. 1	Ŋ.	
Low level output voltage	Vol	IoL = 2.1 mA	A .	W.1	0.4	cO1	1.1	0.4	V

Remarks 1. Vin: Input voltage 2. These DC Characteristics are in common regardless of package types. WWW.100Y.COM.TW WWW.100Y.COM. WWW.100Y.COM.

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#### DC Characteristics (Recommended operating conditions unless otherwise noted) (2/2)

WWW.		OM		WWW	μΡΕ	4325	6B-A	√ μPΕ	)4325	6B-B	l
Parameter	Symbol	Test co	naitio	ons	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Un
Input leakage current	(1.11Li	VIN = 0 V to Vcc		WW.	-1.0	J C	+1.0	-1.0		+1.0	μΑ
I/O leakage current	lLO	$\frac{V_{I/O} = 0 \text{ V to } V_{CC}}{CS} = V_{IH} \text{ or } \overline{WE} = 0$	= VIL	or OE = VIH	-1.0	oy.C	+1.0	-1.0		+1.0	μΑ
Operating supply current	Icca1	$\overline{CS} = V_{IL},$ Minimum cycle time $I_{I/O} = 0 \text{ mA}$	, μΡ[	D43256B-A85 D43256B-A10 D43256B-A12	W.I	1007 1007	45	M.T.	N	_	m/
	MMM		, μΡ[	D43256B-B10 D43256B-B12 D43256B-B15	VWV	N.100	07.C		1.TV	45	
	N. A.		I.I	Vcc ≤ 3.3 V	~1	W.	00 >	7 CO	M.	20	
	Icca2	CS = VIL, II/O = 0	mA	1.44	11		10	-7 C!	M.	10	
	W		Vcc ≤ 3.3			-111	N. 401	100X 00X:	CON	5	l T
	Іссаз	$\overline{\text{CS}} \le 0.2 \text{ V, Cycle} = 1000 \text{ M}, \text{V}_{\text{IL}} \le 0.2 \text{ V}$				WW	10			10	N
	V	$V_{IH} \ge V_{CC} - 0.2 V$		Vcc ≤ 3.3 V		W	$N\overline{A_0}$ .	400	Y.C	5	CV
Standby supply current	Isв	CS = VIH	v.C	ON			3	.10	V.C	3	m/
				Vcc ≤ 3.3 V		,	W	W. In		2	L. I
	I <sub>SB1</sub>	<u>CS</u> ≥ Vcc - 0.2 V	O F	COMIT	N	0.5	15	2.4	0.5	15	μΑ
				Vcc ≤ 3.3 V						10	M
High level output voltage	V <sub>OH1</sub>	Iон = −1.0 mA, Vo	cc ≥ 4	4.5 V	2.4		111			-1 C	V
	WIN	Iон = −0.5 mA, Vo	cc < 4	4.5 V	2.4			2.4	N.19	01.	~0
	V <sub>OH2</sub>	Iон = −0.1 mA	-31 1	1001.00	LŦV			MA	TXX .1	001	
	OM	Iон = -0.02 mA	111-	100 A . Co.	Vcc-0.1	N		Vcc-0.1	1 4 1	1007	
Low level output voltage	VoL	IoL = 2.1 mA, Vcc	≥ 4.	5 V	) IV	W	0.4	W	My,	0.4	V
	COM	IoL = 1.0 mA, Vcc	< 4.	5 V	OM	TV	0.4		VIV	0.4	OY
	V <sub>OL1</sub>	IoL = 0.02 mA	~TV	W.In			<b>(</b> 0.1		WIN	0.1	

Remarks 1. VIN: Input voltage

2. These DC characteristics are in common regardless of package types.

#### Capacitance (TA = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit	1.100 × C
Input capacitance	Cin	Vin = 0 V	J	$M_{JJ,A}$	5	pF	W.100 1.
Input/Output capacitance	C <sub>I/O</sub>	$V_{I/O} = 0 V$			•	pF	1007.

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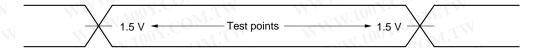
#### AC Characteristics (Recommended operating conditions unless otherwise noted)

#### **AC Test Conditions**

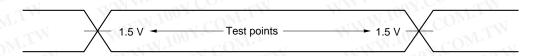
#### Input waveform (Rise/fall time $\leq 5$ ns)

Input pulse levels

0.8 V to 2.2 V: μPD43256B-L, 43256B-LL 0.5 V to 2.2 V: μPD43256B-A, 43256B-B



#### **Output waveform**

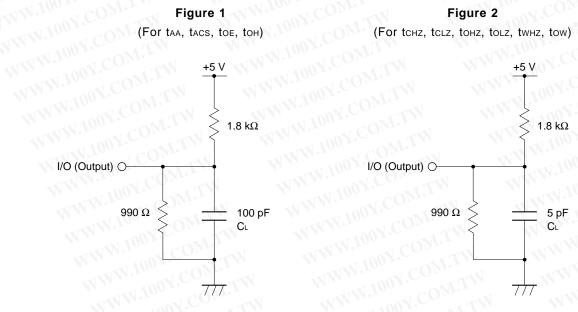


# WWW.100Y.CO

Output load  $\mu$ PD43256B-A, 43256B-B: 1TTL + 100 pF μPD43256B-L, 43256B-LL:

Figure 1 and Figure 2. AC characteristics with notes should be measured with the output load shown in

Figure 2 (For tchz, tclz, tohz, tolz, twhz, tow)



 $\textbf{Remark} \quad \textbf{C} \textbf{$\text{L}$ includes capacitances of the probe and jig, and stray capacitances.}$ 

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#### ★ Read Cycle (1/2)

MWW.Inc	CON	Vcc ≥ 4.5 V						
Parameter	Symbol	μPD432	256B-70	μPD43256B-85 μPD43256B-A85/A10/A12 μPD43256B-B10/B12/B15			Condition	
M. TW WWW	TOOK C	MIN.	MAX.	MIN.	MAX.			
Read cycle time	trc	70	I W	85	COM	ns		
Address access time	taa	COM	70	WWW	85	ns	Note 1	
CS access time	tacs	A COM.	70	MM.In	85	ns		
OE access time	toe	COM.	35	M.In.	40	ns		
Output hold from address change	tон	10	TV	10	COM.	ns	]	
CS to output in low impedance	tcLz	10	LTW	10	OO TOM	ns	Note 2	
OE to output in low impedance	tolz	1005	MIM	5	1007.	ns	1	
CS to output in high impedance	tснz	1 100 Y.C.	30	MA	30	ns	N	
OE to output in high impedance	tонz	M. TOON.C	30	MM.	30	ns	TW	

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- **Notes 1.** See the output load shown in **Figure 1** except for  $\mu$ PD43256B-A, 43256B-B.
  - 2. See the output load shown in **Figure 2** except for  $\mu$ PD43256B-A, 43256B-B.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

#### ★ Read Cycle (2/2)

	171-	W		Vcc ≥	3.0 V		Y.C.			Vcc ≥	2.7 V			X.C	
Parameter	Symbol	μPD432	56B-A85	μPD432	56B-A10	μPD432	256B-A12	μPD432	56B-B10	μPD432	56B-B12	μPD432	56B-B15	Unit	Con- dition
M.100 x	$CO_{M}$	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	03	dition
Read cycle time	trc	85		100		120	00-	100	1.1	120		150	11.1	ns	v.C
Address access time	taa	M.	85		100	NW	120	of CC	100	-XXI	120	- 1	150	ns	Note
CS access time	tacs	Mo	85		100	- XIV	120	7. C	100	LA	120		150	ns	0 1.
OE access time	toe		50		60	- 41	60	D.A.	60	TA	60		70	ns	003
Output hold from address change	toн	10	T.N	10		10	7XI.1	10		10	N	10	MA	ns	100
CS to output in low impedance	tcLz	10	MI	10		10	N N N	10		10	N	10	11/1	ns	u 10
OE to output in low impedance	toLz	5	) L	5		5	MA	5	Y.C.	5	IN	5	W	ns	XI 1
CS to output in high impedance	tснz	oy.C	35	TV	35		40	-110	35	OF	40		50	ns	- XI
OE to output in high impedance	tонz	01	35		35		40	M.	35	$C_{O_{D_{A}}}$	40	V	50	ns	M

Remark These AC characteristics are in common regardless of package types and L, LL versions. WW.100Y.COM.TW

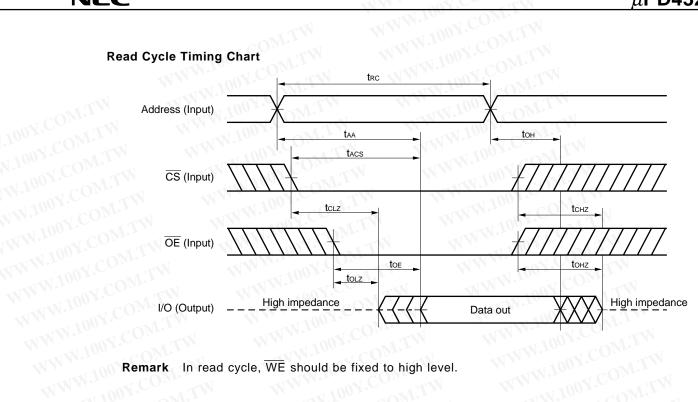
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WWW.100Y.C



#### Read Cycle Timing Chart



WW.100Y.C

WWW.

COM.TW

Remark In read cycle, WE should be fixed to high level. WWW.100Y.CC WWW.100Y.COM.TW WWW.100Y.COM.TW

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#### ★ Write Cycle (1/2)

W.100	=1 CO	Vcc ≥ 4.5 V						
Parameter	Symbol	μPD432	256B-70	μPD43256B-85 μPD43256B-A8 μPD43256B-B1	5/A10/A12	Unit	Condition	
	TOOX	MIN.	MAX.	MIN.	MAX.			
Write cycle time	twc	70	W	85	TW	ns		
CS to end of write	tcw	50	N V	70	COM	ns		
Address valid to end of write	taw	50		70	V.COM.	ns		
Write pulse width	twp	55		60	COM.	ns		
Data valid to end of write	tow	30	TA	35	COM.	ns		
Data hold time	tон	100 0	1.17	0	OON.	ns		
Address setup time	tas	1000	MIN	0	1007	ns	-1	
Write recovery time	twR	100 7.0	MILMO	0	1.1007.00	ns	N	
WE to output in high impedance	twnz	1,100 X.C	30	MW	30	ns	Note	
Output active from end of write	tow	10	COBL	10	A. JOUL'S	ns	WT	

**Note** See the output load shown in **Figure 2** except for  $\mu$ PD43256B-A, 43256B-B.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

#### ★ Write Cycle (2/2)

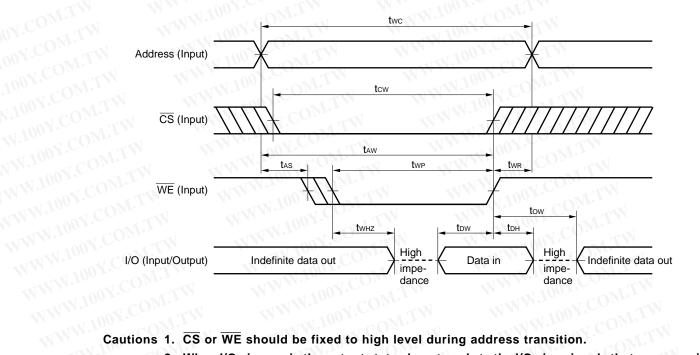
M.M. 100 J.C.	11	L.M.		Vcc ≥	3.0 V	1 100	1.0	M	LA	Vcc ≥	2.7 V	-11/	100	7.	-01
Parameter	Symbol	μPD432	56B-A85	μPD432	56B-A10	μPD432	256B-A12	μPD432	56B-B10	μPD432	56B-B12	μPD432	56B-B15	Unit	Con- dition
	$CO_{N}$	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	005	uition
Write cycle time	twc	85		100	WV	120	Voo.	100	. T.	120		150	M	ns	Y.C
CS to end of write	tcw	70	- N	70	***	90	Ino	70	Mr.	90		100	MW.	ns	NY.
Address valid to end of write	taw	70	1	70		90	1.700	70	OM.	90		100	WW	ns	001
Write pulse width	twp	60	r.r.	60		80	W.10	60	CON	80	ß.	90	TIN'	ns	no.
Data valid to end of write	tow	60	VI.T	60		70	W.1	60	col	70	- «T	80	W Y Y	ns	100
Data hold time	tон	0	W.T	0		0	TIN.	0		0	N	0	M	ns	V.10
Address setup time	tas	0	M	0		0		0	N.C	0	CM	0		ns	W.1
Write recovery time	twr	0	O.	0		0	M.	0	21.0	0	TW	0		ns	TXN
WE to output in high impedance	twnz	OOY	30		35		40	-11	35		40		50	ns	Note
Output active from end of write	tow	10	CO	10	W	10		10	.005	10		10		ns	W

Remark These AC characteristics are in common regardless of package types and L, LL versions. NW.100Y.COM.TW

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#### Write Cycle Timing Chart 1 (WE Controlled)

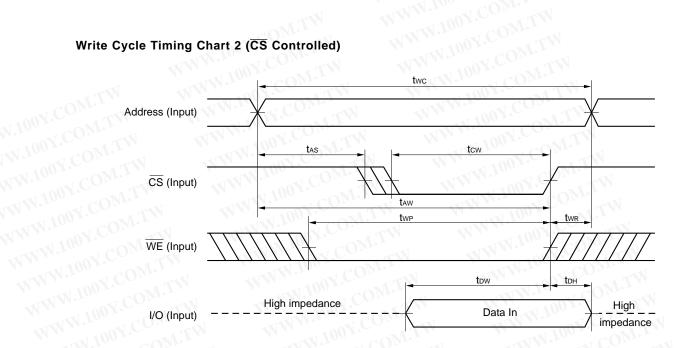


- Cautions 1. CS or WE should be fixed to high level during address transition.
  - 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.
- Write operation is done during the overlap time of a low level  $\overline{\text{CS}}$  and a low level  $\overline{\text{WE}}$ . Remarks 1.
- 2. When WE is at low level, the I/O pins are always high impedance. When WE is at high level, read operation is executed. Therefore  $\overline{OE}$  should be at high level to make the I/O pins high WWW.100 impedance.
  - 3. If  $\overline{\text{CS}}$  changes to low level at the same time or after the change of  $\overline{\text{WE}}$  to low level, the I/O pins will remain high impedance state ودی نامه iow level at the sa will remain high impedance state. WWW.100Y.COM

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#### Write Cycle Timing Chart 2 (CS Controlled)



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WWW

- WWW. Cautions 1. CS or WE should be fixed to high level during address transition.
  - 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level  $\overline{\text{CS}}$  and a low level  $\overline{\text{WE}}$ . WWW.100Y.COM.TW

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# Low Vcc Data Retention Characteristics

# WWW.100Y.COM.TW L Version ( $\mu$ PD43256B-L: T<sub>A</sub> = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	
Data retention supply voltage	Vccdr	<u>CS</u> ≥ Vcc – 0.2 V	2.0	Y	
Data retention supply current	Iccdr	Vcc = 3.0 V, <del>CS</del> ≥ Vcc - 0.2 V	TIMO	0.5	2
Chip deselection to data retention mode	tcdr	OW.TW WWW.100X;	COM		
Operation recovery time	tR	COM.	5		

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WWW.100Y. LL Version ( $\mu$ PD43256B-LL: T<sub>A</sub> = 0 to 70 °C) B Version (μPD43256B-B: T<sub>A</sub> = 0 to 70 °C) A Version ( $\mu$ PD43256B-A: T<sub>A</sub> = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	ι
Data retention supply voltage	Vccdr	<u>CS</u> ≥ Vcc − 0.2 V	2.0	OY.CU	5.5	
Data retention supply current	Iccdr	Vcc = 3.0 V, <del>CS</del> ≥ Vcc - 0.2 V	NN.	0.5	7Note	N
Chip deselection to data retention mode	tcdr	WW.100X.COM.TW	0	100X.C	$c_{\mathrm{OM},\mathrm{I}}$	W
Operation recovery time	tR	1100 . W.TW	5	17007	Mos	1

**Note** 2  $\mu$ A (TA  $\leq$  40 °C), 1  $\mu$ A (TA  $\leq$  25 °C) WWW.100Y.COM.TW WWW.100Y.COM.7 WWW.1003

WWW.100Y.COM:TV

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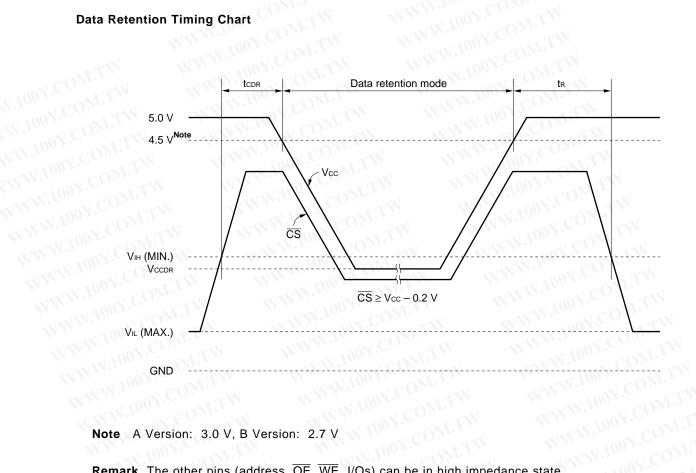
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# Data Retention Timing Chart



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WWW.

WWW.100Y.COM.

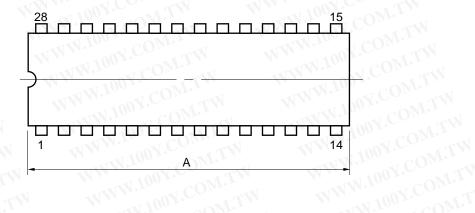
W.100Y.COM.TW WWW.100Y.COM.TW  $\textbf{Remark} \ \ \text{The other pins (address, } \overline{\text{OE}}, \overline{\text{WE}}, \text{ I/Os) can be in high impedance state}.$ WWW.100Y.CO WWW.100Y.C WWW.100Y.COM.TW

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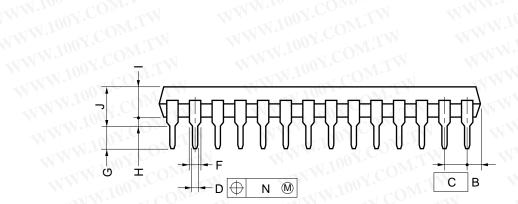
## Package Drawings

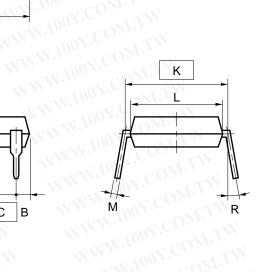
#### 28 PIN PLASTIC DIP (600 mil)



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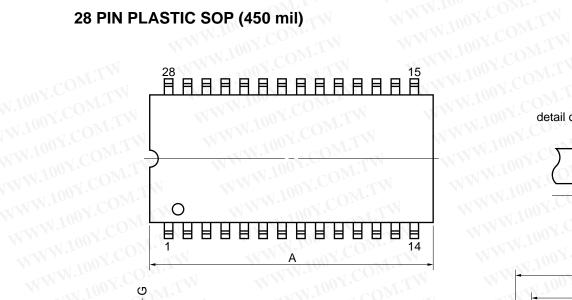
#### **NOTES**

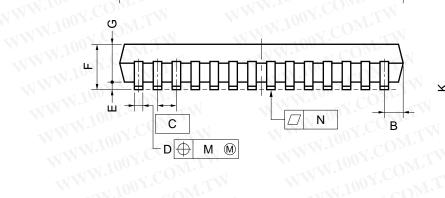
- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

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	EM <	MILLIMETERS	INCHES
V. 1.	Α	38.10 MAX.	1.500 MAX.
~ A L L	В	2.54 MAX.	0.100 MAX.
MI.	С	2.54 (T.P.)	0.100 (T.P.)
OW.T.	D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
TIMO	F	1.2 MIN.	0.047 MIN.
CON	G	3.6±0.3	0.142±0.012
COM	H	0.51 MIN.	0.020 MIN.
T	1	4.31 MAX.	0.170 MAX.
"COM"	J	5.72 MAX.	0.226 MAX.
I.M.	K	15.24 (T.P.)	0.600 (T.P.)
V.CO	L	13.2	0.520
COM.	М	0.25+0.10	0.010+0.004
ON	N	0.25	0.01
1007.0	R	0 ~ 15°	0 ~ 15°
100 -1 CO	Mr.	P	28C-100-600A1-1

#### 28 PIN PLASTIC SOP (450 mil)

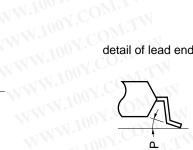


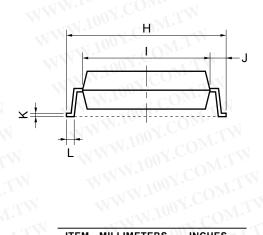


## WW.100Y.COM.TW detail of lead end WWW.100Y.C

WWW.100Y.CO

WWW.100Y.COM.TW





#### NOTE

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Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material activities. WWW.100Y.COM.TW its true position (T.P.) at maximum material condition.

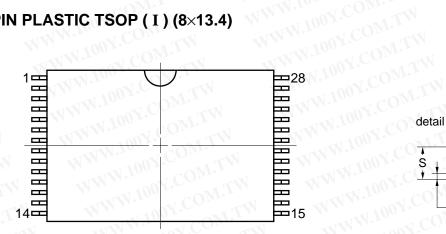
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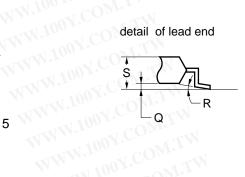
	ITEM	MILLIMETERS	INCHES	
0.005 inch) of	M A	19.05 MAX.	0.750 MAX.	
dition.	В	1.27 MAX.	0.050 MAX.	
	C	1.27 (T.P.)	0.050 (T.P.)	
	D	0.40±0.10	$0.016^{+0.004}_{-0.005}$	
	E	0.2±0.1	0.008±0.004	
	F	3.0 MAX.	0.119 MAX.	
7 100 Y.Co.	G	2.55±0.1	0.100+0.005	
WWW. 100X.Co	H	11.8±0.3	$0.465^{+0.012}_{-0.013}$	
7 WWW. 100X.C	TMO	8.4±0.1	0.331+0.004	
MAN OUX	CO J	1.7±0.2	0.067±0.008	
WWW.Ioo	COK	$0.20^{+0.07}_{-0.03}$	$0.008^{+0.003}_{-0.002}$	
	N.CON	0.7±0.2	$0.028^{+0.008}_{-0.009}$	
	M	0.12	0.005	
	N	0.10	0.004	
	P	5°±5°	5°±5°	
	. ON V.C	ON TWI	P28GU-50-450A-1	

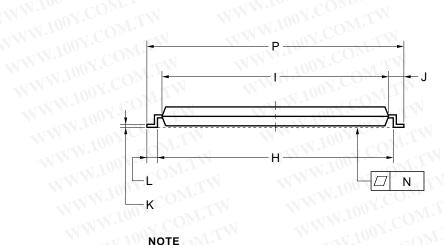


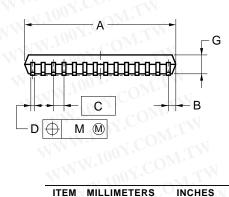
#### 28PIN PLASTIC TSOP ( I ) (8×13.4)



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WWW.100

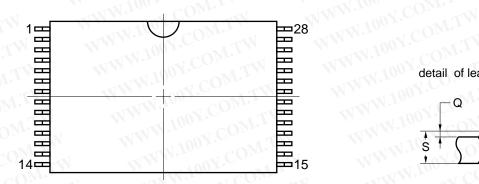
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- (1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition
  - (2) "A" excludes mold flash. (Includes mold flash: 8.4mm MAX. <0.331 inch MAX.>)

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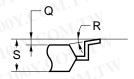
	ITEM	MILLIMETERS	INCHES
3 inch) of	Α	8.0±0.1	0.315±0.004
·	В	0.6 MAX.	0.024 MAX.
	С	0.55 (T.P.)	0.022 (T.P.)
4mm MAX.	D	$0.22^{+0.08}_{-0.07}$	0.009±0.003
	G	1.0	0.039
	Н	12.4±0.2	0.488±0.008
	1	11.8±0.1	$0.465^{+0.004}_{-0.005}$
	J	0.8±0.2	0.031+0.009
	K	0.145 <sup>+0.025</sup> -0.015	0.006±0.001
	L	0.5±0.1	0.020+0.004
	М	0.08	0.003
	N	0.10	0.004
	Р	13.4±0.2	0.528+0.008
	Q	0.1±0.05	0.004±0.002
	R	3°+7° -3°	3°+7° -3°
	S	1.2 MAX.	0.048 MAX.
	On	-CVV	P28GW-55-9JL-1

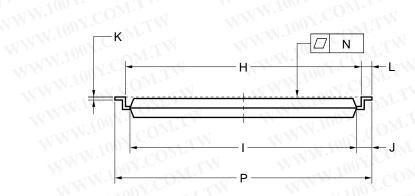
#### 28PIN PLASTIC TSOP ( I ) (8×13.4)

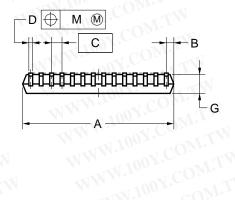


detail of lead end

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#### NOTE

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- (1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
- (2) "A" excludes mold flash. (Includes mold flash: 8.4mm MAX. <0.331 inch MAX.>)

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ITEI	M MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
В	0.6 MAX.	0.024 MAX.
С	0.55 (T.P.)	0.022 (T.P.)
D	$0.22^{+0.08}_{-0.07}$	0.009±0.003
G	1.0	0.039
Н	12.4±0.2	0.488±0.008
T.	11.8±0.1	0.465+0.004
J	0.8±0.2	0.031+0.009
K	0.145 <sup>+0.025</sup> -0.015	0.006±0.001
COME	0.5±0.1	0.020+0.004
M	0.08	0.003
N	0.10	0.004
Р	13.4±0.2	0.528+0.008
Q	0.1±0.05	0.004±0.002
R	3°+7° -3°	3°+7° -3°
S	1.2 MAX.	0.048 MAX.
001.	TW	P28GW-55-9KL-1



#### **Recommended Soldering Conditions**

The following conditions (See table below) must be met when soldering  $\mu$ PD43256B. For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

#### Types of Surface Mount Device

```
\muPD43256BGU: 28-pin plastic SOP (450 mil)
\muPD43256BGW-9JL: 28-pin plastic TSOP (I) (8 × 13.4 mm) (Normal bent)
\muPD43256BGW-9KL: 28-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)
  Please consult with our sales offices.
```

#### Type of Through Hole Mount Device

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#### $\mu$ PD43256BCZ: 28-pin plastic DIP (600 mil)

Soldering process	Soldering conditions	
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	NAM:TO
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)	WWW.

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#### **NOTES FOR CMOS DEVICES**

#### (1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

#### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

#### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices. the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster Special: systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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