

R1LV0108E Series

1Mb Advanced LPSRAM (128k word x 8bit)

R10DS0152EJ0100

Rev.1.00

2013.6.21

Description

The R1LV0108E Series is a family of low voltage 1-Mbit static RAMs organized as 131,072-word by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LV0108E Series has realized higher density, higher performance and low power consumption. The R1LV0108E Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. It has been packaged in 32-pin SOP, 32-pin TSOP and 32-pin sTSSOP.

Features

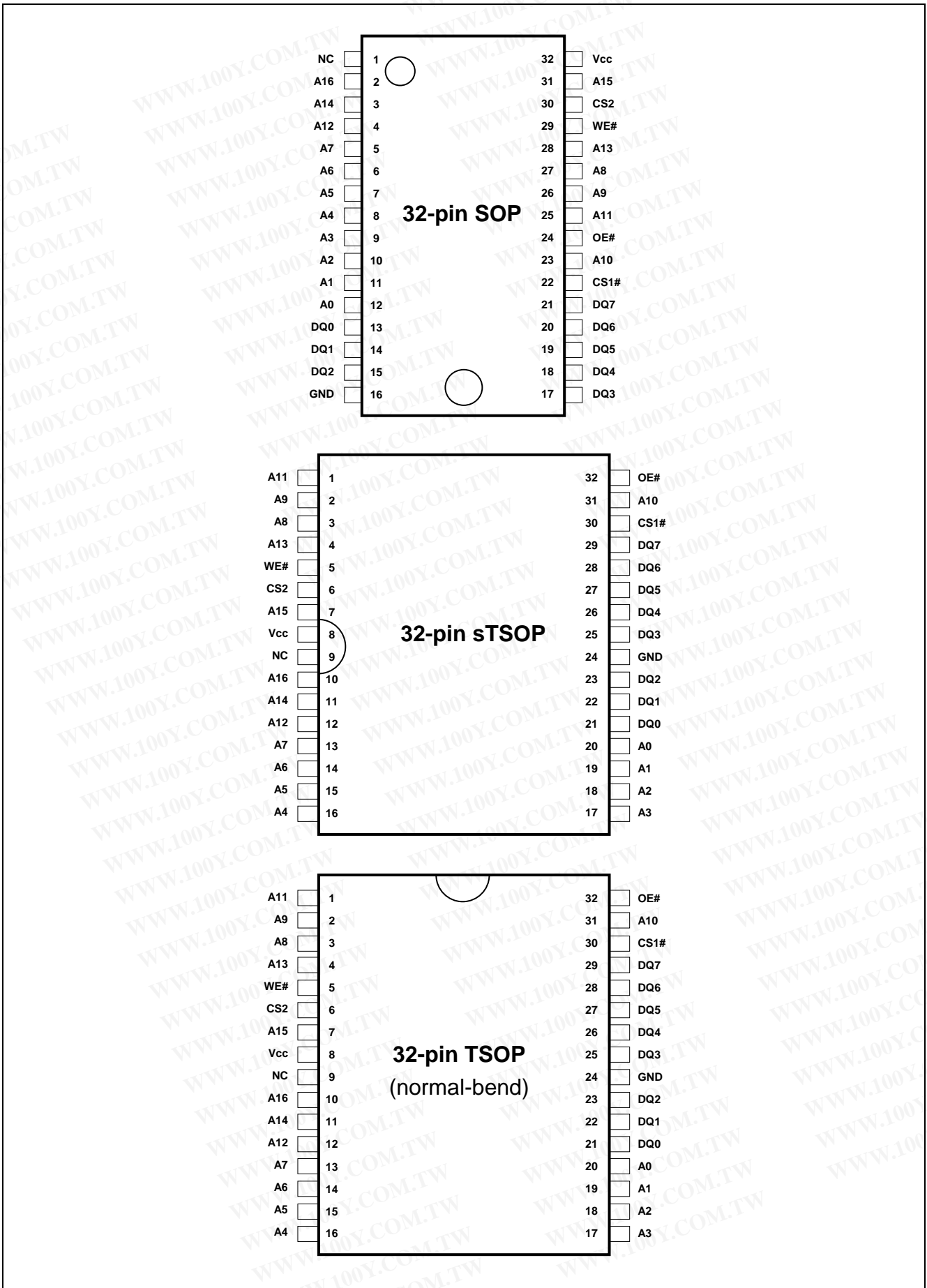
- Single 2.7~3.6V power supply
- Small stand-by current: 0.6μA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1# and CS2
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

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Ordering Information

| Orderable Part Name | Access time | Temperature Range | Package | Shipping Container | Quantity |
|---------------------|-------------|-------------------|---|--------------------|---|
| R1LV0108ESN-5SR#B* | 55 ns | 0 ~ +70°C | 525-mil 32-pin plastic SOP | Tube | Max. 25pcs/Tube Max. 225pcs/Inner Bag Max. 900pcs/Inner Box |
| R1LV0108ESN-5SI#B* | | -40 ~ +85°C | | | |
| R1LV0108ESN-7SR#B* | 70 ns | 0 ~ +70°C | | | |
| R1LV0108ESN-7SI#B* | | -40 ~ +85°C | | | |
| R1LV0108ESN-5SR#S* | 55 ns | 0 ~ +70°C | PRSP0032DF-A (32P2S-A) | Embossed tape | 1000pcs/Reel |
| R1LV0108ESN-5SI#S* | | -40 ~ +85°C | | | |
| R1LV0108ESN-7SR#S* | 70 ns | 0 ~ +70°C | | | |
| R1LV0108ESN-7SI#S* | | -40 ~ +85°C | | | |
| R1LV0108ESA-5SR#B* | 55 ns | 0 ~ +70°C | 8mm×13.4mm 32-pin plastic sT SOP (normal-bend type) | Tray | Max. 234pcs/Tray Max. 1872pcs/Inner Box |
| R1LV0108ESA-5SI#B* | | -40 ~ +85°C | | | |
| R1LV0108ESA-7SR#B* | 70 ns | 0 ~ +70°C | | | |
| R1LV0108ESA-7SI#B* | | -40 ~ +85°C | | | |
| R1LV0108ESA-5SR#S* | 55 ns | 0 ~ +70°C | PTSA0032KB-A (32P3K-B) | Embossed tape | 1000pcs/Reel |
| R1LV0108ESA-5SI#S* | | -40 ~ +85°C | | | |
| R1LV0108ESA-7SR#S* | 70 ns | 0 ~ +70°C | | | |
| R1LV0108ESA-7SI#S* | | -40 ~ +85°C | | | |
| R1LV0108ESF-5SR#B* | 55 ns | 0 ~ +70°C | 8mm×20mm 32-pin plastic TSOP (normal-bend type) | Tray | Max. 156pcs/Tray Max. 1248pcs/Inner Box |
| R1LV0108ESF-5SI#B* | | -40 ~ +85°C | | | |
| R1LV0108ESF-7SR#B* | 70 ns | 0 ~ +70°C | | | |
| R1LV0108ESF-7SI#B* | | -40 ~ +85°C | | | |
| R1LV0108ESF-5SR#S* | 55 ns | 0 ~ +70°C | PTSA0032KA-A (32P3H-E) | Embossed tape | 1000pcs/Reel |
| R1LV0108ESF-5SI#S* | | -40 ~ +85°C | | | |
| R1LV0108ESF-7SR#S* | 70 ns | 0 ~ +70°C | | | |
| R1LV0108ESF-7SI#S* | | -40 ~ +85°C | | | |

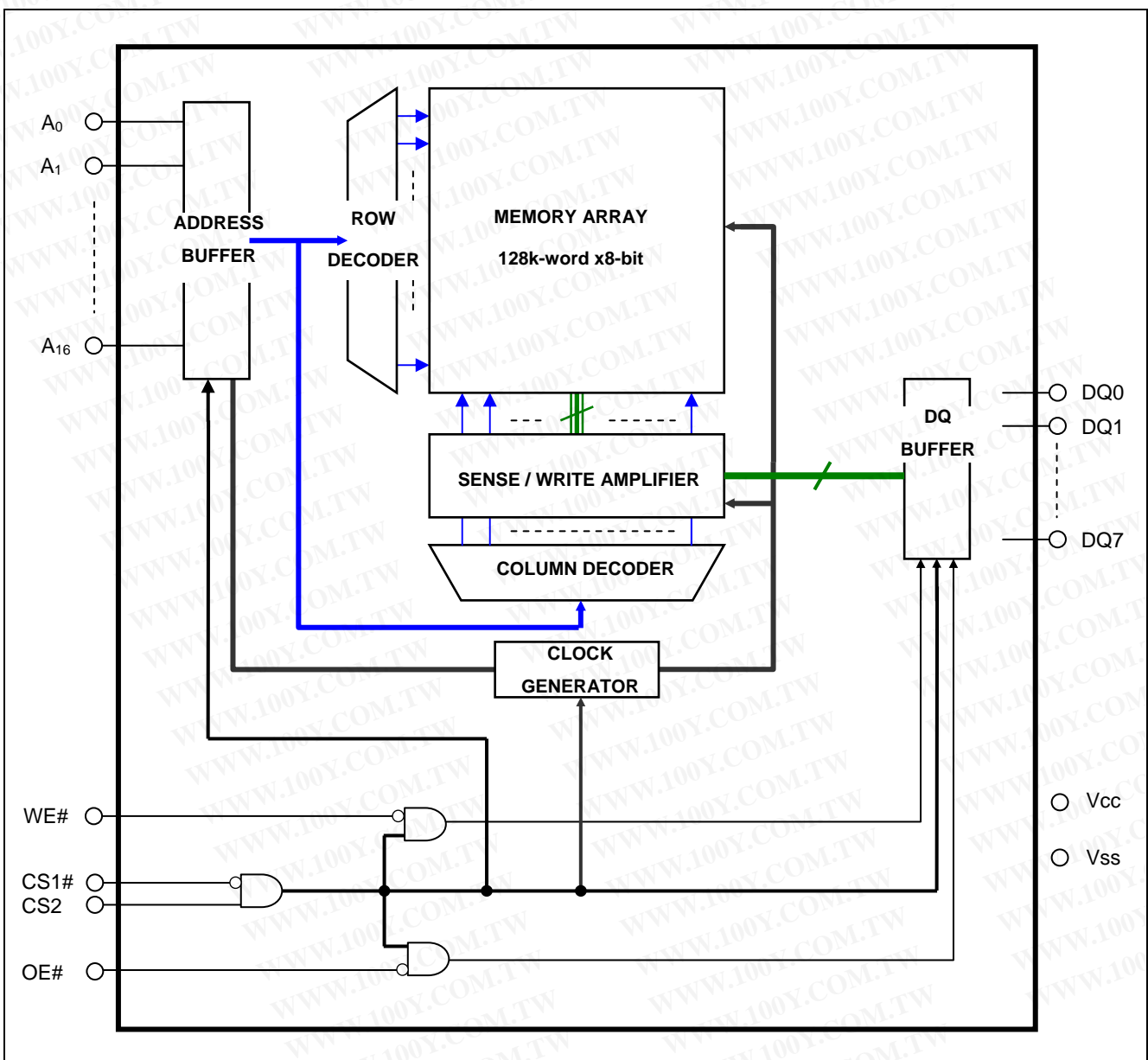
Pin Arrangement



Pin Description

| Pin name | Function |
|------------|-------------------|
| Vcc | Power supply |
| Vss | Ground |
| A0 to A16 | Address input |
| DQ0 to DQ7 | Data input/output |
| CS1# | Chip select 1 |
| CS2 | Chip select 2 |
| WE# | Write enable |
| OE# | Output enable |
| NC | Non connection |

Block Diagram



Operation Table

| CS1# | CS2 | WE# | OE# | DQ0~7 | Operation |
|------|-----|-----|-----|--------|----------------|
| X | L | X | X | High-Z | Stand-by |
| H | X | X | X | High-Z | Stand-by |
| L | H | L | X | Din | Write |
| L | H | H | L | Dout | Read |
| L | H | H | H | High-Z | Output disable |

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

| Parameter | Symbol | Value | unit |
|---|-----------------|----------------------------------|------------|
| Power supply voltage relative to Vss | Vcc | -0.3 to +4.6 | V |
| Terminal voltage on any pin relative to Vss | V_T | -0.3^{*1} to $V_{cc}+0.3^{*2}$ | V |
| Power dissipation | P_T | 0.7 | W |
| Operation temperature | T_{opr}^{*3} | R Ver. | 0 to +70 |
| | | I Ver. | -40 to +85 |
| Storage temperature range | T_{stg} | -65 to 150 | °C |
| Storage temperature range under bias | T_{bias}^{*3} | R Ver. | 0 to +70 |
| | | I Ver. | -40 to +85 |

Note 1. -3.0V for pulse ≤ 30 ns (full width at half maximum)

2. Maximum voltage is +4.6V.

3. Ambient temperature range depends on R/I-version. Please see table on page 1.

DC Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note | |
|---------------------------|-----------------|----------------|------|----------------------|------|------|---|
| Supply voltage | V _{CC} | 2.7 | 3.0 | 3.6 | V | | |
| | V _{SS} | 0 | 0 | 0 | V | | |
| Input high voltage | V _{IH} | 2.0 | - | V _{CC} +0.3 | V | | |
| Input low voltage | V _{IL} | -0.3 | - | 0.6 | V | 1 | |
| Ambient temperature range | R Ver. | T _a | 0 | - | +70 | °C | 2 |
| | I Ver. | | -40 | - | +85 | °C | 2 |

- Note
1. -3.0V for pulse \leq 30ns (full width at half maximum)
 2. Ambient temperature range depends on R/I-version. Please see table on page 1.

DC Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions | |
|---------------------------|------------------|--------------------------|-------------------|------|---------|--|--|
| Input leakage current | I _{LI} | - | - | 1 | μ A | V _{in} = V _{SS} to V _{CC} | |
| Output leakage current | I _{LO} | - | - | 1 | μ A | CS1# = V _{IH} or CS2 = V _{IL} or OE# = V _{IH} , V _{I/O} = V _{SS} to V _{CC} | |
| Average operating current | I _{CC1} | - | 15 | 25 | mA | Min. cycle, duty = 100%, I _{I/O} = 0mA CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL} | |
| | I _{CC2} | - | 2 | 5 | mA | Cycle = 1 μ s, duty = 100%, I _{I/O} = 0mA CS1# \leq 0.2V, CS2 \geq V _{CC} -0.2V, V _{IH} \geq V _{CC} -0.2V, V _{IL} \leq 0.2V | |
| Standby current | I _{SB} | - | - | 0.33 | mA | "CS2 = V _{IL} " or "CS2 = V _{IH} and CS1# = V _{IH} ", Others = V _{SS} to V _{CC} | |
| Standby current | I _{SB1} | - | 0.6 ^{*1} | 2 | μ A | ~+25°C | V _{in} = V _{SS} to V _{CC} (1) CS2 \leq 0.2V or (2) CS1# \geq V _{CC} -0.2V, CS2 \geq V _{CC} -0.2V |
| | | - | - | 3 | μ A | ~+40°C | |
| | | - | - | 8 | μ A | ~+70°C | |
| | | - | - | 10 | μ A | ~+85°C | |
| Output high voltage | V _{OH} | 2.4 | - | - | V | I _{OH} = -0.5mA | |
| | V _{OH2} | V _{CC} - 0.5 | - | - | V | I _{OH} = -0.05mA | |
| Output low voltage | V _{OL} | - | - | 0.4 | V | I _{OL} = 2mA | |

- Note
1. Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.

Capacitance

(V_{CC} = 2.7V ~ 3.6V, f = 1MHz, T_a = 0 ~ +70°C / -40 ~ +85°C^{*2})

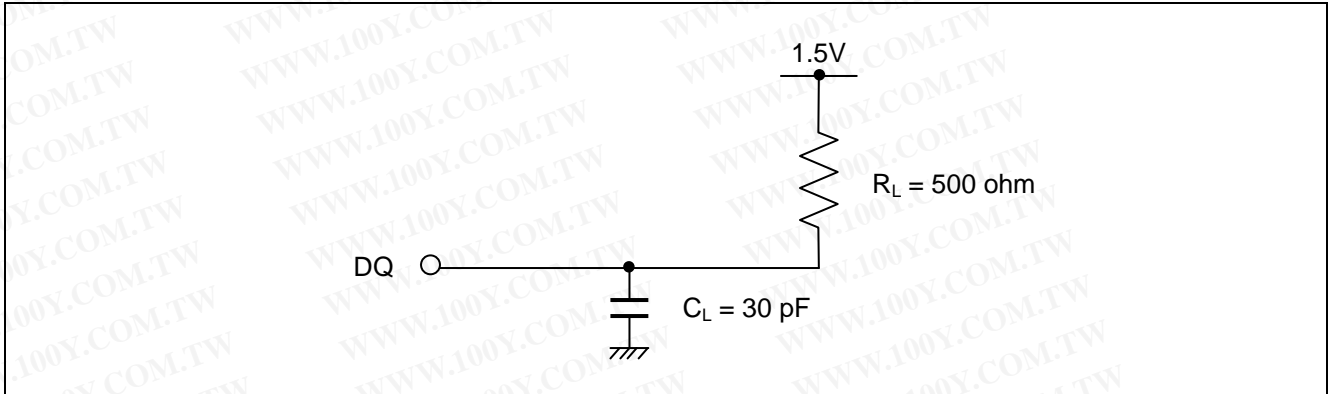
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions | Note |
|----------------------------|------------------|------|------|------|------|-----------------------|------|
| Input capacitance | C _{in} | - | - | 8 | pF | V _{in} = 0V | 1 |
| Input / output capacitance | C _{I/O} | - | - | 10 | pF | V _{I/O} = 0V | 1 |

- Note
1. This parameter is sampled and not 100% tested.
 2. Ambient temperature range depends on R/I-version. Please see table on page 1.

AC Characteristics

Test Conditions ($V_{CC} = 2.7V \sim 3.6V$, $T_a = 0 \sim +70^{\circ}C / -40 \sim +85^{\circ}C^{*1}$)

- Input pulse levels: $V_{IL} = 0.4V$, $V_{IH} = 2.2V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Note 1. Ambient temperature range depends on R/I-version. Please see table on page 1.

Read Cycle

| Parameter | Symbol | R1LV0108E**-5** | | R1LV0108E**-7** | | Unit | Note |
|------------------------------------|------------|-----------------|------|-----------------|------|------|-------|
| | | Min. | Max. | Min. | Max. | | |
| Read cycle time | t_{RC} | 55 | - | 70 | - | ns | |
| Address access time | t_{AA} | - | 55 | - | 70 | ns | |
| Chip select access time | t_{ACS1} | - | 55 | - | 70 | ns | |
| | t_{ACS2} | - | 55 | - | 70 | ns | |
| Output enable to output valid | t_{OE} | - | 30 | - | 35 | ns | |
| Output hold from address change | t_{OH} | 5 | - | 10 | - | ns | |
| Chip select to output in low-Z | t_{CLZ1} | 5 | - | 10 | - | ns | 2,3 |
| | t_{CLZ2} | 5 | - | 10 | - | ns | 2,3 |
| Output enable to output in low-Z | t_{OLZ} | 5 | - | 5 | - | ns | 2,3 |
| Chip deselect to output in high-Z | t_{CHZ1} | 0 | 20 | 0 | 25 | ns | 1,2,3 |
| | t_{CHZ2} | 0 | 20 | 0 | 25 | ns | 1,2,3 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 20 | 0 | 25 | ns | 1,2,3 |

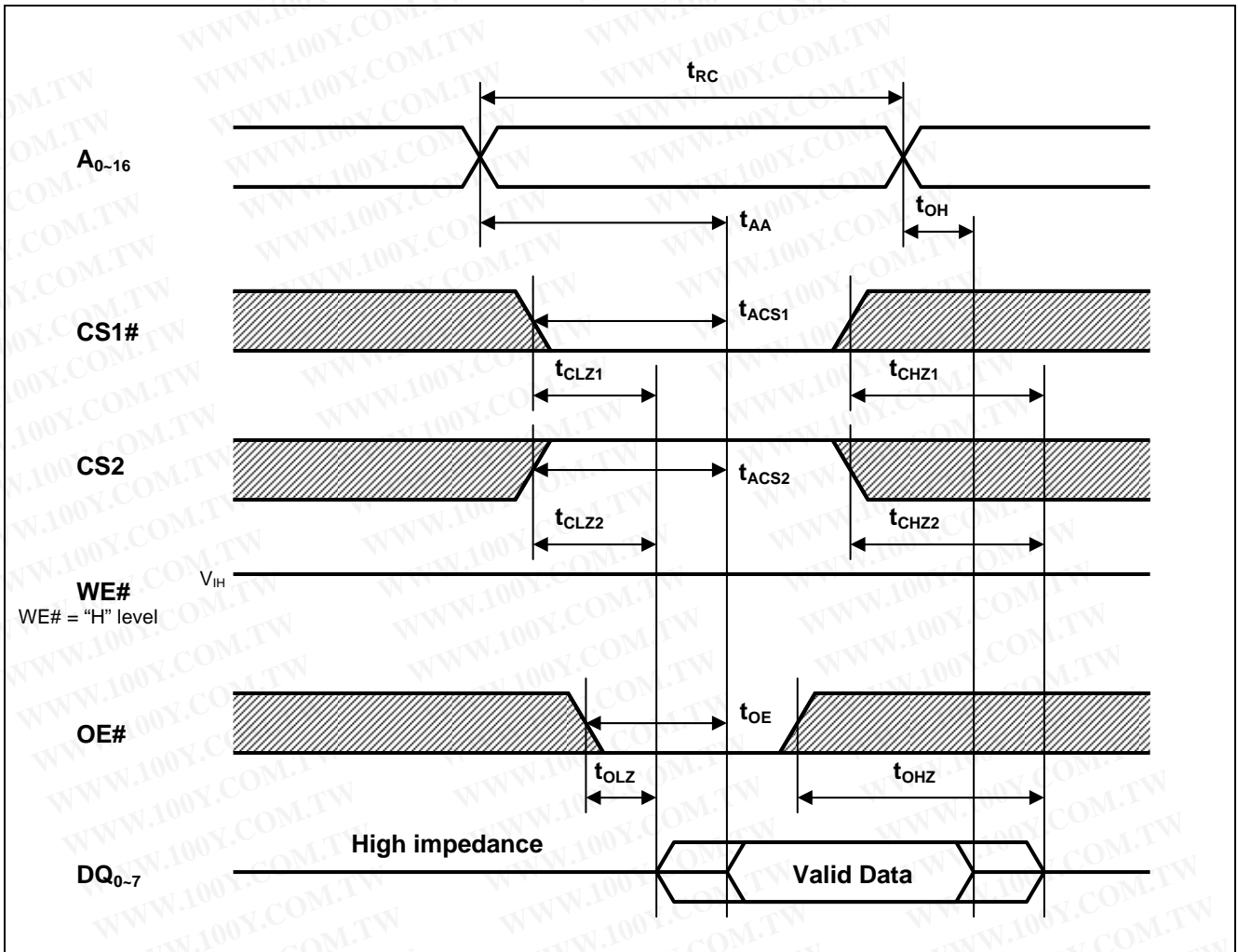
Write Cycle

| Parameter | Symbol | R1LV0108E**-5** | | R1LV0108E**-7** | | Unit | Note |
|------------------------------------|-----------|-----------------|------|-----------------|------|------|------|
| | | Min. | Max. | Min. | Max. | | |
| Write cycle time | t_{WC} | 55 | - | 70 | - | ns | |
| Address valid to end of write | t_{AW} | 50 | - | 55 | - | ns | |
| Chip select to end of write | t_{CW} | 50 | - | 55 | - | ns | 5 |
| Write pulse width | t_{WP} | 45 | - | 50 | - | ns | 4 |
| Address setup time | t_{AS} | 0 | - | 0 | - | ns | 6 |
| Write recovery time | t_{WR} | 0 | - | 0 | - | ns | 7 |
| Data to write time overlap | t_{DW} | 25 | - | 30 | - | ns | |
| Data hold from write time | t_{DH} | 0 | - | 0 | - | ns | |
| Output enable from end of write | t_{OW} | 5 | - | 5 | - | ns | 2 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 20 | 0 | 25 | ns | 1,2 |
| Write to output in high-Z | t_{WHZ} | 0 | 20 | 0 | 25 | ns | 1,2 |

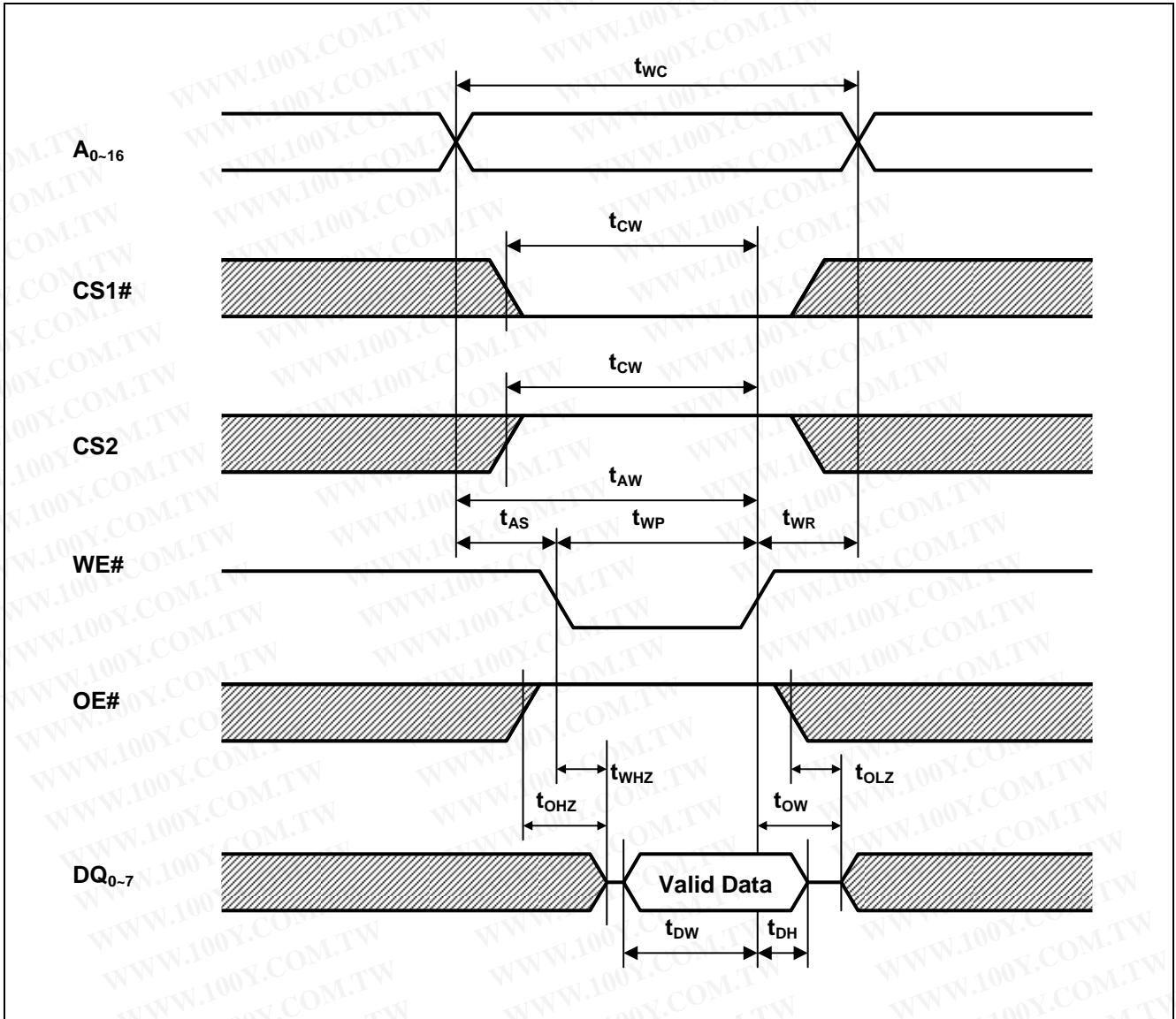
- Note
- t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 - A write occurs during the overlap of a low CS1#, a high CS2, a low WE#.
 - A write begins at the latest transition among CS1# going low, CS2 going high and WE# going low.
 - A write ends at the earliest transition among CS1# going high, CS2 going low and WE# going high.
 - t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
 - t_{AS} is measured the address valid to the beginning of write.
 - t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.
 - Don't apply inverted phase signal externally when DQ pin is output mode.

Timing Waveforms

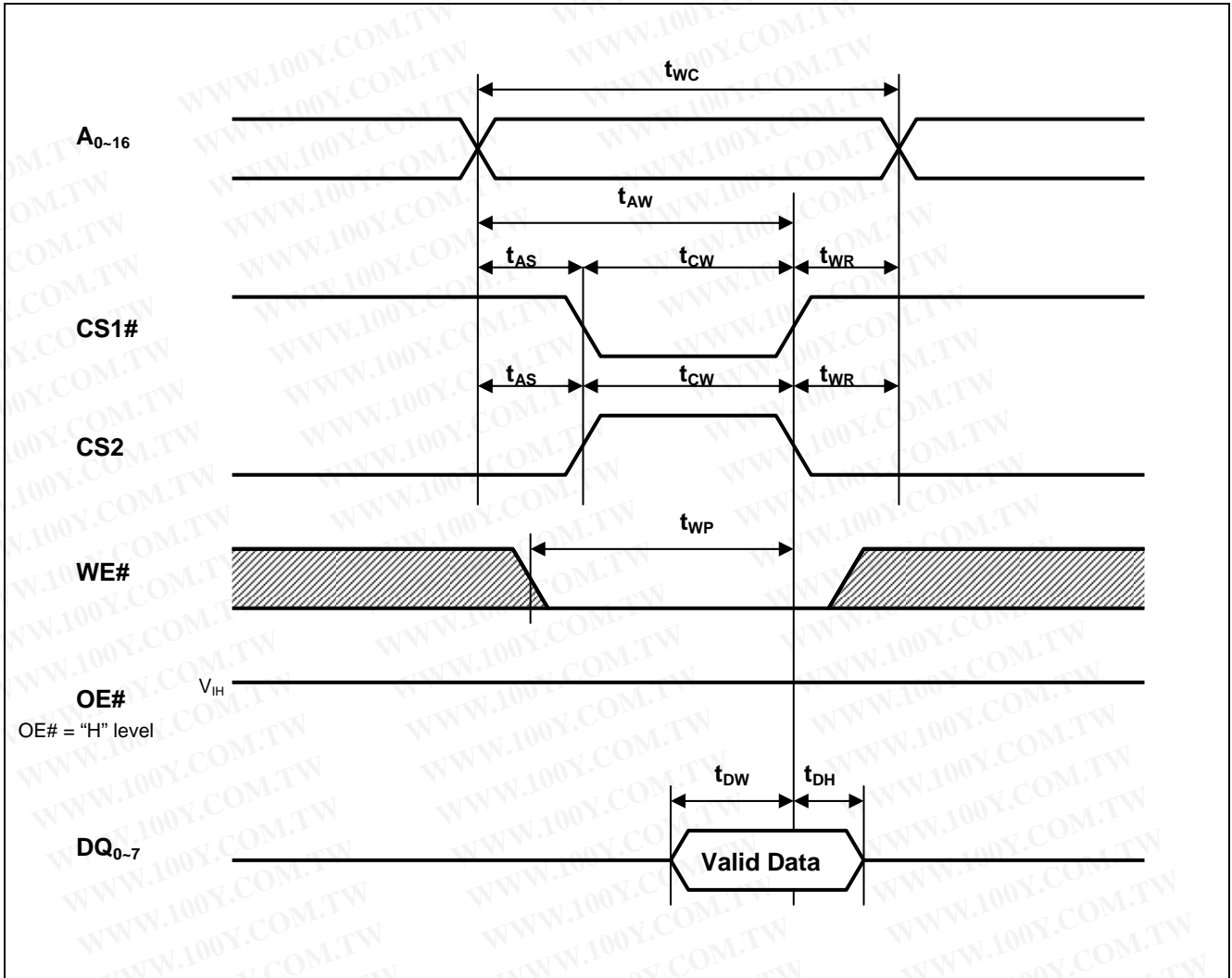
Read Cycle



Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS1#, CS2 CLOCK)

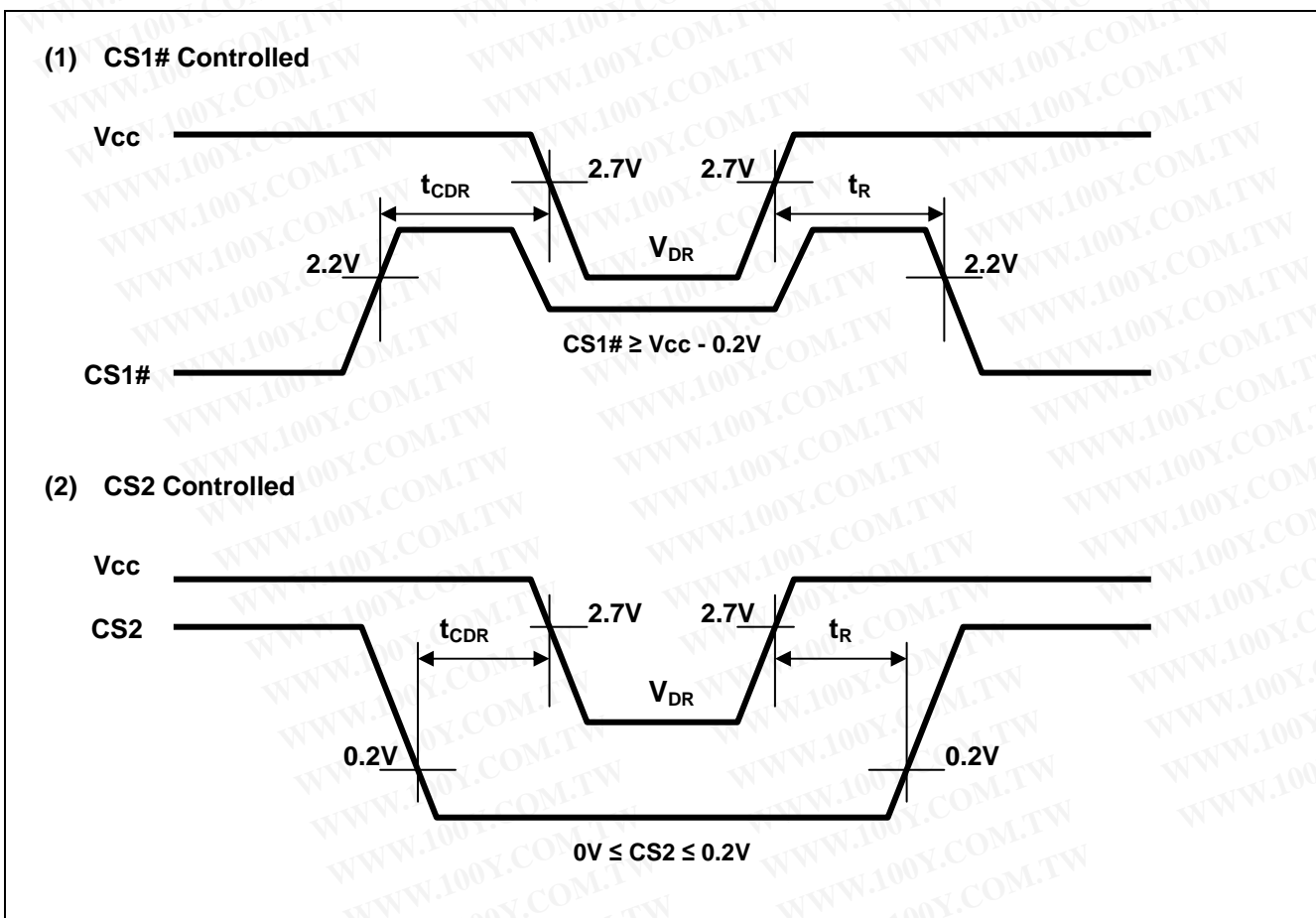


Low Vcc Data Retention Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions ² | |
|--------------------------------------|-------------------|------|-------------------|------|------|--|---|
| V _{CC} for data retention | V _{DR} | 2.0 | - | 3.6 | V | V _{in} ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V | |
| Data retention current | I _{CCDR} | - | 0.6 ^{*1} | 2 | μA | ~+25°C | V _{CC} =3.0V, V _{in} ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V |
| | | - | - | 3 | μA | ~+40°C | |
| | | - | - | 8 | μA | ~+70°C | |
| | | - | - | 10 | μA | ~+85°C | |
| Chip deselect to data retention time | t _{CDR} | 0 | - | - | ns | See retention waveform. | |
| Operation recovery time | t _R | 5 | - | - | ms | | |

- Note
- Typical parameter indicates the value for the center of distribution at 3.0V (T_a= 25°C), and not 100% tested.
 - CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE#, OE#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms



| | |
|------------------|-----------------------------|
| Revision History | R1LV0108E Series Data Sheet |
|------------------|-----------------------------|

| Rev. | Date | Description | |
|------|-----------|-------------|----------------------|
| | | Page | Summary |
| 1.00 | 2013.6.21 | - | First Edition issued |
| | | | |

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