SONY CXK5816PN/M

10/10L/12/
12L/15/15L

2048-word × 8 bit High Speed CMOS Static RAM

Description

CXK5816PN/M is a 16,384 bits high speed CMOS static RAM organized as 2,048 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power spplications in which battery back up for nonvolatility is required.

Features

- High speed operation (Access time)
  - CXK5816PN/M -10, 10L 100ns (Max.)
  - CXK5816PN/M -12, 12L 120ns (Max.)
  - CXK5816PN/M -15, 15L 150ns (Max.)
- Low power consumption (Standby) (Operation)
  - CXK5816PN/M -10, 12, 15 100μW(Typ.) 125mW(Typ.)
  - CXK5816PN/M -10L, 12L, 15L 5μW(Typ.) 125mW(Typ.)
- Single +5V supply: 5V±10%.
- Fully static memory ..... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)

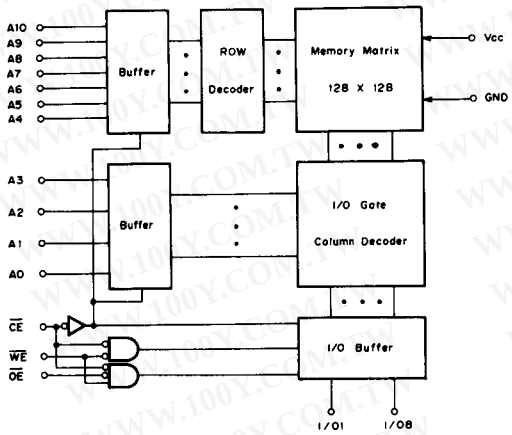
Function

2048-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

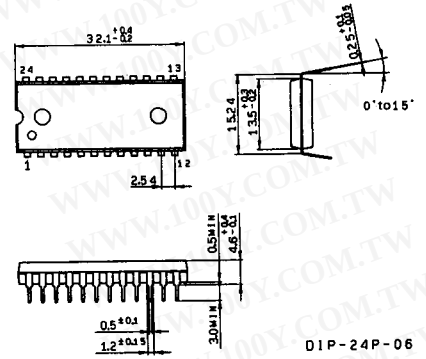
Block Diagram



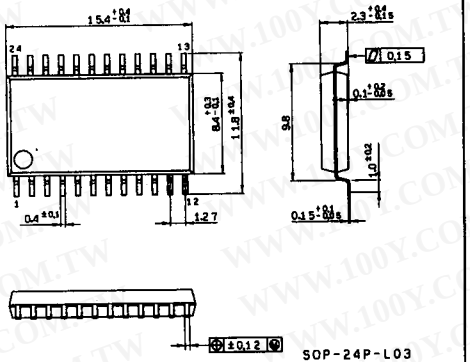
Package Outline

Unit: mm

CXK5816PN 24 Pin DIP (Plastic)

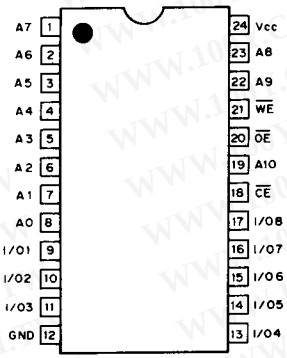


CXK5816M 24 Pin SOP (Plastic)



Note) All Typical values are measured under the conditions Vcc=5.0V and Ta=25°C.

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A10	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

Ta = 25°C, GND = 0V

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5* to +7.0	V
Input voltage	V_{IN}		−0.5* to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		−0.5* to Vcc+0.5	V
Allowable power dissipation	P_D	CXK5816PN/SP	1.0	W
		CXK5816M	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260·10	°C • sec

* V_{CC}, V_{IN} $V_{I/O}$ Minimum value=−3.0V, Pulse width is under 50 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	D out	I_{CC1}, I_{CC2}
L	X	L	Write	D in	I_{CC1}, I_{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to +70°C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3	—	0.8	V

DC and Operating Characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5816PN/M/SP −10/12/15			CXK5816PN/M/SP −10L/12L/15L			Unit
			Min.	Typ.**	Max.	Min.	Typ.**	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−2	—	2	−2	—	2	μA
Output leakage current	I_{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	−2	—	2	−2	—	2	μA
Operating power supply current	I_{CC1}	$\overline{CE}=V_{IL}$, $I_{OUT}=0$mA	—	25	60	—	25	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100% $I_{OUT}=0$mA	—	28 *(31)	60 *(75)	—	28 *(31)	60 *(75)	mA
Standby current	I_{SB1}	$\overline{CE}\geqq V_{CC}-0.2V$	—	0.02	1.0	—	0.001	0.05	mA
	I_{SB2}	$\overline{CE}=V_{IH}$	—	0.3	2	—	0.2	1	mA
Output high voltage	V_{OH}	$I_{OH}=-1.0$mA	2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL}=4.0$mA	—	—	0.4	—	—	0.4	V

*** Note)** Shows CXK5816PN/M/SP-10, 10L value.

** V_{CC}=5V, Ta=25°C

Capacitance

Ta=25°C, f=1 MHz

Item	Test condition	Symbol	Min.	Max.	Unit
Input capacitance	V_{IN}=0V	C_{IN}	—	7	pF
Input/output capacitance	$V_{I/O}$=0V	$C_{I/O}$	—	10	pF

Note) This parameter is sampled and is not 100% tested.

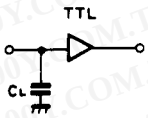
AC Operating Characteristics

- **AC test condition**

V_{CC} = 5V ± 10%, Ta = 0 to +70°C

Item	Condition
Input pulse high level	$V_{IH}=2.4V$
Input pulse low level	$V_{IL}=0.6V$
Input rise time	$t_R=5$ns
Input fall time	$t_F=5$ns
Input and output timing reference level	1.5V
Output load	C_L* = 100pF, 1TTL

* C_L includes scope and jig capacitance.



• **Read cycle**

Item	Symbol	CXK5816PN/M −10/10L		CXK5816PN/M −12/12L		CXK5816PN/M −15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time	t_{CO}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	55	—	60	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	15	—	15	—	15	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	10	—	10	—	10	—	ns
Chip disable to output in high Z ($\overline{CE}$)	*t_{HZ}	0	30	0	40	0	50	ns
Output disable to output in high Z ($\overline{OE}$)	*t_{OHZ}	0	30	0	40	0	50	ns

*** Note)** t_{HZ} and t_{OHZ} are specified by the time length until the output circuit is turned off and not specified by the output voltage level.

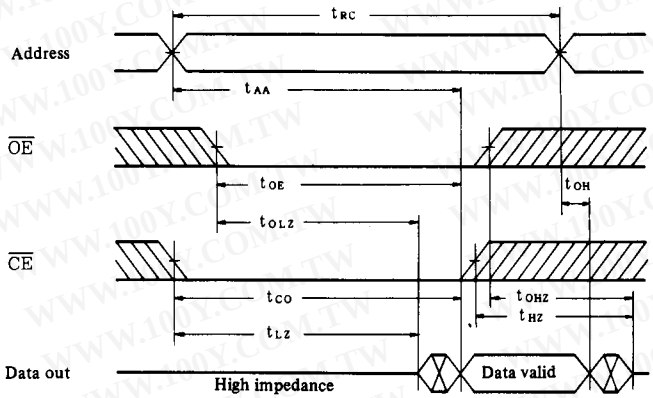
• **Write cycle**

Item	Symbol	CXK5816PN/M −10/10L		CXK5816PN/M −12/12L		CXK5816PN/M −15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	80	—	100	—	120	—	ns
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	60	—	75	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	5	—	5	—	5	—	ns
Output active from end of write	t_{OW}	15	—	15	—	15	—	ns
Write to output in high Z	t_{WHZ}*	0	30	0	40	0	50	ns

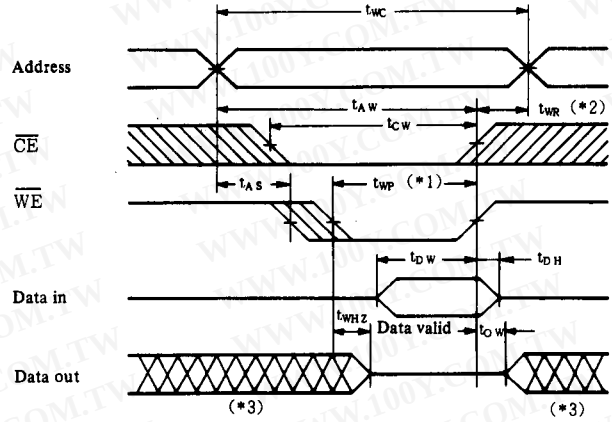
*** Note)** t_{WHZ} is specified by the time length until the output circuit is turned off and not specified by the output voltage level.

Timing Waveform

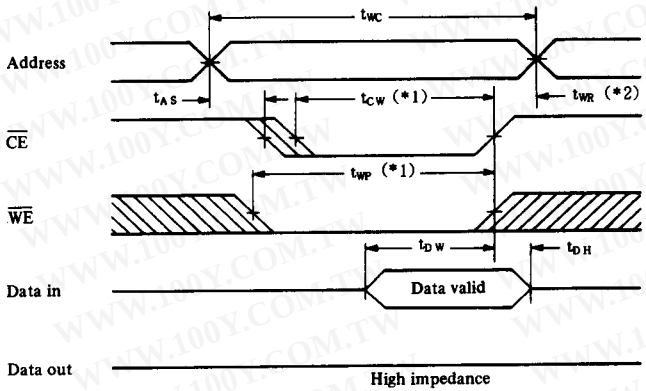
(1) Read Cycle [$\overline{WE}$=V_{IH}]



(2) Write Cycle (1): $\overline{WE}$ Control [$\overline{OE}$=V_{IH}]



Write Cycle (2): $\overline{CE}$ Control [$\overline{OE}$=V_{IL}]



Note)

*1 A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
*2 t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
*3 During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

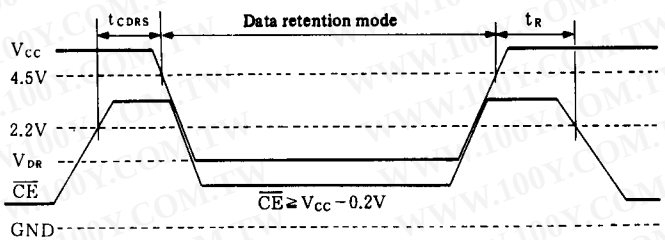
Data Retention Characteristics

Ta = 0 to +70°C

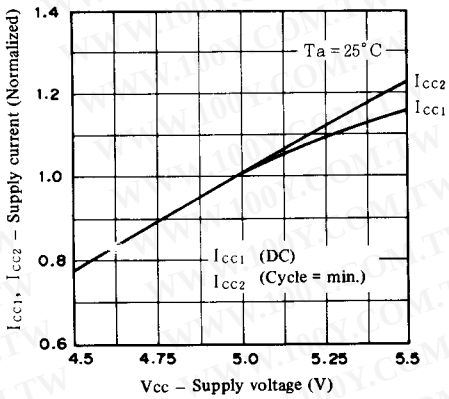
Item	Symbol	Test condition	CXK5816PN/M -10/12/15			CXK5816PN/M -10L/12L/15L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$	2.0	5.0	5.5	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} =3.0V, $\overline{CE} \geqq 2.8V$	—	12	600	—	0.6	30	μA
	I_{CCDR2}	V_{CC} =2.0 to 5.5V, $\overline{CE} \geqq V_{CC}-0.2V$	—	20	1000	—	1.0	50	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		t_{RC}*	—	—	t_{RC}*	—	—	ns

* t_{RC} : Read cycle time

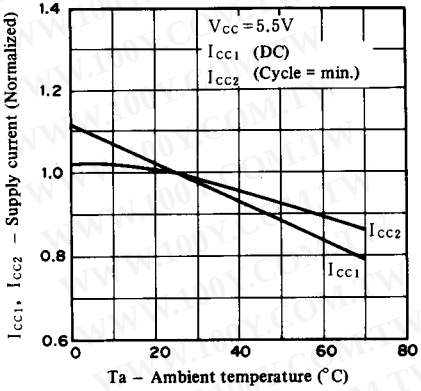
Data Retention Waveform



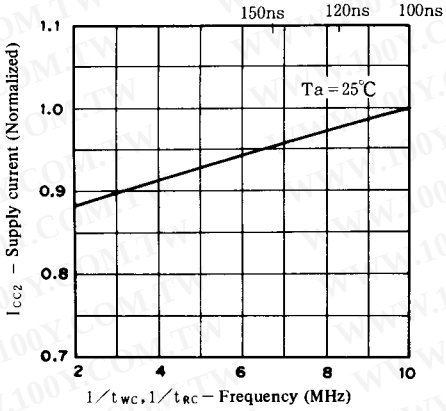
Supply current vs. Supply voltage



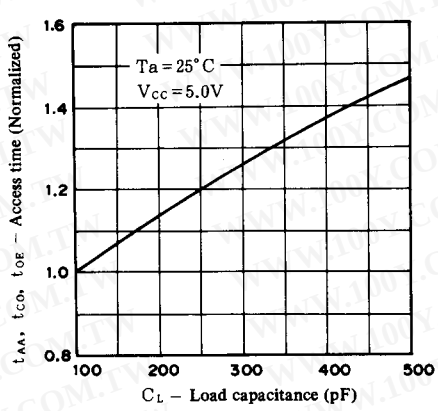
Supply current vs. Ambient temperature



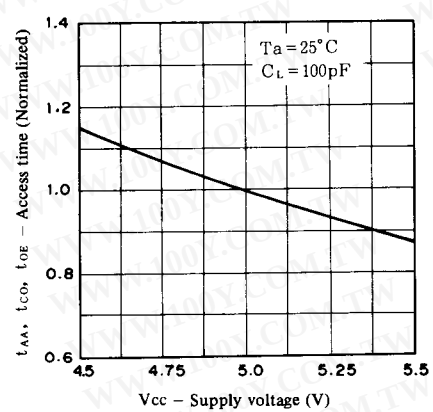
Supply current vs. Frequency



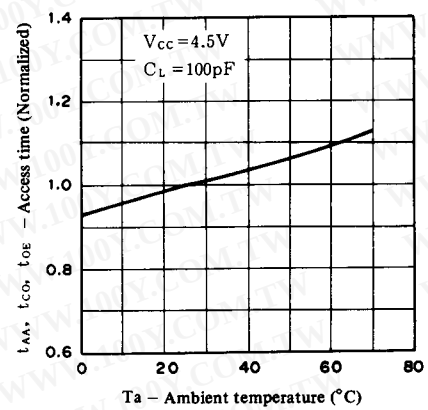
Access time vs. Load capacitance



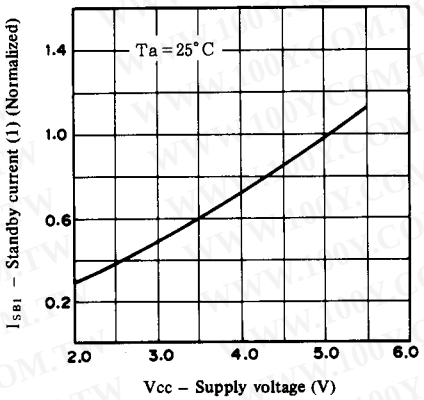
Access time vs. Supply voltage



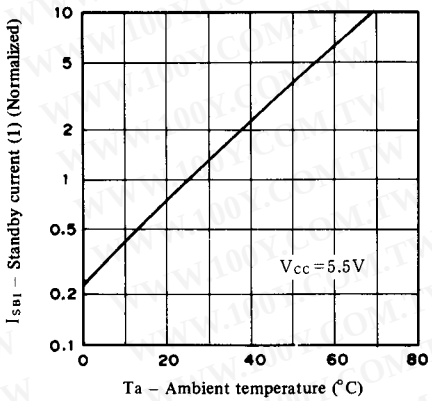
Access time vs. Ambient temperature



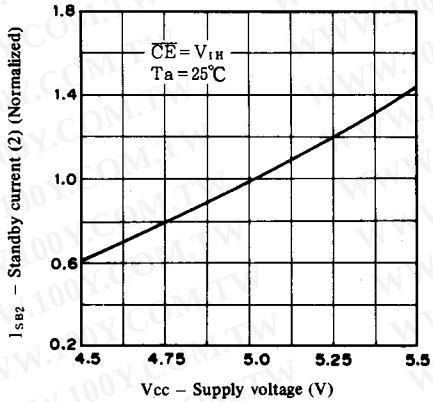
Standby current (1) vs. Supply voltage



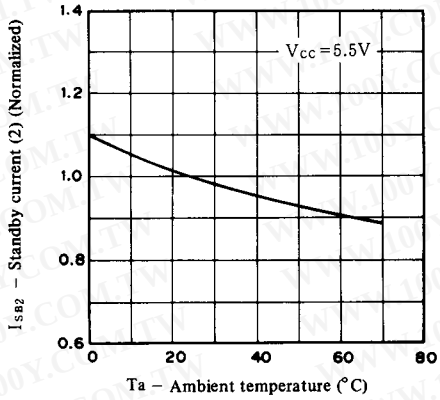
Standby current (1) vs. Ambient temperature



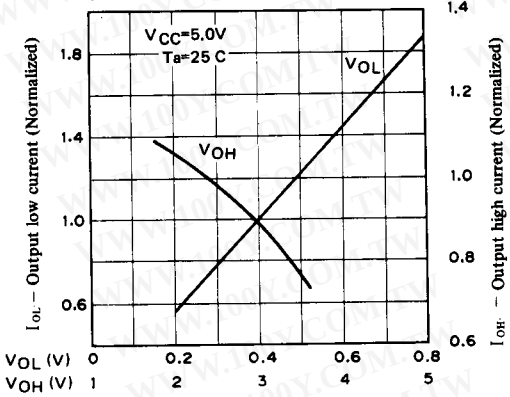
Standby current (2) vs. Supply voltage



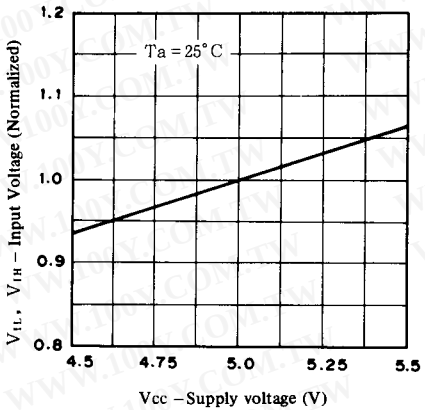
Standby current (2) vs. Ambient temperature



Output high current vs. Output high voltage
Output low current vs. Output low voltage

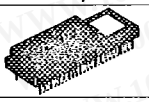


Input voltage vs. Supply voltage



T-90-20

7. Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic