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# M24128 M24C64 M24C32

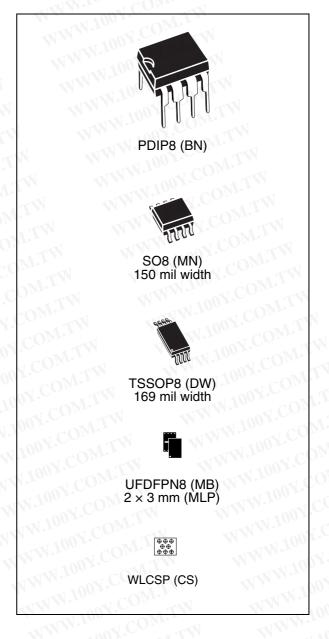
# 128 Kbit, 64 Kbit and 32 Kbit serial I<sup>2</sup>C bus EEPROM

## Features

- Two-wire I<sup>2</sup>C serial interface supports 400 kHz protocol
- Single supply voltages (see Table 1 for root part numbers):
  - 2.5 V to 5.5 V
  - 7 1.8 V to 5.5 V
    - 1.7 V to 5.5 V
- Write Control input
- Byte and Page Write
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 Million write cycles
- More than 40-year data retention
- Packages
  - ECOPACK<sup>®</sup> (RoHS compliant)

Table 1.Device summary	
------------------------	--

Reference	Part number	Supply voltage
MM.	M24128-BW	2.5 V to 5.5V
M24128	M24128-BR	1.8 V to 5.5V
	M24128-BF	1.7 V to 5.5V
W	M24C64-W	2.5 V to 5.5V
M24C64	M24C64-R	1.8 V to 5.5V
	M24C64-F	1.7 V to 5.5V
	M24C32-W	2.5 V to 5.5V
M24C32	M24C32-R	1.8 V to 5.5V
	M24C32-F	1.7 V to 5.5V



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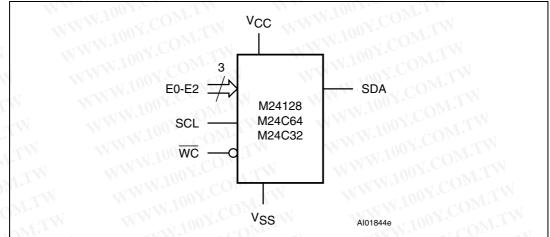
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# Description

The M24C32, M24C64 and M24128 devices are  $l^2$ C-compatible electrically erasable programmable memories (EEPROM). They are organized as 4096 × 8 bits, 8192 × 8 bits and 16384 × 8 bits, respectively.

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I<sup>2</sup>C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I<sup>2</sup>C bus definition.

The device behaves as a slave in the  $I^2C$  protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW) (as described in *Table 3*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9<sup>th</sup> bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

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Table 2.         Signal names	NWW.100 P.CO	M.I.
Signal name	Function	Direction
E0, E1, E2	Chip Enable	Input
SDA	Serial Data	01/0
SCL	Serial Clock	Input
WC COMP	Write Control	Input
V <sub>cc</sub>	Supply voltage	CONT.
V <sub>SS</sub>	Ground	COM

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#### Table 2. Signal names

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WWW.100Y.COM.TW

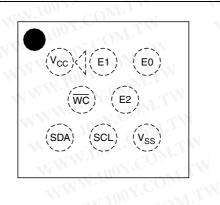
WWW.100

#### Figure 2. **DIP, SO, TSSOP and UFDFPN connections**

M24 <sup>-</sup>	1128 MAN 100 COMPANY
M240	IC64
M240	IC32
E0 [] 1	8]V <sub>CC</sub>
OE1 [2	8 ] V <sub>CC</sub> 7 ] ₩C
E2 🛛 3	6 SCL
V <sub>SS</sub> [ 4	5] SDA
	No lotoc

1. See Package mechanical data section for package dimensions, and how to identify pin-1.

#### Figure 3. M24128 WLCSP connections (top view, marking side, with balls on the underside)



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Signal description

# 2 Signal description

## 2.1 Serial Clock (SCL)

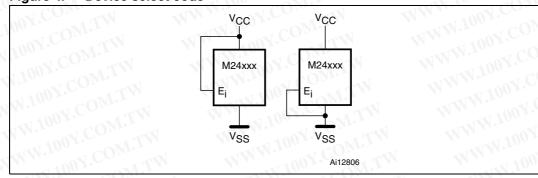
This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to  $V_{CC}$ . (*Figure 5* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

## 2.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to  $V_{CC}$ . (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

## 2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to  $V_{CC}$  or  $V_{SS}$ , to establish the device select code as shown in *Figure 4*. When not connected (left floating), these inputs are read as low (0,0,0).



#### Figure 4. Device select code

## 2.4 Write Control (WC)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ( $\overline{WC}$ ) is driven high. When unconnected, the signal is internally read as V<sub>IL</sub>, and Write operations are allowed.

When Write Control ( $\overline{WC}$ ) is driven high, device select and Address bytes are acknowledged, Data bytes are not acknowledged.

## 2.5 V<sub>SS</sub> ground

 $V_{\text{SS}}$  is the reference for the  $V_{\text{CC}}$  supply voltage.

## 2.6 Supply voltage (V<sub>CC</sub>)

## 2.6.1 Operating supply voltage V<sub>CC</sub>

Prior to selecting the memory and issuing instructions to it, a valid and stable V<sub>CC</sub> voltage within the specified [V<sub>CC</sub>(min), V<sub>CC</sub>(max)] range must be applied (see *Table 9* and *Table 10*). In order to secure a stable DC supply voltage, it is recommended to decouple the V<sub>CC</sub> line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V<sub>CC</sub>/V<sub>SS</sub> package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle  $(t_W)$ .

#### 2.6.2 Power-up conditions

When the power supply is turned on,  $V_{CC}$  rises from  $V_{SS}$  to  $V_{CC}$ . The  $V_{CC}$  rise time must not vary faster than  $1V/\mu s$ .

#### 2.6.3 Device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of  $V_{CC}$ ), the device does not respond to any instruction until  $V_{CC}$  has reached the power on reset threshold voltage (this threshold is lower than the minimum  $V_{CC}$  operating voltage defined in *Table 9* and *Table 10*). Until  $V_{CC}$  passes over the POR threshold, the device is reset and in Standby Power mode.

In a similar way, during power-down (continuous decay of  $V_{CC}$ ), as soon as  $V_{CC}$  drops below the POR threshold voltage, the device is reset and stops responding to any instruction sent to it.

#### 2.6.4 Power-down conditions

During power-down (continuous decay of  $V_{CC}$ ), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal Write cycle in progress).

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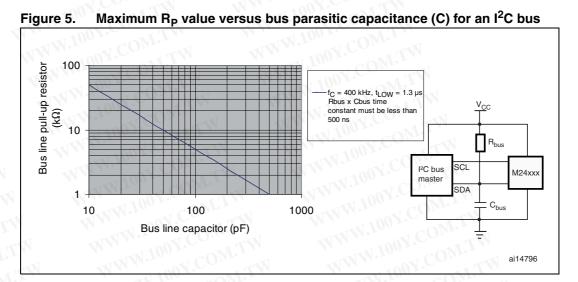


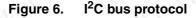
Signal description

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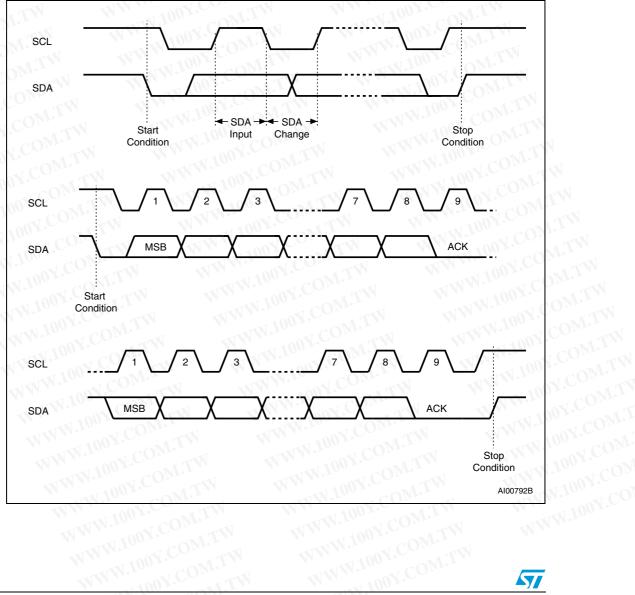
M24128, M24C64, M24C32

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#### Table 3. **Device select code**

Table 3. Device	select co	de	WW.	J.V.	001.	N			
WWW.100 Y.COM	Device type identifier <sup>(1)</sup>				Chip Enable address <sup>(2)</sup>			RW	
	b7	b6	b5	b4	b3	b2	b1	b0	
Device select code	Dia	0	A.M.	0	E2	E1	E0	RW	

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2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 4.	Address most significant byte	
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Address most significant byte									
b14	b13	b12	b11	b10	b9	b8			

	Addice	so icast sigi	inicant bytt				
b7	b6	b5	b4	b3	b2	b1	b0
-W	WWW	V.IUV N.CC	WT.	N	WW.100	N.COM	WT
			INK HE	는 11 원	886-3-575	2170	

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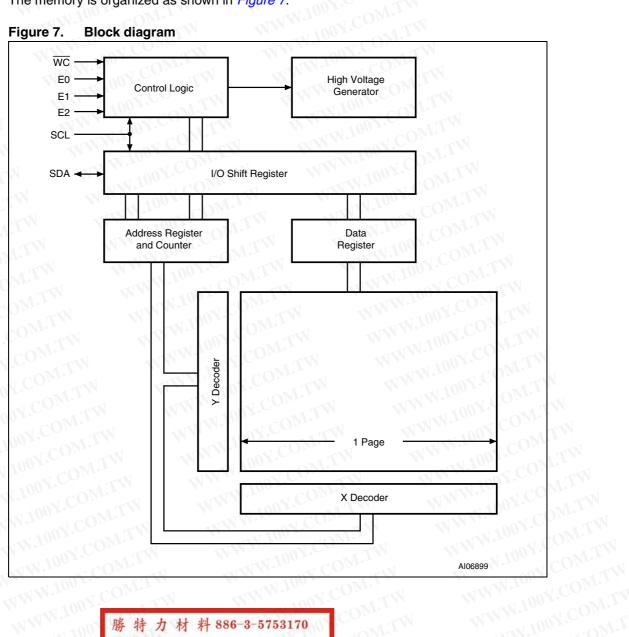
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# **Memory organization**

W.100Y.COM. The memory is organized as shown in *Figure 7*.





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# **Device operation**

The device supports the I<sup>2</sup>C protocol. This is summarized in *Figure 6*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24C32, M24C64 and M24128 devices are always slaves in all communications.

## 4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

## 4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

## 4.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9<sup>th</sup> clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

## 4.4 Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

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#### 4.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in Table 3 (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit device type identifier is 1010b.

Up to eight memory devices can be connected on a single I<sup>2</sup>C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The  $8^{th}$  bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9<sup>th</sup> bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Mode	RW bit	WC <sup>(1)</sup>	Bytes	Initial sequence	
Current Address Read	1	x	DX.COHLTW	Start, device select, $\overline{RW} = 1$	
Random Address	0	Х	ONY.COMETY	Start, device select, $R\overline{W} = 0$ , Address	
Read Random Address Read Sequential Read	1	X	TIONY.COM	reStart, device select, $R\overline{W} = 1$	
Sequential Read	1	x	≥1	Similar to Current or Random Address Read	
Byte Write	0	VIL	W.1001. CON	Start, device select, $\overline{RW} = 0$	
Page Write	0 V <sub>IL</sub>		≤ 32 for M24C64 and M24C32	Start, device select, $R\overline{W} = 0$	
			≤ 64 for M24128		

Table 6. **Operating modes** 

1.  $X = V_{IH} \text{ or } V_{IL}$ . WWW.100Y.COM.TW

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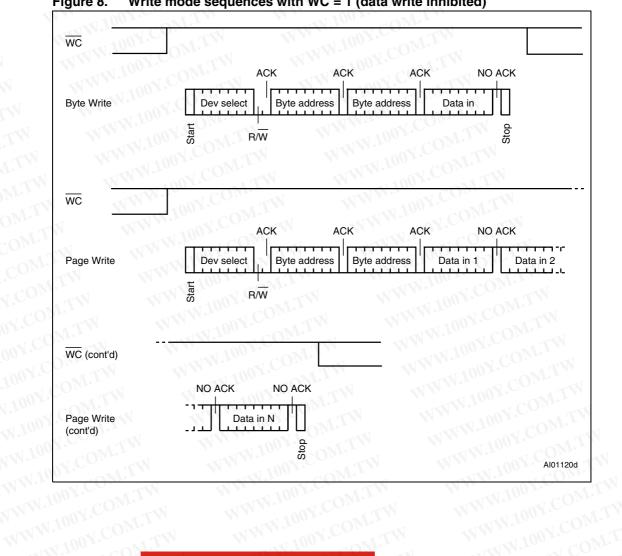
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Write mode sequences with  $\overline{WC} = 1$  (data write inhibited) Figure 8.

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## 4.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/Write bit (RW) reset to 0. The device acknowledges this, as shown in *Figure 9*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data Byte.

Writing to the memory may be inhibited if Write Control ( $\overline{WC}$ ) is driven high. Any Write instruction with Write Control ( $\overline{WC}$ ) driven high (during a period of time from the Start condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in *Figure 8*.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (*Table 4*) is sent first, followed by the Least Significant Byte (*Table 5*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10<sup>th</sup> bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay  $t_W$ , and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

## Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ( $\overline{WC}$ ) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 9*.

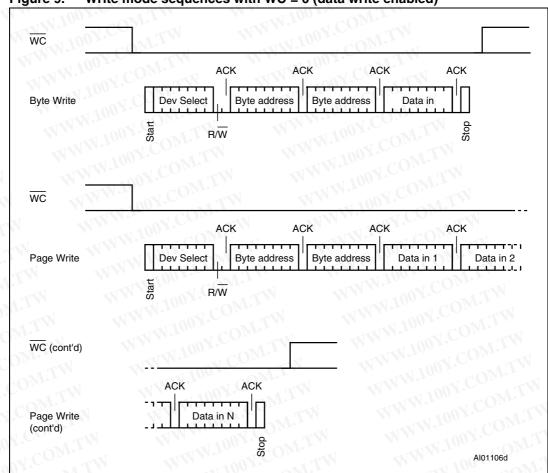
## 4.8 Page Write

The Page Write mode allows up to 32 bytes (for the M24C32 and M24C64) or 64 bytes (for the M24128) to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b13-b6 for M24128, b12-b5 for M24C64, and b11-b5 for M24C32) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 32 bytes of data (for the M24C32 and M24C64) or 64 bytes of data (for the M24128), each of which is acknowledged by the device if Write Control ( $\overline{WC}$ ) is low. If Write Control ( $\overline{WC}$ ) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (inside the page) is incremented. The transfer is terminated by the bus master generating a Stop condition.

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## 4.9 ECC (error correction code) and write cycling

The M24128 and M24C64 in UFDFPN8 (MLP)  $2 \times 3$  mm package and the M24128 in WLCSP package offer an ECC (error correction code) logic which compares each 4-byte word with its six associated EEPROM ECC bits. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

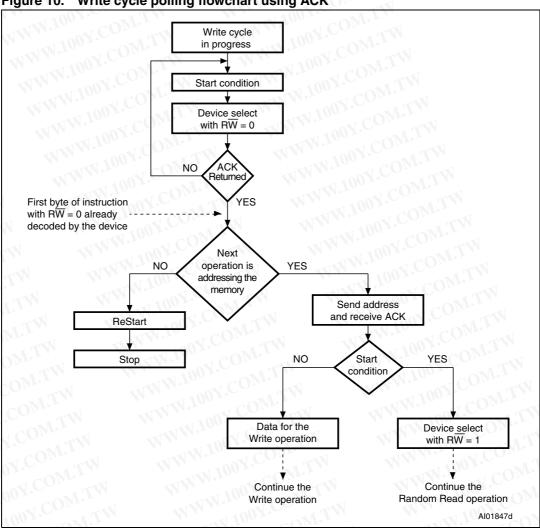
Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC word), that is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write by packets of 4 bytes in order to benefit from the larger amount of write cycles.

All M24C32, M24C64 and M24128 devices are qualified at 1 million (1 000 000) write cycles; the M24128 and M24C64 in UFDFPN8 (MLP)  $2 \times 3$  mm package and the M24128 in WLCSP package are qualified (at 1 million write cycles), using a cycling routine that writes to the device by multiples of 4-byte words.

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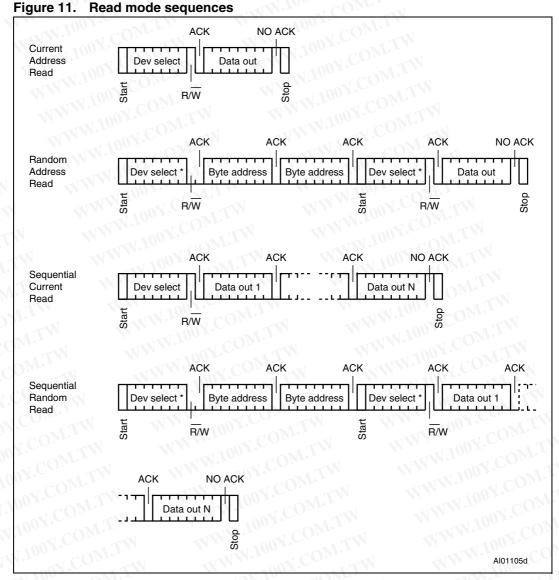
## 4.10 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time  $(t_w)$  is shown in *Table 17* and *Table 18*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 10*, is:

- 1. Initial condition: a Write cycle is in progress.
- 2. Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- 3. Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

#### **Device** operation



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WWW.100X.COM.TW WWW The seven most significant bits of the device select code of a Random Read (in the 1<sup>st</sup> and 4<sup>th</sup> bytes) must be identical.

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## 4.11 Read operations

Read operations are performed independently of the state of the Write Control ( $\overline{WC}$ ) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

## 4.12 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 11*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/Write bit (RW) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

## 4.13 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/Write bit (RW) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 11*, *without* acknowledging the Byte.

## 4.14 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 11*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

## 4.15 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9<sup>th</sup> bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

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**Initial delivery state** 5

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

## Maximum rating

Stressing the device outside the ratings listed in Table 7 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Symbol	Parameter	Min.	Max.	Unit
T <sub>A</sub>	Ambient operating temperature	-40	130	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C
OVI.TW	Lead temperature during soldering	see n	ote <sup>(1)</sup>	°C
T <sub>LEAD</sub>	PDIP-specific lead temperature during soldering	WW.10	260 <sup>(2)</sup>	°C
V <sub>IO</sub>	Input or output range	-0.50	6.5	V
V <sub>CC</sub>	Supply voltage	-0.50	6.5	V
V <sub>ESD</sub>	Electrostatic discharge voltage (human body model) <sup>(3)</sup>	-4000	4000	V

Table 7. Absolute maximum ratings

Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

2.  $T_{LEAD}$  max must not be applied for more than 10 s.

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W.100Y.COM. WWW.100Y.COM.TW 3. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500 Ω, R2=500 Ω)

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## **DC and AC parameters**

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This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

#### Table 8. Operating conditions (M24xxx-W)

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply voltage	2.5	5.5	V
Ŧ	Ambient operating temperature (device grade 6)	-40	85	°C
T <sub>A</sub>	Ambient operating temperature (device grade 3)	-40	125	°C

#### Table 9. **Operating conditions (M24xxx-R)**

				Unit
cc s	Supply voltage	1.8	5.5	V
Γ <sub>A</sub> A	Ambient operating temperature	-40	85	°C
	00			

#### Table 10. **Operating conditions (M24xxx-F)**

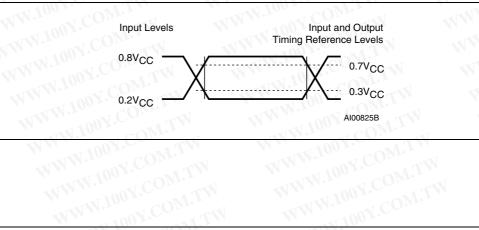
Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply voltage	1.7	5.5	COV.
M. TOM	Ambient operating temperature (device grade 6)	-40	85	°C
TA	Ambient operating temperature (device grade 5)	-20	85	°C

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Symbol	Parameter	Min.	Max.	Unit
CL	Load capacitance	1	00	pF
1.1001.	Input rise and fall times	1.1	50	ns
W.1001	Input levels	0.2V <sub>CC</sub> 1	to 0.8V <sub>CC</sub>	V
100	Input and output timing reference levels	0.3V <sub>CC</sub> t	to 0.7V <sub>CC</sub>	V.V

#### Figure 12. AC test measurement I/O waveform

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able 12.	Input parameters	WW.Inc COM	IIm	-	
Symbol	Parameter	Test condition	Min.	Max.	Unit
CIN	Input capacitance (SDA)	WWW.POON.CO	WT	8	pF
C <sub>IN</sub>	Input capacitance (other pins)	WWW.ICONY.C	DIVI. TV	6	pF
Z <sub>WCL</sub> <sup>(1)</sup>	WC input impedance	$V_{IN} < 0.3 V_{CC}$	50	200	kΩ
Z <sub>WCH</sub> <sup>(1)</sup>	WC input impedance	$V_{IN} > 0.7V_{CC}$	500	W.	kΩ
t <sub>NS</sub> <sup>(1)</sup>	Pulse width ignored (Input filter on SCL and SDA)	WWW.100	K.COM.	200	ns

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Table 12. Input parameters

Symbol	Parameter	Test condition (in addition to those in <i>Table 8</i> )	Min.	Max.	ι
TVILI	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or $V_{CC}$ device in Standby mode	Y.COA	±2	ŀ
I <sub>LO</sub>	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: Vss or Vcc	00Y.C	± 2	Įμ
Icc	Supply current (Read)	$2.5 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}, \text{ f}_{\text{c}} = 400 \text{ kHz}$	1001.	2	m
I <sub>CC0</sub>	Supply current (Write)	During t <sub>W</sub> , 2.5 V < V <sub>CC</sub> < 5.5 V	100Y	5 <sup>(1)</sup>	m
CON1.1	Standby supply current	$V_{IN} = V_{SS} \text{ or } V_{CC},$ $V_{CC} = 5.5 \text{ V}$	W.100	5	μ
I <sub>CC1</sub>	Standby supply current	$V_{IN} = V_{SS} \text{ or } V_{CC},$ $V_{CC} = 2.5 \text{ V}$	VW.10	2	μ
V <sub>IL</sub>	Input low voltage (SDA, SCL, $\overline{WC}$ )	N.100Y.COM.TW	-0.45	0.3V <sub>CC</sub>	<b>0</b> 1
ViH	Input high voltage (SDA, SCL, WC)	N.100Y.COM.TW	0.7V <sub>CC</sub>	V <sub>CC</sub> +0.6	
V <sub>OL</sub>	Output low voltage	$I_{OL} = 2.1 \text{ mA}, V_{CC} = 2.5 \text{ V or}$ $I_{OL} = 3 \text{ mA}, V_{CC} = 5.5 \text{ V}$	WY	0.4	V

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Symbol	Parameter	Test condition (in addition to those in <i>Table 8</i> )	Min.	Max.	Unit
luvy	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or $V_{CC}$ device in Standby mode	C.M.	± 2	μA
I <sub>LO</sub>	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: Vss or Vcc	WT.	± 2	μA
I <sub>CC</sub>	Supply current (Read)	$2.5 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}, \text{ f}_{\text{c}} = 400 \text{ kHz}$	1.1	2	mA
I <sub>CC0</sub>	Supply current (Write)	During t <sub>W</sub> , 2.5 V < V <sub>CC</sub> < 5.5 V	M. I	5 <sup>(1)</sup>	mA
I <sub>CC1</sub>	Standby supply current	$V_{IN} = V_{SS} \text{ or } V_{CC},$ 2.5 V < $V_{CC}$ < 5.5 V	OM.1	🔨 10	μA
V <sub>IL</sub>	Input low voltage (SDA, SCL, WC)	TW WWW.100X	-0.45	0.3V <sub>CC</sub>	V
V <sub>IH</sub>	Input high voltage (SDA, SCL, WC)	M.TW WWW.100	0.7V <sub>CC</sub>	V <sub>CC</sub> +0.6	V
V <sub>OL</sub>	Output low voltage	$I_{OL} = 2.1 \text{ mA}, V_{CC} = 2.5 \text{ V or}$ $I_{OL} = 3 \text{ mA}, V_{CC} = 5.5 \text{ V}$	ox.C	0.4	V

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able 14.	DC characteristics	s (M24xxx-W, device grade 3	3)

DC characteristics (M24xxx-R - device grade 6)

.doM	Input leakage current (SCL, SDA, E2, E1, E0)	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub> device in Standby mode	WW.10	± 2	μA
I <sub>LO</sub>	Output leakage current	SDA Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$	NWW.	± 2	μA
I <sub>CC</sub>	Supply current (Read)	$V_{CC} = 1.8 \text{ V}, \text{ f}_{c} = 400 \text{ kHz}$	WWW	0.8	mA
I <sub>CC0</sub>	Supply current (Write)	During t <sub>W</sub> , 1.8 V < V <sub>CC</sub> < 2.5 V	WW	3 <sup>(1)</sup>	mA
I <sub>CC1</sub>	Standby supply current	$V_{IN} = V_{SS} \text{ or } V_{CC},$ 1.8 V < $V_{CC}$ < 2.5 V	MA	1.100 1.100	μA
-1100	Input low voltage (SDA,	1.8 V ≤V <sub>CC</sub> < 2.5 V	-0.45	0.25 V <sub>CC</sub>	v
V <sub>IL</sub>	SCL, WC)	2.5 V ≤V <sub>CC</sub> < 5.5 V	-0.45	0.3 V <sub>CC</sub>	V
V	Input high voltage (SDA,	1.8 V ≤V <sub>CC</sub> < 2.5 V	$0.75V_{CC}$	V <sub>CC</sub> +1	V
V <sub>IH</sub>	SCL, WC)	2.5 V ≤V <sub>CC</sub> < 5.5 V	0.7V <sub>CC</sub>	V <sub>CC</sub> +1	V
VOL	Output low voltage	$I_{OL} = 1 \text{ mA}, V_{CC} = 1.8 \text{ V}$	N	0.2	V

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Symbol	Parameter	Test condition (in addition to those in <i>Table 10</i> )	Min.	Max.	Uni
I <sub>LI</sub>	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or $V_{CC}$ device in Standby mode	LM	± 2	μA
I <sub>LO</sub>	Output leakage current	SDA Hi-Z, external voltage applied on SDA: $V_{SS}$ or Vcc	WT.N	± 2	μA
I <sub>CC</sub> 🔨	Supply current (Read)	$V_{CC} = 1.7 \text{ V}, \text{ f}_{c} = 400 \text{ kHz}$	MT.IM	0.8	mA
I <sub>CC0</sub>	Supply current (Write)	During t <sub>W</sub> , 1.7 V < V <sub>CC</sub> < 2.5 V	OM.TY	3 <sup>(2)</sup>	mA
√ I <sub>CC1</sub>	Standby supply current	$V_{IN} = V_{SS} \text{ or } V_{CC},$ 1.7 V < V <sub>CC</sub> < 2.5 V	COM	CW 1	μA
	Input low voltage (SDA, SCL,	1.8 V ≤V <sub>CC</sub> < 2.5 V	-0.45	0.25 V <sub>CC</sub>	V
V <sub>IL</sub>	WC)	2.5 V ≤V <sub>CC</sub> < 5.5 V	-0.45	0.3 V <sub>CC</sub>	V
VIH	Input high voltage (SDA, SCL,	1.8 V ≤V <sub>CC</sub> < 2.5 V	0.75V <sub>CC</sub>	V <sub>CC</sub> +1	V
νн	WC)	2.5 V ≤V <sub>CC</sub> < 5.5 V	0.7V <sub>CC</sub>	V <sub>CC</sub> +1	V
WT .					v

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10X.CO DC characteristics (M24xxx-F)<sup>(1)</sup> Table 16.

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		Test conditions specified in <i>Table 8</i> and	Table 9		
Symbol	Alt.	Parameter	Min.	Max.	Unit
fc	f <sub>SCL</sub>	Clock frequency	WIM	400	kHz
t <sub>CHCL</sub>	t <sub>HIGH</sub>	Clock pulse width high	600	2	ns
t <sub>CLCH</sub>	t <sub>LOW</sub>	Clock pulse width low	1300	Z	ns
t <sub>XH1XH2</sub> <sup>(1)</sup>	t <sub>R</sub>	Input signal rise time	20	300	ns
t <sub>XL1XL2</sub> <sup>(1)</sup>	tF	Input signal fall time	20	300	ns
t <sub>DL1DL2</sub>	t <sub>F</sub>	SDA (out) fall time	20	100	ns
t <sub>DXCX</sub>	t <sub>SU:DAT</sub>	Data in set up time	100	WT	ns
t <sub>CLDX</sub>	t <sub>HD:DAT</sub>	Data in hold time	0	Mr. W	ns
t <sub>CLQX</sub>	t <sub>DH</sub>	Data out hold time 200		ON.	ns
t <sub>CLQV</sub> (2)(3)	t <sub>AA</sub>	Clock low to next data valid (access time)	200	900	ns
t <sub>CHDX</sub> <sup>(4)</sup>	t <sub>SU:STA</sub>	Start condition set up time		COM.	ns
t <sub>DLCL</sub>	t <sub>HD:STA</sub>	Start condition hold time	600	TCOM	ns
t <sub>CHDH</sub>	t <sub>SU:STO</sub>	Stop condition set up time	600	1 COV	ns
t <sub>DHDL</sub>		Time between Stop condition and next Start condition	1300	001.CO	ns
tw	N	Write time	MMM.	5 <sup>(5)</sup>	ms

#### Table 17 AC characteristics (M24xxx-W6\_M24xxW3\_M24xxB6)

1. Values recommended by the I<sup>2</sup>C-bus Fast-Mode specification.

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2. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

 $t_{CLQV}$  is the time (from the falling edge of SCL) required by the SDA bus line to reach 0.8V<sub>CC</sub> in a compatible way with the I<sup>2</sup>C specification (which specifies  $t_{SU:DAT}$  (min) = 100 ns), assuming that the R<sub>bus</sub> × C<sub>bus</sub> time constant is less than 500 ns (as specified in *Figure 5*). 3. OM.TW

For a reStart condition, or following a Write cycle. 4.

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WWW.100Y.COM.TW For production lots assembled from 1st July 2007 (data code 727: week27, year 2007), the M24xxx-R 5 WWW.100Y.COM.TW (1.8 V to 5.5 V range) memories are specified with tw = 5 ms (instead of 10ms).

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Test conditions specified in <i>Table 10</i>										
Symbol	Alt.	Parameter	Min.	Max.	Unit					
fc	f <sub>SCL</sub>	Clock frequency	WIN	400	kHz					
t <sub>CHCL</sub>	t <sub>HIGH</sub>	Clock pulse width high		V	ns					
t <sub>CLCH</sub>	t <sub>LOW</sub>	Clock pulse width low	1300	Z	ns					
t <sub>XH1XH2</sub> <sup>(1)</sup>	t <sub>R</sub>	Input signal rise time	20	300	ns					
t <sub>XL1XL2</sub> <sup>(1)</sup>	t <sub>F</sub>	Input signal fall time	20	300	ns					
t <sub>DL1DL2</sub>	t <sub>F</sub>	SDA (out) fall time	20	100	ns					
t <sub>DXCX</sub>	t <sub>SU:DAT</sub>	Data in set up time	100	Wn	ns					
t <sub>CLDX</sub>	t <sub>HD:DAT</sub>	Data in hold time	0	Mr. TM	ns					
t <sub>CLQX</sub>	t <sub>DH</sub>	Data out hold time	200	ON	ns					
t <sub>CLQV</sub> <sup>(2)(3)</sup>	t <sub>AA</sub>	Clock low to next data valid (access time)	200	900	ns					
t <sub>CHDX</sub> <sup>(4)</sup>	t <sub>SU:STA</sub>	Start condition set up time	600	1 COM. 1	ns					
t <sub>DLCL</sub>	t <sub>HD:STA</sub>	Start condition hold time	600	COM	ns					
t <sub>CHDH</sub>	t <sub>SU:STO</sub>	Stop condition set up time	600	TCON	ns					
t <sub>DHDL</sub>	t <sub>BUF</sub>	Time between Stop condition and next Start condition	1300	001.CO	ns					
tw		Write time	WWW.	10 <sup>(5)</sup>	ms					

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1. Values recommended by the I<sup>2</sup>C-bus Fast-Mode specification.

2. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

 $t_{CLQV}$  is the time (from the falling edge of SCL) required by the SDA bus line to reach 0.8V<sub>CC</sub> in a compatible way with the I<sup>2</sup>C specification (which specifies  $t_{SU:DAT}$  (min) = 100 ns), assuming that the R<sub>bus</sub> × C<sub>bus</sub> time constant is less than 500 ns (as specified in *Figure 5*). 3. WW.100Y.COM.TW

For a reStart condition, or following a Write cycle. 4. 100X.COM.TW

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For temperature range 6:  $t_{W(max)} = 5 \text{ ms.}$ 5. For temperature range 5:  $t_{W(max)} = 10$  ms.

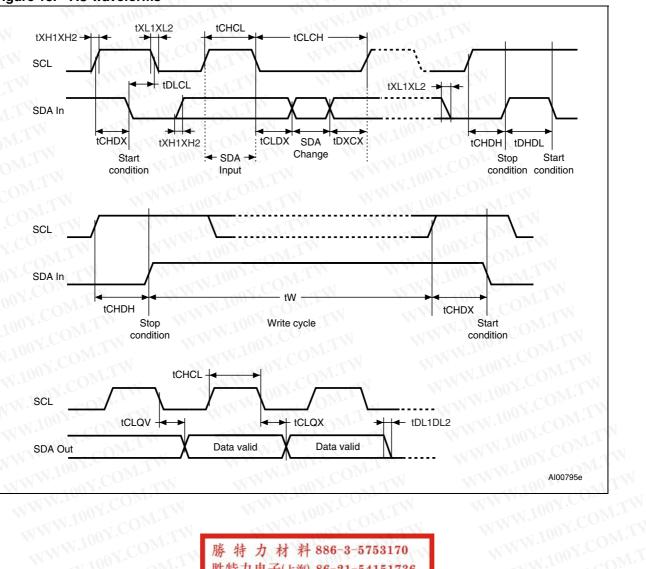
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#### **DC and AC parameters**

M24128, M24C64, M24C32



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#### Figure 13. AC waveforms

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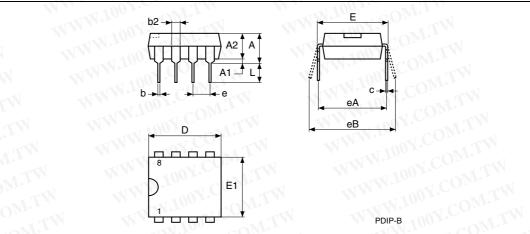
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## 8

# Package mechanical data

In order to meet environmental requirements, ST offers the M24C32, M24C64 and M24128 in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.



#### Figure 14. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package outline

### 1. Drawing is not to scale.

Max	inches <sup>(1)</sup>	Turn	Max	millimeters	Tun	Symbol
Max	Min.	Тур.	Max.	Min.	Тур.	COM.
0.209	WWW.	Wn	5.33	WWW.	The second se	A
. Los	0.0150	W.T.	IN COL	0.38		A1
0.194	0.1150	0.1299	4.95	2.92	3.30	A2
0.022	0.0142	0.0181	0.56	0.36	0.46	b
0.070	0.0449	0.0598	1.78	1.14	1.52	b2
0.014	0.0079	0.0098	0.36	0.20	0.25	C 00 7.
0.400	0.3551	0.3650	10.16	9.02	9.27	D 1001
0.325	0.3000	0.3098	8.26	7.62	7.87	Ex 100
0.279	0.2402	0.2500	7.11	6.10	6.35	E1 10
	T.T.	0.1000	WM I	TW-	2.54	е
N	M.T.M	0.3000	W.W.	NTN_	7.62	eA
0.429	WI.IW	100Y.CC	10.92	WIN	100Y.CO	eB
0.150	0.1150	0.1299	3.81	2.92	3.30	LAWY

#### PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package mechanical data



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#### Package mechanical data

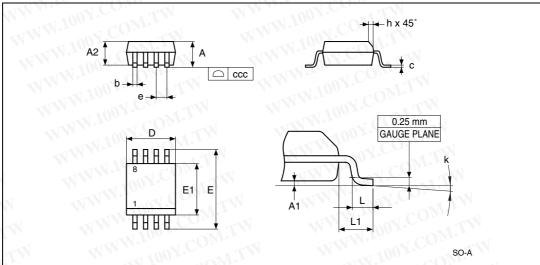
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SO8 narrow - 8 lead plastic small outline, 150 mils body width, package Figure 15. outline



1. Drawing is	s not to scale.	
Table 20.	SO8 narrow – 8 lead plastic small ou package mechanical data	utline, 150 mils body width,

Symbol	MM	millimeters	WT.Mo	d	inches <sup>(1)</sup>	M.TV
Cymbol	Тур	Min	Max	Тур	Min	Max
Α		100×	1.75	N.	W.1001	0.0689
A1	1 1	0.10	0.25		0.0039	0.0098
A2	TN I	1.25	DY.COM!	1 M	0.0492	N.CON
0.Y.b	TW	0.28	0.48	TW.	0.0110	0.0189
100XcCO	WILL	0.17	0.23	WT.I	0.0067	0.0091
ccc	WTD	MMM	0.10	WLIN	WW	0.0039
D	4.90	4.80	5.00	0.1929	0.1890	0.1969
Env.C	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	- 1	MM-2 001	0.0500		<u> 10</u>
Wh.	N.COM.	0.25	0.50	Y.COM.	N N	TAN.
k	N.COM.	0°	8°	N.COM.	~~ 0°	8°
TAN'I	COM.	0.40	1.27	N.COM.	0.0157	0.0500
L1	1.04		WW.	0.0410	N/m	WWW

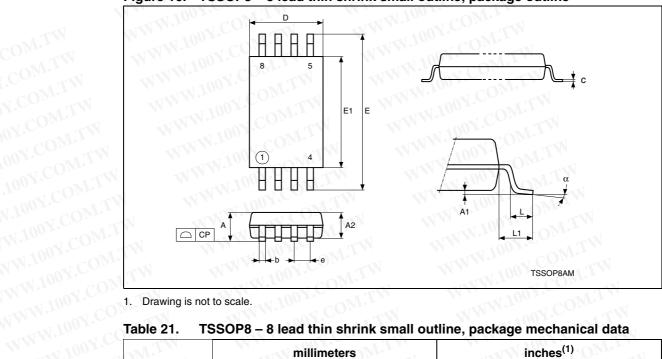
Values in inches are converted from mm and rounded to 4 decimal digits. WWW.100Y.COM.TW 1. WWW.100Y.COM.

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TSSOP8 - 8 lead thin shrink small outline, package outline Figure 16.

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T. Drawing is	s not to scale.		
Table 21.	TSSOP8 – 8 lead thin shrink small out	line, package mechanical d	ata

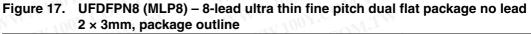
WILLINO	Тур.	Min.	Max.	Тур.	Min.	Max.
CO A	VW	N.I.	1.200	W	KUUT VA	0.0472
A1	N.	0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b).	N N	0.190	0.300	N/	0.0075	0.0118
c OV		0.090	0.200		0.0035	0.0079
CP		I.WW.	0.100		WW.	0.0039
100 D 001	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	<u>v</u>	1.100 <u>1</u> .CO	0.0256	-	N.100 - C
ILEY.	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
4007.	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1 001	1.000	1	W.100	0.0394		W.10
α	T.M.	0°	8°	Y.COM.I	0°	8°

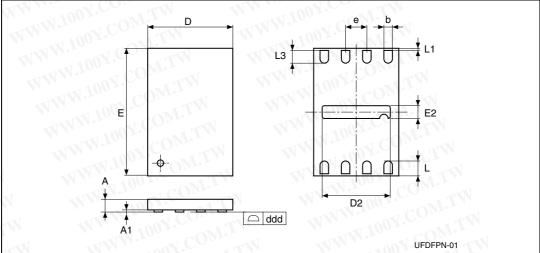
1. Values in inches are converted from mm and rounded to 4 decimal digits. WWW.100Y.CC 100Y.COM.TW WWW.100Y.COM.TW WWW.100Y.C

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1. Drawing is not to scale.

1. Drawing is	not to scale.
Table 22.	UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, package mechanical data

Symbol	Тур	Min	Max	Тур	Min	Max
A	0.55 🚿	0.50	0.60	0.0217	0.0197	0.023
A1	0.02	0.00	0.05	0.0008	0	0.0020
b	0.25	0.20	0.30	0.0098	0.0079	0.0118
D	2.00	1.90	2.10	0.0787	0.0748	0.0827
D2	1.60	1.50	1.70	0.0630	0.0591	0.0669
ddd	WT.	WWW	0.08	WTN	MMM	0.003
Ev CC	3.00	2.90	3.10	0.1181	0.1142	0.1220
E2	0.20	0.10	0.30	0.0079	0.0039	0.0118
e	0.50		NN.10	0.0197	- 11	N
AMTON Y	0.45	0.40	0.50	0.0177	0.0157	0.0197
WEI100 ;	CONT.		0.15	V.COM.	NX	0.005
L3	COM.1	0.30	WW.10	COM.	0.0118	WW.

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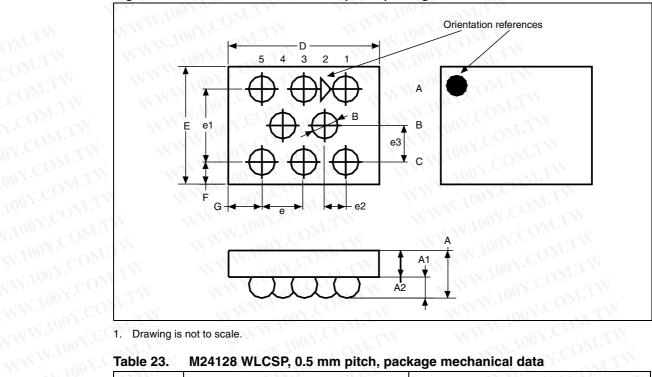


Figure 18. M24128 WLCSP, 0.5 mm pitch, package outline

M24128 WLCSP, 0.5 mm pitch, package mechanical data

Symbol		millimeters		W	inches <sup>(1)</sup>	
symbol	🕺 Тур. 🗹	Min.	Max.	Тур.	Min.	Max.
Α	0.585	0.535	0.635	0.0230	0.0211	0.0250
A1	0.230	0.205	0.255	0.0091	0.0081	0.0100
A2	0.355	0.330	0.380	0.0140	0.0130	0.0150
В	0.320	0.290	0.350	0.0126	0.0114	0.0138
D.CC	1.805	1.785	1.825	0.0711	0.0703	0.0719
EV.C	1.400	1.380	1.420	0.0551	0.0543	0.0559
е	0.5	W	Von.	0.0197	MM	100Y.
e1	0.886		WW.	0.0349	W	1005
e2	0.250	N N	WWW.	0.0098	N N	Q11.
e3	0.443	W	WWW.IC	0.0174	N N	NNN.
FN.LO	0.257	W	WWW.	0.0101	WT	WWW.
G	0.4025	N/m	WWW.	0.0158	Wn	MMM.
N <sup>(2)</sup>	100 x. COJ	8	WW	.100 V COV	8	WWW

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M24C32-

M24128, M24C64, M24C32

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# Part numbering

Table 24. Ordering information scheme

Example:

#### **Device type**

 $M24 = I^2C$  serial access EEPROM

#### **Device function**

128–B = 128 Kbit (16384 x 8) C64– = 64 Kbit (8192 x 8) C32– = 32 Kbit (4096 x 8)

#### **Operating voltage**

#### Package

BN = PDIP8 MN = SO8 (150 mil width) DW = TSSOP8 (169 mil width) MB = UFDFPN8 (MLP8) CS = WLCSP

#### **Device grade**

6 = Industrial: device tested with standard test flow over -40 to 85 °C

- 3 = Automotive: device tested with high reliability certified flow<sup>(1)</sup> over -40 to  $125^{\circ}$ C.
- 5 = Consumer: device tested with standard test flow over -20 to 85°C

#### Option

blank = standard packing

T = Tape and reel packing

#### Plating technology

P or  $G = ECOPACK^{\mathbb{R}}$  (RoHS compliant)

#### Process<sup>(2)</sup>

P = F6DP26% Chartered

A = F8L Rousset (only for the WLCSP package)

- 1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
- 2. Used only for device grade 3 and WLCSP packages.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Package	M24C32-F 1.7 V to 5.5 V	M24C32-R 1.8 V to 5.5 V	M24C32-W 2.5 V to 5.5 V
DIP8 (BN)	MITH - WI	W.1001. COM.1	Grade6
SO8N (MN)	DM.TW W	Grade 6	Grade 3 Grade 6
TSSOP8 (DW)	Grade 5	Grade 6	Grade 6
MLP8 (MB)	Grade 5	Grade 6	- WT

#### Table 25. Available M24C32 products (package, voltage range, temperature grade)

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TSSOP8 (DW)	Grade 5	Grade 6	Grade 6
MLP8 (MB)	Grade 5	Grade 6	- 117
Table 26. Availabl	e M24C64 products (p	ackage, voltage rang	e, temperature gra
Package	M24C64-F 1.7 V to 5.5 V	M24C64-R 1.8 V to 5.5 V	M24C64-W 2.5 V to 5.5 V
DIP8 (BN)	. Jow COM.	WWW.1001	Grade6
SO8N (MN)	VI00Y.COM.TW	Grade 6	Grade 3 Grade 6
TSSOP8 (DW)	Grade 5	Grade 6	Grade 6
MLP8 (MB)	Grade 6	Grade 6	MT. Frank

#### Available M24128 products (package, voltage range, temperature grade) Table 27.

DIP8 (BN)	WW 100X.C.	WI.IW - WI	W.1001. COM.
SO8N (MN)	WWW.100Y.C	Grade 6	Grade 3 Grade 6
TSSOP8 (DW)	WWW.Ioo	Grade 6	Grade 6
MLP8 (MB)	Grade 6	Grade 6	WWW.10
WLCSP (CS)	Grade 6	Grade 6	WW. IV

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#### **Revision history** 10

Revisi	on history	
Table 28.	Document revisio	n history

Date	Revision	Changes
22-Dec-1999	2.3	TSSOP8 package in place of TSSOP14 (pp 1, 2, OrderingInfo, PackageMechData).
28-Jun-2000	2.4	TSSOP8 package data corrected
31-Oct-2000	2.5	References to Temperature Range 3 removed from Ordering Inform Voltage range -S added, and range -R removed from text and table throughout.
20-Apr-2001	2.6	Lead Soldering Temperature in the Absolute Maximum Ratings tabl amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical d updated
16-Jan-2002	2.7	Test condition for I <sub>LI</sub> made more precise, and value of I <sub>LI</sub> for E2-E0 WC added -R voltage range added
02-Aug-2002	2.8	Document reformatted using new template. TSSOP8 (3x3mm <sup>2</sup> body size) package (MSOP8) added. 5ms write time offered for 5V and 2.5V devices
04-Feb-2003	2.9	SO8W package removedS voltage range removed
27-May-2003	2.10	TSSOP8 (3x3mm <sup>2</sup> body size) package (MSOP8) removed
22-Oct-2003	3.0	Table of contents, and Pb-free options added. Minor wording chang Summary Description, Power-On Reset, Memory Addressing, Write Operations, Read Operations. $V_{IL}$ (min) improved to -0.45V.
01-Jun-2004	4.0	Absolute Maximum Ratings for V <sub>IO</sub> (min) and V <sub>CC</sub> (min) improved. Soldering temperature information clarified for RoHS compliant dev Device Grade clarified
04-Nov-2004	5.0	Product List summary table added. Device Grade 3 added. 4.5-5.5 range is Not for New Design. Some minor wording changes. AEC-C 002 compliance. $t_{NS}(max)$ changed. $V_{IL}(min)$ is the same on all inpupins of the device. $Z_{WCL}$ changed.
05-Jan-2005	6.0	UFDFPN8 package added. Small text changes.

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#### Document revision history (continued) Table 28.

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Date	Revision	Changes
29-Jun-2006		Document converted to new ST template. M24C32 and M24C64 products (4.5 to 5.5V supply voltage) removed. M24C64 and M24C32 products (1.7 to 5.5V supply voltage) added. Section 2.3: Chip Enable (E0, E1, E2) and Section 2.4: Write Control (WC) modified, Section 2.6: Supply voltage ( $V_{CC}$ ) added and replaces Power On Reset: VCC Lock-Out Write Protect section. T <sub>A</sub> added, Note 1 updated and T <sub>LEAD</sub> specified for PDIP packages in Table 7: Absolute maximum ratings. I <sub>CC0</sub> added, I <sub>CC</sub> voltage conditions changed and I <sub>CC1</sub> specified over the whole voltage range in Table 13: DC characteristics (M24xxx-W, device grade 6). I <sub>CC0</sub> added, I <sub>CC</sub> frequency conditions changed and I <sub>CC1</sub> specified over the whole voltage range in Table 15: DC characteristics (M24xxx-R - device grade 6).
	WWW WWW WWW	t <sub>W</sub> modified in <i>Table 17: AC characteristics (M24xxx-W6, M24xxW3, M24xxR6)</i> . SO8N package specifications updated (see <i>Figure 15</i> and <i>Table 20</i> ). Device grade 5 added, B and P Process letters added to <i>Table 24: Ordering information scheme</i> . Small text changes.
03-Jul-2006	8	I <sub>CC1</sub> modified in <i>Table 13: DC characteristics (M24xxx-W, device grade 6)</i> . <i>Note 1</i> added to <i>Table 16: DC characteristics (M24xxx-F)</i> and table title modified.
17-Oct-2006	9	UFDFPN8 package specifications updated (see <i>Table 22</i> ). M24128-BW and M24128-BR part numbers added. Generic part number corrected in <i>Features on page 1</i> . I <sub>CC0</sub> corrected in <i>Table 14</i> and <i>Table 13</i> . Packages are ECOPACK® compliant.
27-Apr-2007	10	Available packages and temperature ranges by product specified in <i>Table 25, Table 26</i> and <i>Table 27.</i> Notes modified below <i>Table 12: Input parameters.</i> V <sub>IH</sub> max modified in DC characteristics tables (see <i>Table 13, Table 14, Table 15</i> and <i>Table 16</i> ). C process code added to <i>Table 24: Ordering information scheme.</i> For M24xxx-R (1.8 V to 5.5 V range) products assembled from July 2007 on, t <sub>W</sub> will be 5 ms (see <i>Table 17: AC characteristics (M24xxx-W6, M24xxW3, M24xxR6</i> ).
27-Nov-2007	x.COM ox.COM oottON 001100 1002.CC	<ul> <li>Small text changes. Section 2.5: V<sub>SS</sub> ground and Section 4.9: ECC (error correction code) and write cycling added.</li> <li>V<sub>IL</sub> and V<sub>IH</sub> modified in Table 15: DC characteristics (M24xxx-R - device grade 6).</li> <li>JEDEC standard reference updated below Table 7: Absolute maximum ratings.</li> <li>Package mechanical data inch values calculated from mm and rounded to 4 decimal digits (see Section 8: Package mechanical data).</li> </ul>



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Date	Revision	Changes
WWW.10 WWW.10 WWW WWW WWW	5X.COM 50Y.COM 100X.CO	Added Section 2.6.2: Power-up conditions, updated Section 2.6.3: Device reset, and Section 2.6.4: Power-down conditions in Section 2.6: Supply voltage ( $V_{CC}$ ). Updated Figure 5: Maximum $R_P$ value versus bus parasitic capacitance (C) for an I <sup>2</sup> C bus. Replace M24128 and M24C64 by M24128-BFMB6 and M24C64-FMB6, respectively, in Section 4.9: ECC (error correction code) and write cycling. Added temperature grade 6 in Table 10: Operating conditions (M24xxx- F). Updated test conditions for I <sub>LO</sub> and V <sub>LO</sub> in Table 13: DC characteristics
18-Dec-2007	12	( <i>M24xxx-W</i> , device grade 6), Table 14: DC characteristics ( <i>M24xxx-W</i> , device grade 3), and Table 15: DC characteristics ( <i>M24xxx-R</i> - device grade 6). Test condition updated for I <sub>LO</sub> , and V <sub>IH</sub> and V <sub>IL</sub> differentiate for 1.8 V $\leq$ V <sub>CC</sub> < 2.5 V and 2.5 V $\leq$ V <sub>CC</sub> < 5.5 V in Table 16: DC characteristics ( <i>M24xxx-F</i> ). Updated Table 17: AC characteristics ( <i>M24xxx-W6</i> , <i>M24xxW3</i> , <i>M24xxR6</i> ), and Table 18: AC characteristics ( <i>M24xxx-F</i> ). Updated Figure 13: AC waveforms. Added M24128-BF in Table 27: Available M24128 products (package, voltage range, temperature grade). Process B removed from Table 24: Ordering information scheme.
30-May-2008	13	Small text changes. C <i>Process</i> option and Blank <i>Plating technology</i> option removed from <i>Table 24: Ordering information scheme</i> .
15-Jul-2008	14	WLCSP package added (see Figure 3: M24128 WLCSP connections (top view, marking side, with balls on the underside) and Section 8: Package mechanical data). Section 4.9: ECC (error correction code) and write cycling updated.

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