M24128
M24C64 M24C32

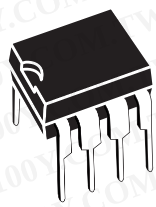
128 Kbit, 64 Kbit and 32 Kbit serial I²C bus EEPROM

Features

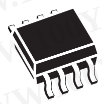
- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltages (see *Table 1* for root part numbers):
  - 2.5 V to 5.5 V
  - 1.8 V to 5.5 V
  - 1.7 V to 5.5 V
- Write Control input
- Byte and Page Write
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 Million write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

Table 1. Device summary

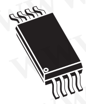
Reference	Part number	Supply voltage
M24128	M24128-BW	2.5 V to 5.5V
	M24128-BR	1.8 V to 5.5V
	M24128-BF	1.7 V to 5.5V
M24C64	M24C64-W	2.5 V to 5.5V
	M24C64-R	1.8 V to 5.5V
	M24C64-F	1.7 V to 5.5V
M24C32	M24C32-W	2.5 V to 5.5V
	M24C32-R	1.8 V to 5.5V
	M24C32-F	1.7 V to 5.5V



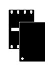
PDIP8 (BN)



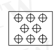
SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



UFDFPN8 (MB)
2 × 3 mm (MLP)



WLCSP (CS)

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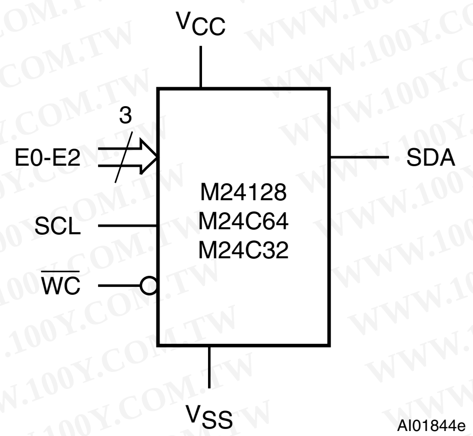
1 Description

The M24C32, M24C64 and M24128 devices are I^{2}C-compatible electrically erasable programmable memories (EEPROM). They are organized as 4096 × 8 bits, 8192 × 8 bits and 16384 × 8 bits, respectively.

Figure 1. Logic diagram



I^{2}C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^{2}C bus definition.

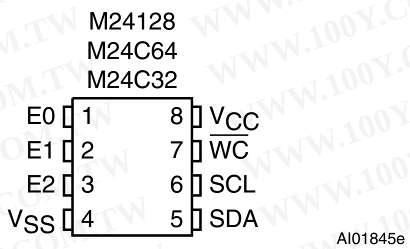
The device behaves as a slave in the I^{2}C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/$\overline{\text{Write}}$ bit ($R\overline{W}$) (as described in *Table 3*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 2. Signal names

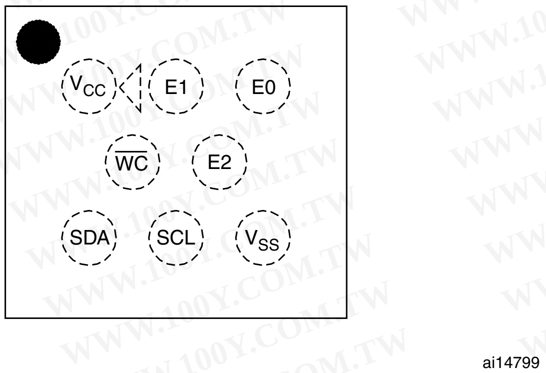
Signal name	Function	Direction
E0, E1, E2	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
WC	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. DIP, SO, TSSOP and UFDFPN connections



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Figure 3. M24128 WLCSP connections (top view, marking side, with balls on the underside)



2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

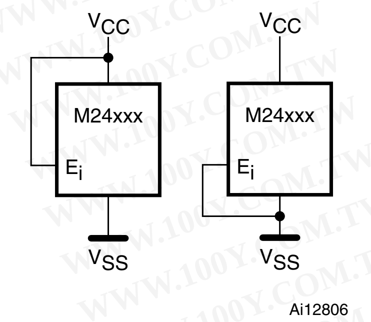
2.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 4*. When not connected (left floating), these inputs are read as low (0,0,0).

Figure 4. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven high, device select and Address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 9* and *Table 10*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

2.6.3 Device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 9* and *Table 10*). Until V_{CC} passes over the POR threshold, the device is reset and in Standby Power mode.

In a similar way, during power-down (continuous decay of V_{CC}), as soon as V_{CC} drops below the POR threshold voltage, the device is reset and stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal Write cycle in progress).

Figure 5. Maximum R_P value versus bus parasitic capacitance (C) for an I^2C bus

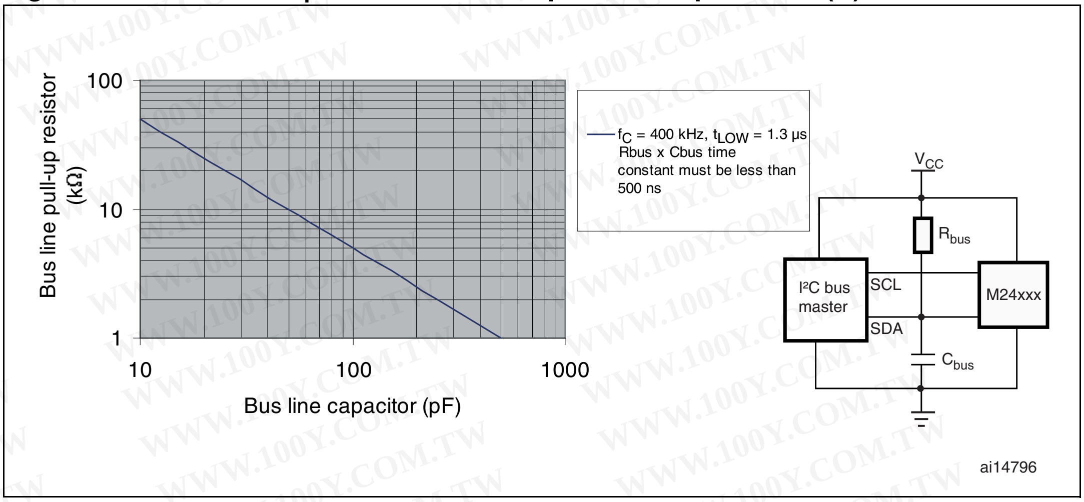


Figure 6. I^2C bus protocol

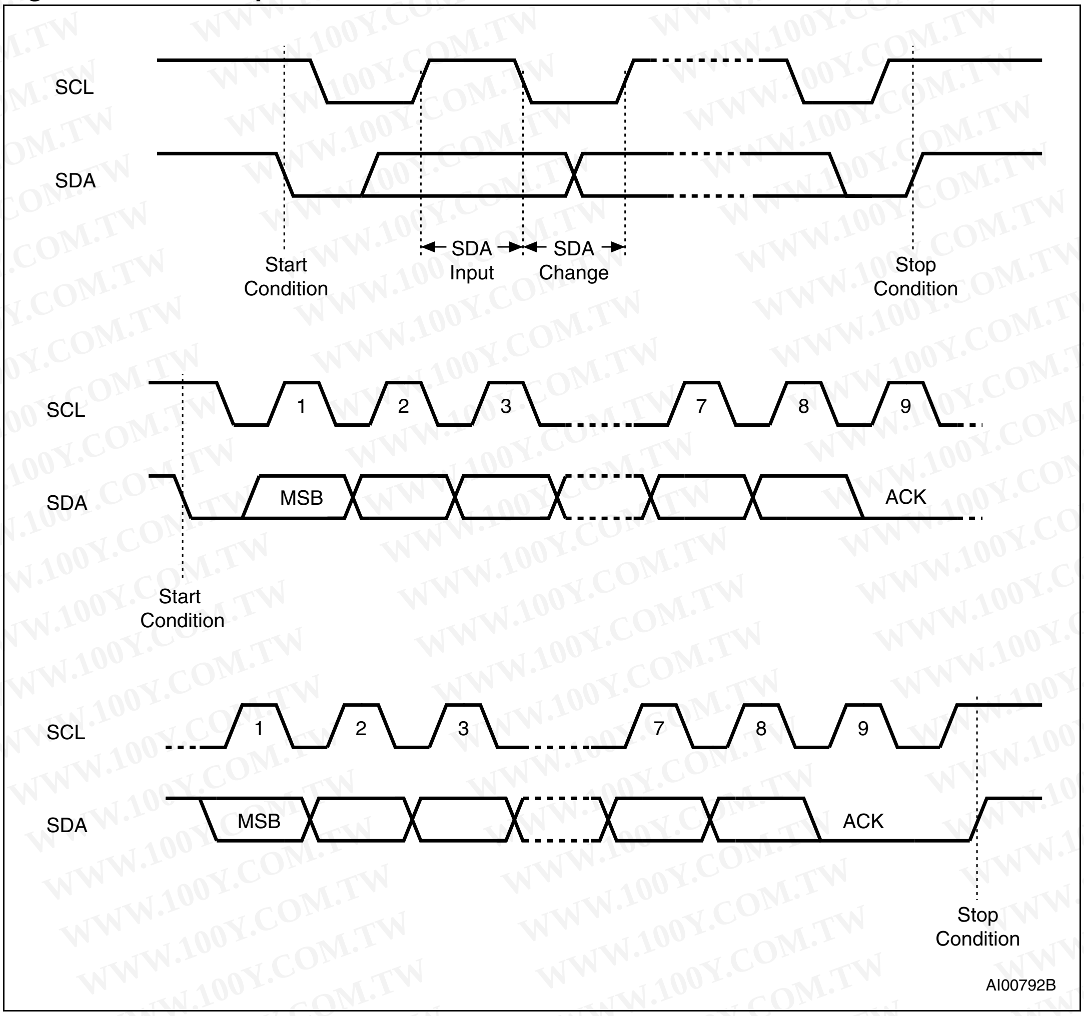


Table 3. Device select code

	Device type identifier(1)				Chip Enable address(2)			R$\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2	E1	E0	R$\overline{W}$

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 4. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

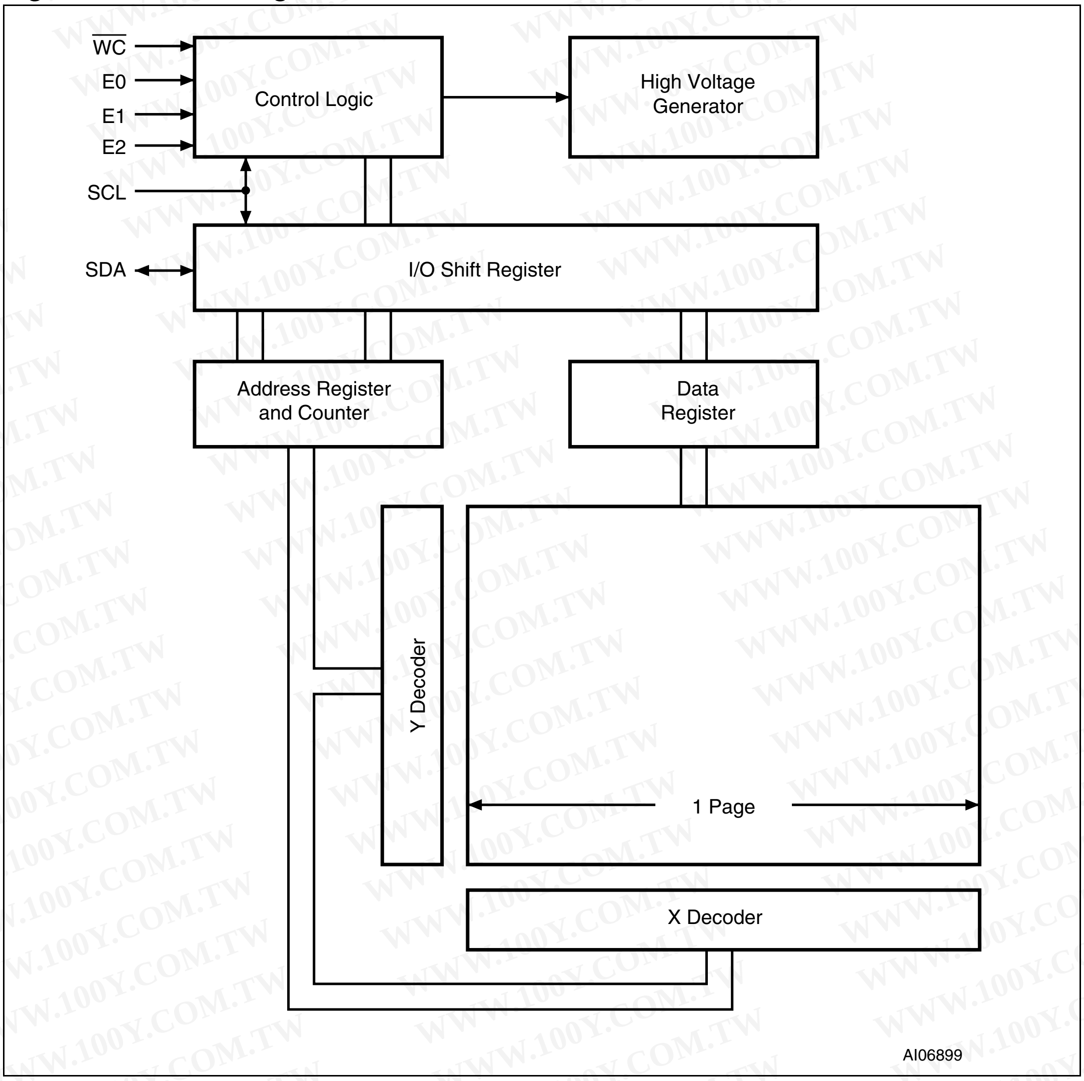
Table 5. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Memory organization

The memory is organized as shown in *Figure 7*.

Figure 7. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 6*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24C32, M24C64 and M24128 devices are always slaves in all communications.

4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

4.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.4 Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 3* (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit Chip Enable “Address” (E2, E1, E0). To address the memory array, the 4-bit device type identifier is 1010b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8^{th} bit is the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$). This bit is set to 1 for Read and 0 for Write operations.

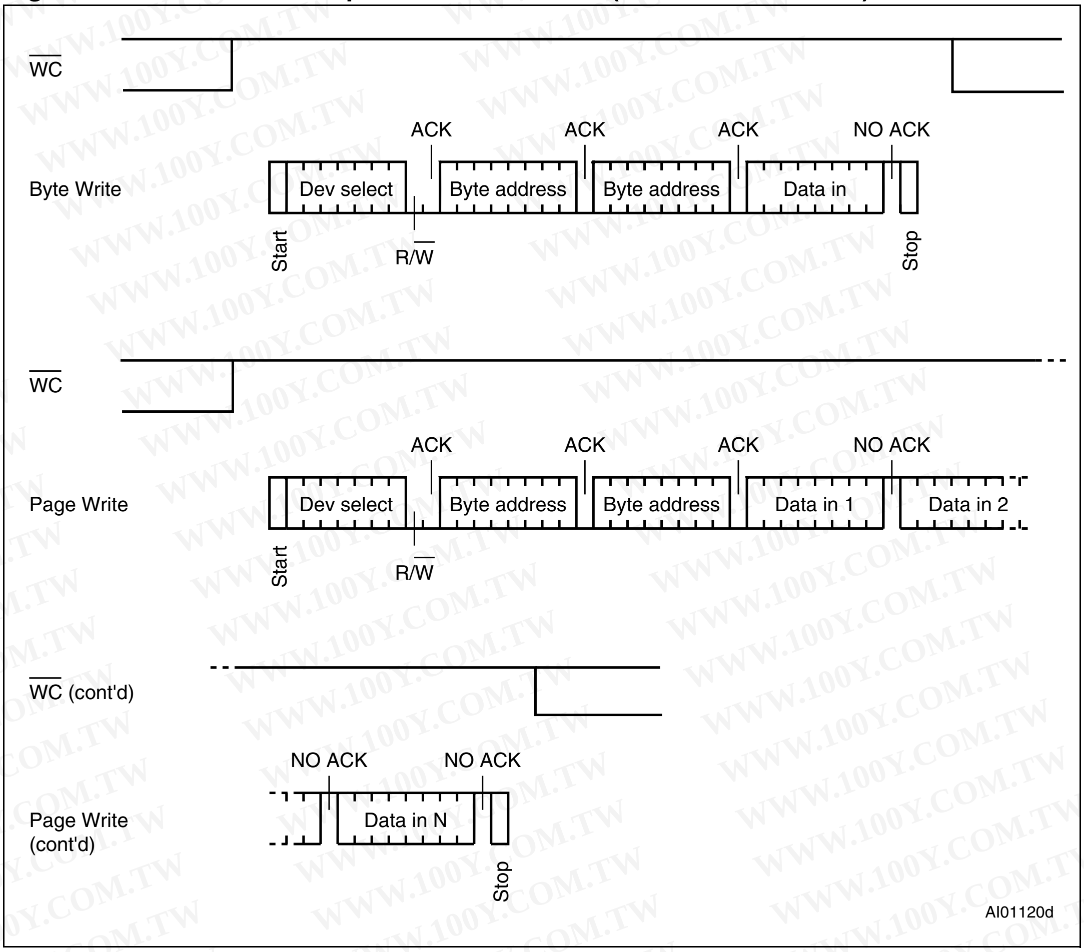
If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Table 6. Operating modes

Mode	R$\overline{\text{W}}$ bit	$\overline{\text{WC}}$[1]	Bytes	Initial sequence
Current Address Read	1	X	1	Start, device select, R$\overline{\text{W}}$ = 1
Random Address Read	0	X	1	Start, device select, R$\overline{\text{W}}$ = 0, Address
	1	X		reStart, device select, R$\overline{\text{W}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, device select, R$\overline{\text{W}}$ = 0
Page Write	0	V_{IL}	≤ 32 for M24C64 and M24C32	Start, device select, R$\overline{\text{W}}$ = 0
			≤ 64 for M24128	

1. X = V_{IH} or V_{IL}.

Figure 8. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



4.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) reset to 0. The device acknowledges this, as shown in *Figure 9*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data Byte.

Writing to the memory may be inhibited if Write Control ($\overline{\text{WC}}$) is driven high. Any Write instruction with Write Control ($\overline{\text{WC}}$) driven high (during a period of time from the Start condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in *Figure 8*.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (*Table 4*) is sent first, followed by the Least Significant Byte (*Table 5*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

4.7 Byte Write

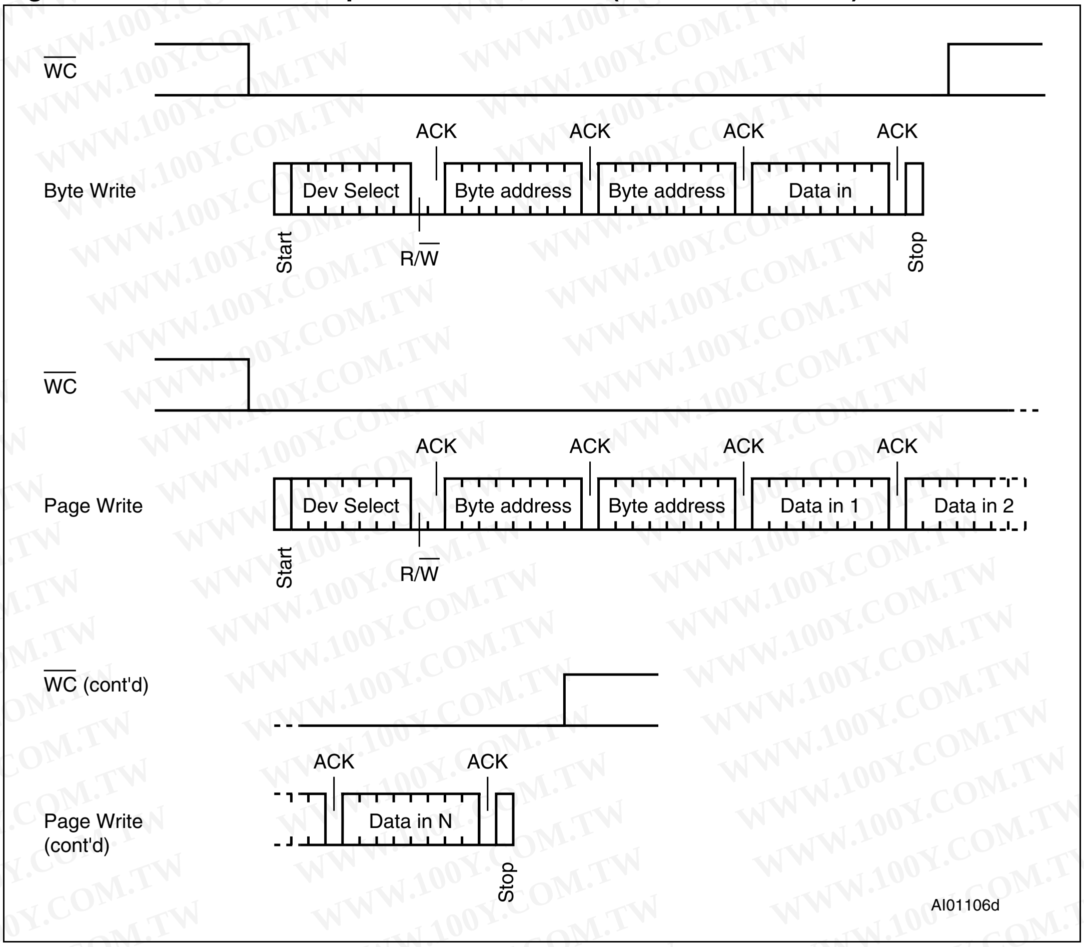
After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{\text{WC}}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 9*.

4.8 Page Write

The Page Write mode allows up to 32 bytes (for the M24C32 and M24C64) or 64 bytes (for the M24128) to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b13-b6 for M24128, b12-b5 for M24C64, and b11-b5 for M24C32) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 32 bytes of data (for the M24C32 and M24C64) or 64 bytes of data (for the M24128), each of which is acknowledged by the device if Write Control ($\overline{\text{WC}}$) is low. If Write Control ($\overline{\text{WC}}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (inside the page) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 9. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



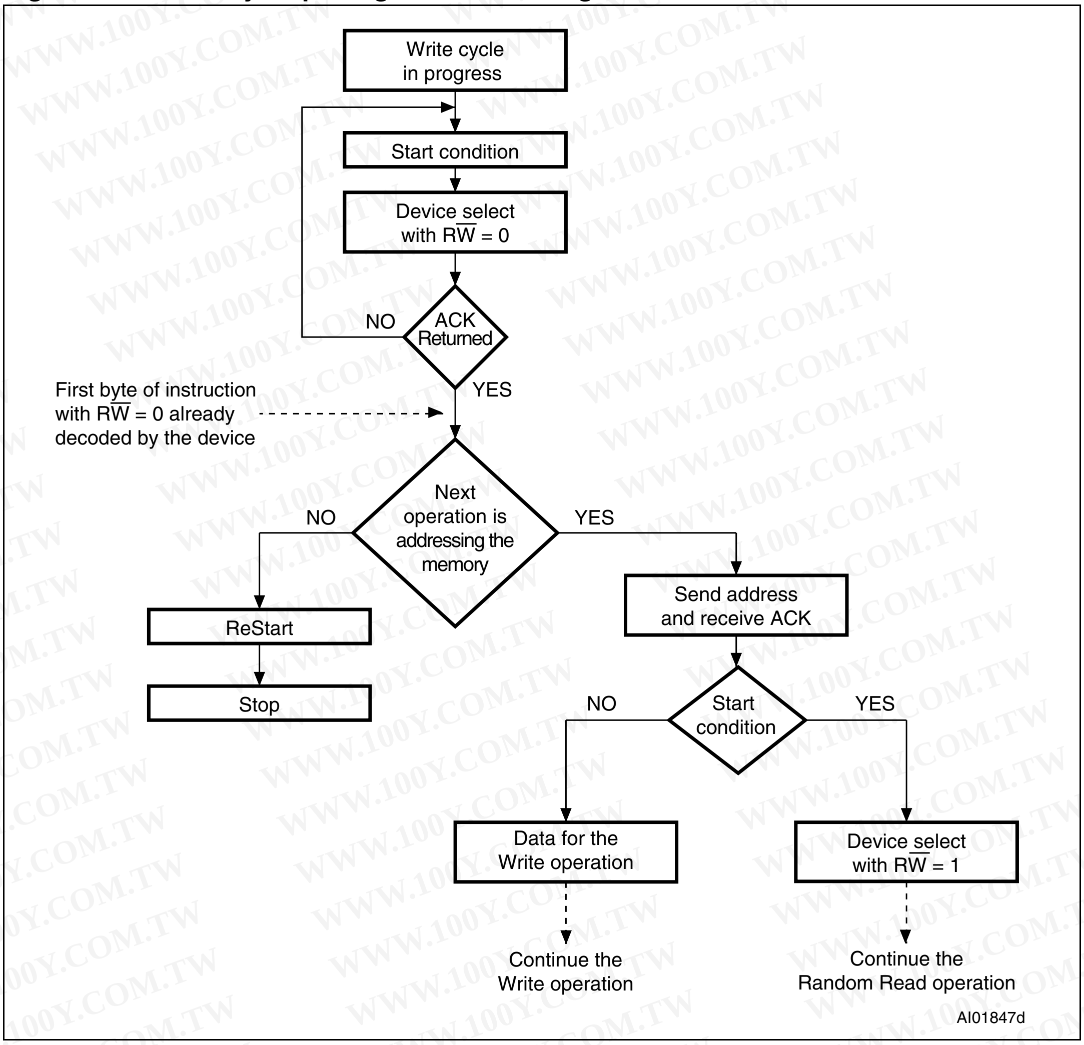
4.9 ECC (error correction code) and write cycling

The M24128 and M24C64 in UFDFPN8 (MLP) 2 × 3 mm package and the M24128 in WLCSP package offer an ECC (error correction code) logic which compares each 4-byte word with its six associated EEPROM ECC bits. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC word), that is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write by packets of 4 bytes in order to benefit from the larger amount of write cycles.

All M24C32, M24C64 and M24128 devices are qualified at 1 million (1 000 000) write cycles; the M24128 and M24C64 in UFDFPN8 (MLP) 2 × 3 mm package and the M24128 in WLCSP package are qualified (at 1 million write cycles), using a cycling routine that writes to the device by multiples of 4-byte words.

Figure 10. Write cycle polling flowchart using ACK



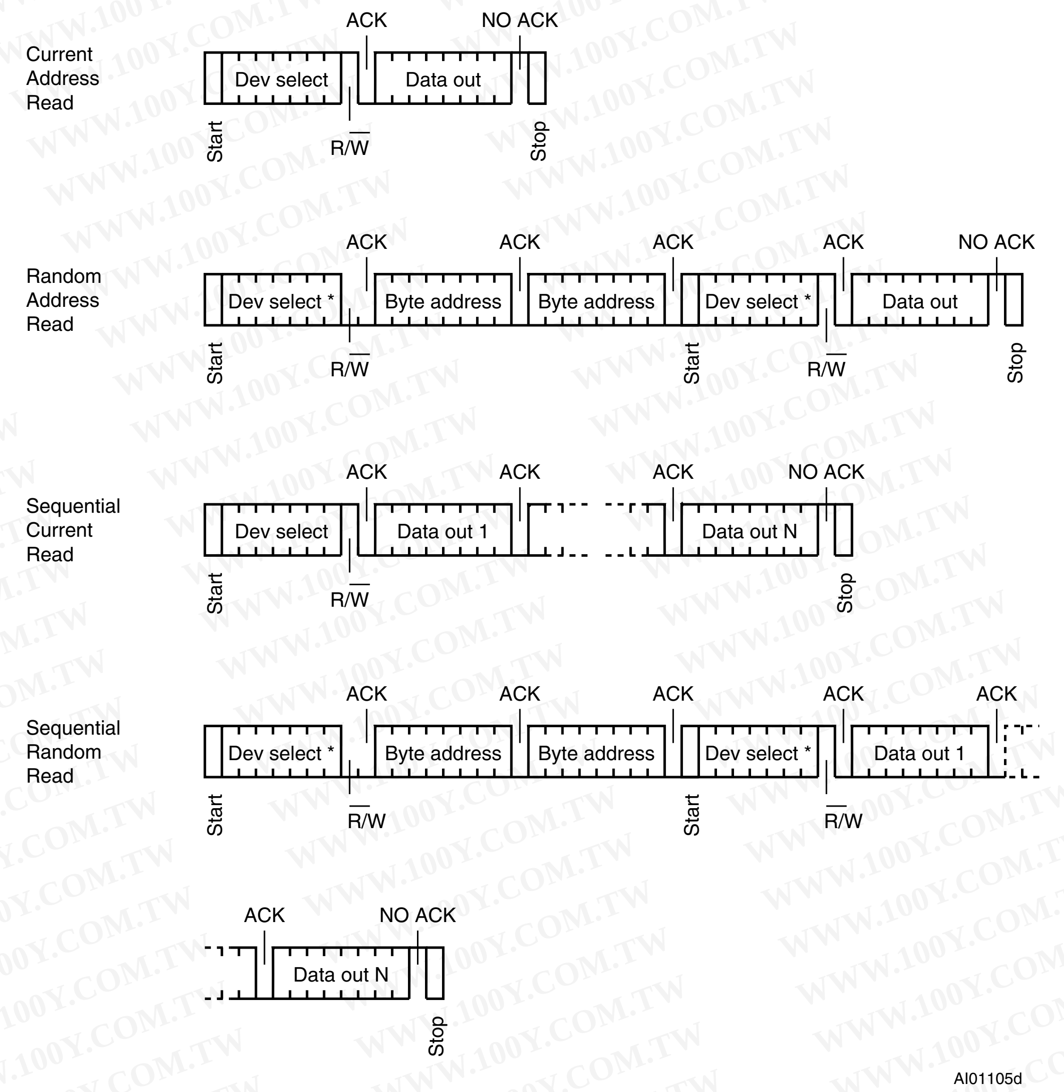
4.10 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in *Table 17* and *Table 18*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 10*, is:

1. Initial condition: a Write cycle is in progress.
2. Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
3. Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 11. Read mode sequences



1. The seven most significant bits of the device select code of a Random Read (in the 1st and 4th bytes) must be identical.

4.11 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{\text{WC}}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

4.12 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 11*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

4.13 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 11*, *without* acknowledging the Byte.

4.14 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 11*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

4.15 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

5 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

6 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
	PDIP-specific lead temperature during soldering		260(2)	°C
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(3)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. T_{LEAD} max must not be applied for more than 10 s.
3. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500 Ω, R2=500 Ω)

7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M24xxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 9. Operating conditions (M24xxx-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. Operating conditions (M24xxx-F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 5)	–20	85	°C

Table 11. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 12. AC test measurement I/O waveform

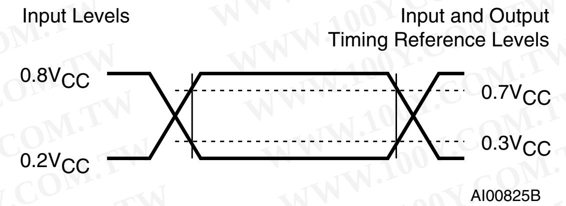


Table 12. Input parameters

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_{WCL}(1)	$\overline{WC}$ input impedance	$V_{IN} < 0.3V_{CC}$	50	200	kΩ
Z_{WCH}(1)	$\overline{WC}$ input impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}(1)	Pulse width ignored (Input filter on SCL and SDA)			200	ns

1. Characterized only.

Table 13. DC characteristics (M24xxx-W, device grade 6)

Symbol	Parameter	Test condition (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: Vss or Vcc		± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz		2	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(1)	mA
I_{CC1}	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		5	µA
	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input high voltage (SDA, SCL, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.

Table 14. DC characteristics (M24xxx-W, device grade 3)

Symbol	Parameter	Test condition (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: Vss or Vcc		± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz		2	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(1)	mA
I_{CC1}	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, 2.5 V < V_{CC} < 5.5 V		10	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)		–0.45	0.3V_{CC}	V
V_{IH}	Input high voltage (SDA, SCL, $\overline{WC}$)		0.7V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.

Table 15. DC characteristics (M24xxx-R - device grade 6)

Symbol	Parameter	Test condition (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c = 400 kHz		0.8	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V < V_{CC} < 2.5 V		3(1)	mA
I_{CC1}	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, 1.8 V < V_{CC} < 2.5 V		1	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SDA, SCL, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
		2.5 V ≤ V_{CC} < 5.5 V	0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.2	V

1. Characterized value, not tested in production.

Table 16. DC characteristics (M24xxx-F)(1)

Symbol	Parameter	Test condition (in addition to those in *Table 10*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA Hi-Z, external voltage applied on SDA: V_{SS} or Vcc		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} =1.7 V, f_c = 400 kHz		0.8	mA
I_{CC0}	Supply current (Write)	During t_W, 1.7 V < V_{CC} < 2.5 V		3(2)	mA
I_{CC1}	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, 1.7 V < V_{CC} < 2.5 V		1	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SDA, SCL, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
		2.5 V ≤ V_{CC} < 5.5 V	0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, V_{CC} = 1.7 V		0.2	V

1. Preliminary data.
2. Characterized value, not tested in production.

Table 17. AC characteristics (M24xxx-W6, M24xxW3, M24xxR6)

Test conditions specified in *Table 8* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{XH1XH2}(1)	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}(1)	t_F	Input signal fall time	20	300	ns
t_{DL1DL2}	t_F	SDA (out) fall time	20	100	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}	t_{DH}	Data out hold time	200		ns
t_{CLQV}(2)(3)	t_{AA}	Clock low to next data valid (access time)	200	900	ns
t_{CHDX}(4)	$t_{SU:STA}$	Start condition set up time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W		Write time		5(5)	ms

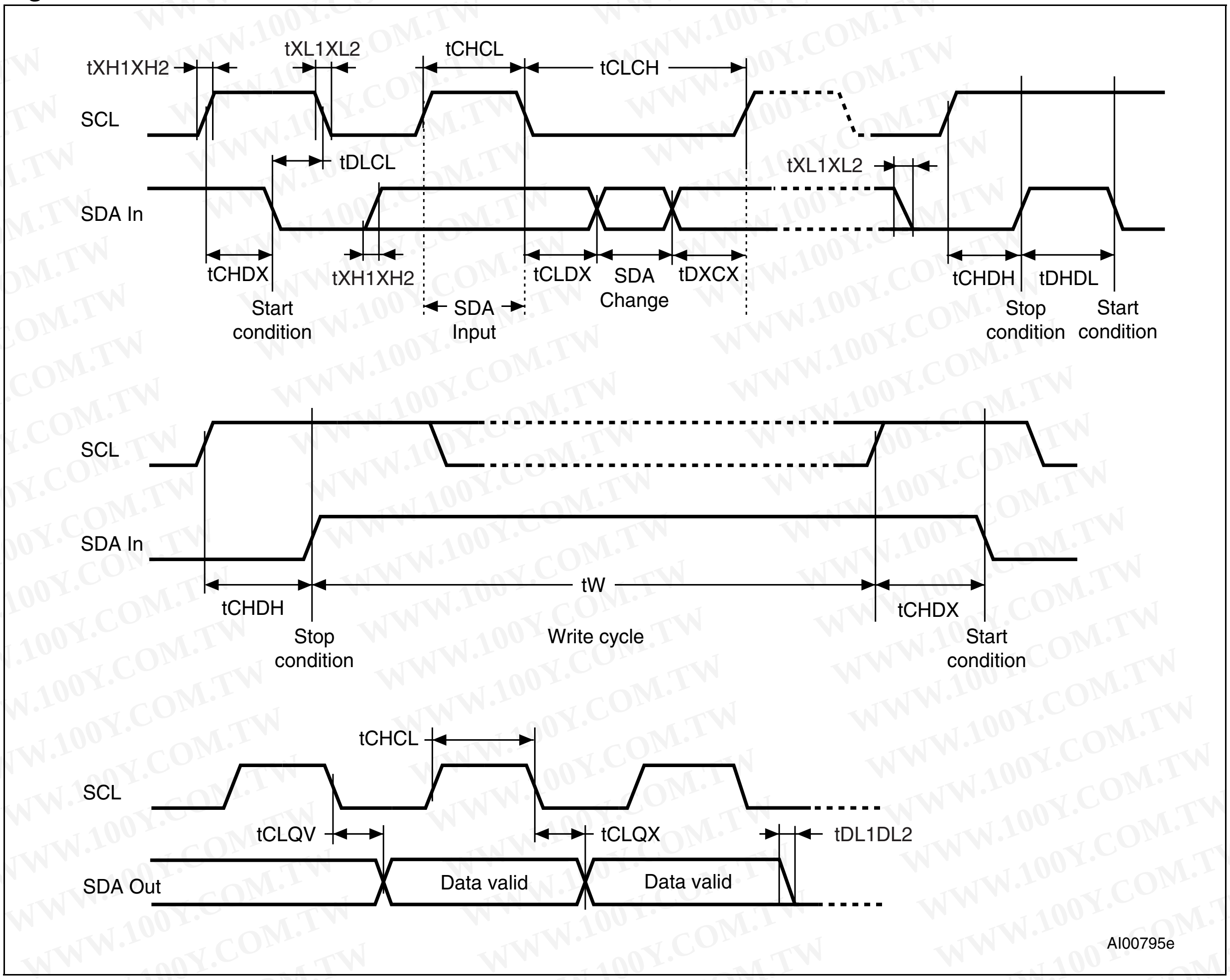
1. Values recommended by the I²C-bus Fast-Mode specification.
2. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach $0.8V_{CC}$ in a compatible way with the I^2C specification (which specifies $t_{SU:DAT}$ (min) = 100 ns), assuming that the $R_{bus} \times C_{bus}$ time constant is less than 500 ns (as specified in *Figure 5*).
4. For a reStart condition, or following a Write cycle.
5. For production lots assembled from 1st July 2007 (data code 727: week27, year 2007), the M24xxx-R (1.8 V to 5.5 V range) memories are specified with tw = 5 ms (instead of 10ms).

Table 18. AC characteristics (M24xxx-F)

Test conditions specified in *Table 10*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{XH1XH2}(1)	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}(1)	t_F	Input signal fall time	20	300	ns
t_{DL1DL2}	t_F	SDA (out) fall time	20	100	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}	t_{DH}	Data out hold time	200		ns
t_{CLQV}(2)(3)	t_{AA}	Clock low to next data valid (access time)	200	900	ns
t_{CHDX}(4)	$t_{SU:STA}$	Start condition set up time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W		Write time		10(5)	ms

1. Values recommended by the I²C-bus Fast-Mode specification.
2. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach $0.8V_{CC}$ in a compatible way with the I^2C specification (which specifies $t_{SU:DAT}$ (min) = 100 ns), assuming that the $R_{bus} \times C_{bus}$ time constant is less than 500 ns (as specified in *Figure 5*).
4. For a reStart condition, or following a Write cycle.
5. For temperature range 6: $t_{W(max)}$ = 5 ms.
For temperature range 5: $t_{W(max)}$ = 10 ms.

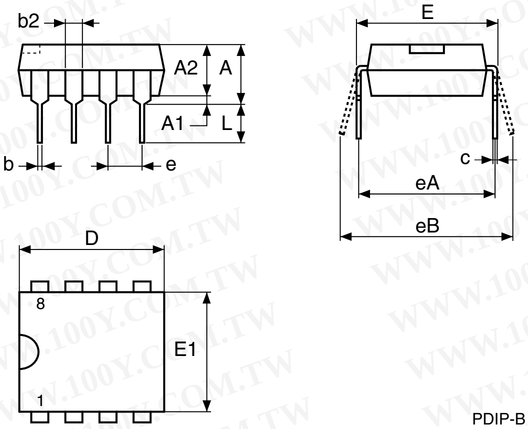
Figure 13. AC waveforms



8 Package mechanical data

In order to meet environmental requirements, ST offers the M24C32, M24C64 and M24128 in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 14. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package outline



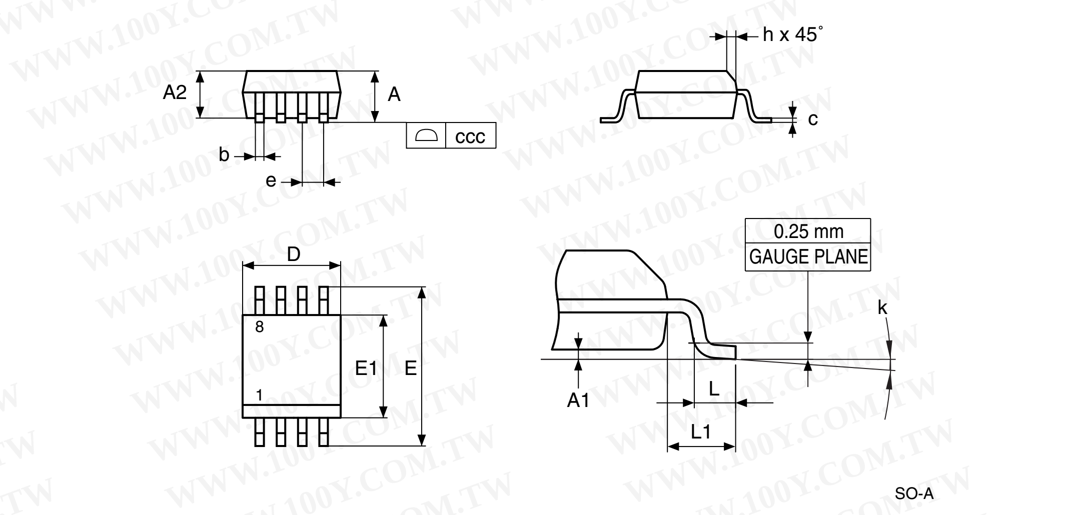
1. Drawing is not to scale.

Table 19. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.2098
A1		0.38			0.0150	
A2	3.30	2.92	4.95	0.1299	0.1150	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.0220
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.20	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.3650	0.3551	0.4000
E	7.87	7.62	8.26	0.3098	0.3000	0.3252
E1	6.35	6.10	7.11	0.2500	0.2402	0.2799
e	2.54	–	–	0.1000	–	–
eA	7.62	–	–	0.3000	–	–
eB			10.92			0.4299
L	3.30	2.92	3.81	0.1299	0.1150	0.1500

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 15. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline



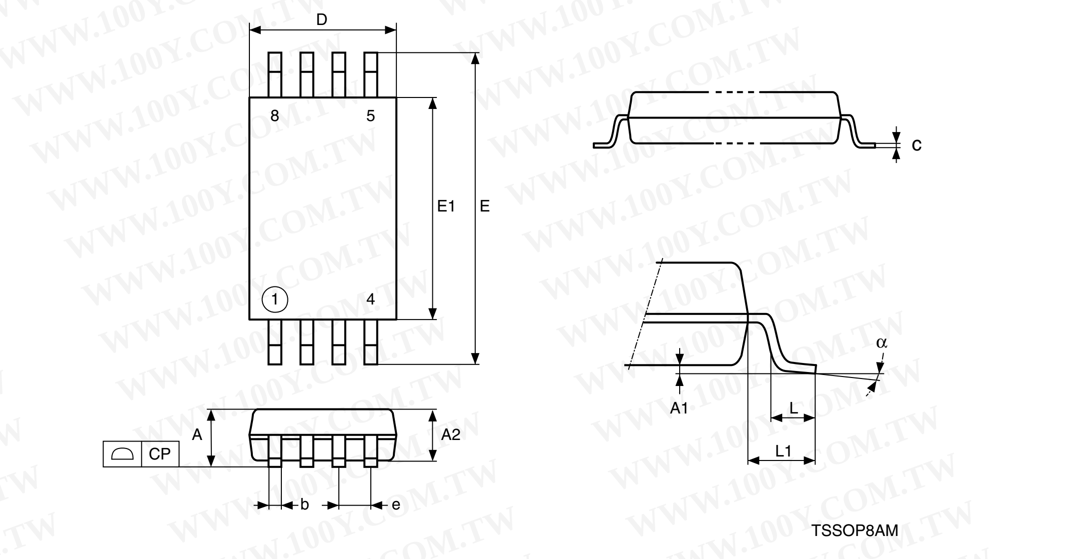
1. Drawing is not to scale.

Table 20. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.10	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.0110	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.10			0.0039
D	4.90	4.80	5.00	0.1929	0.1890	0.1969
E	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	–	–	0.0500	–	–
h		0.25	0.50			
k		0°	8°		0°	8°
L		0.40	1.27		0.0157	0.0500
L1	1.04			0.0410		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 16. TSSOP8 – 8 lead thin shrink small outline, package outline



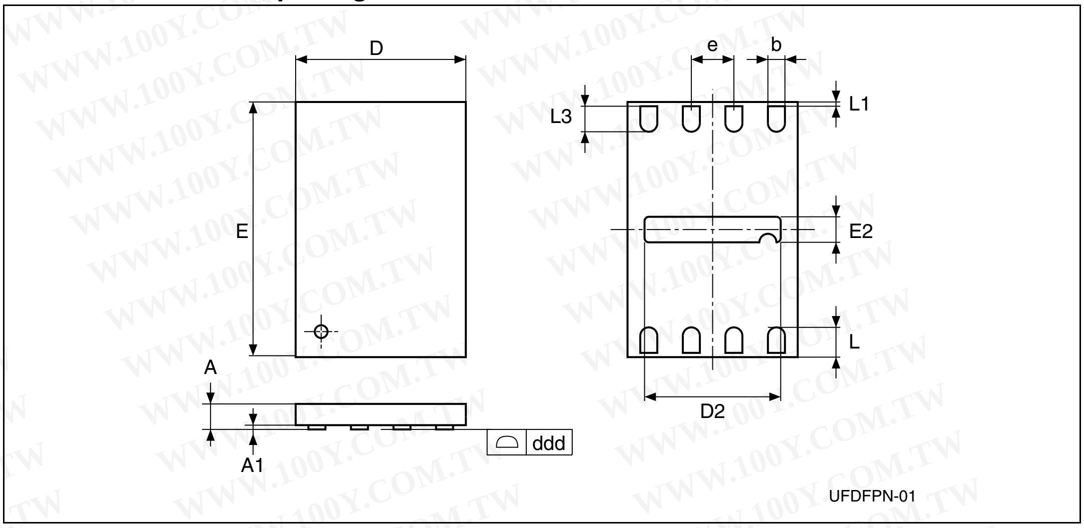
1. Drawing is not to scale.

Table 21. TSSOP8 – 8 lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 17. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, package outline



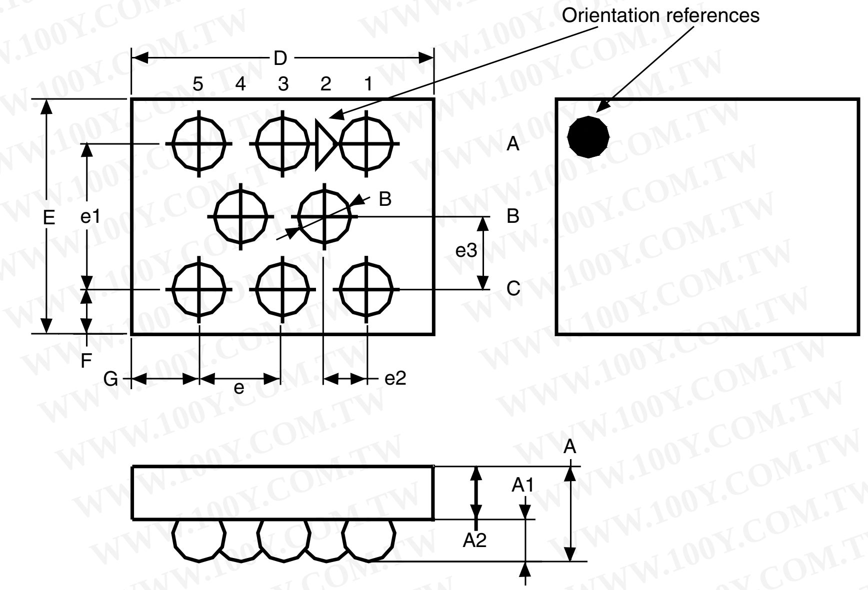
1. Drawing is not to scale.

Table 22. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.50	0.60	0.0217	0.0197	0.0236
A1	0.02	0.00	0.05	0.0008	0	0.0020
b	0.25	0.20	0.30	0.0098	0.0079	0.0118
D	2.00	1.90	2.10	0.0787	0.0748	0.0827
D2	1.60	1.50	1.70	0.0630	0.0591	0.0669
ddd			0.08			0.0031
E	3.00	2.90	3.10	0.1181	0.1142	0.1220
E2	0.20	0.10	0.30	0.0079	0.0039	0.0118
e	0.50	–	–	0.0197	–	–
L	0.45	0.40	0.50	0.0177	0.0157	0.0197
L1			0.15			0.0059
L3		0.30			0.0118	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 18. M24128 WLCSP, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 23. M24128 WLCSP, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[(1)]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.585	0.535	0.635	0.0230	0.0211	0.0250
A1	0.230	0.205	0.255	0.0091	0.0081	0.0100
A2	0.355	0.330	0.380	0.0140	0.0130	0.0150
B	0.320	0.290	0.350	0.0126	0.0114	0.0138
D	1.805	1.785	1.825	0.0711	0.0703	0.0719
E	1.400	1.380	1.420	0.0551	0.0543	0.0559
e	0.5			0.0197		
e1	0.886			0.0349		
e2	0.250			0.0098		
e3	0.443			0.0174		
F	0.257			0.0101		
G	0.4025			0.0158		
N[(2)]	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. N is the total number of terminals.

9 Part numbering

Table 24. Ordering information scheme

Example: M24C32– W MN 6 T P /P

Device type

M24 = I^2C serial access EEPROM

Device function

128–B = 128 Kbit (16384 x 8)
C64– = 64 Kbit (8192 x 8)
C32– = 32 Kbit (4096 x 8)

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V
R = V_{CC} = 1.8 V to 5.5 V
F = V_{CC} = 1.7 V to 5.5 V

Package

BN = PDIP8
MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
MB = UFDFPN8 (MLP8)
CS = WLCSP

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C
3 = Automotive: device tested with high reliability certified flow(1) over –40 to 125°C.
5 = Consumer: device tested with standard test flow over –20 to 85°C

Option

blank = standard packing
T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(2)

P = F6DP26% Chartered
A = F8L Rousset (only for the WLCSP package)

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for device grade 3 and WLCSP packages.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 25. Available M24C32 products (package, voltage range, temperature grade)

Package	M24C32-F 1.7 V to 5.5 V	M24C32-R 1.8 V to 5.5 V	M24C32-W 2.5 V to 5.5 V
DIP8 (BN)	-	-	Grade6
SO8N (MN)	-	Grade 6	Grade 3 Grade 6
TSSOP8 (DW)	Grade 5	Grade 6	Grade 6
MLP8 (MB)	Grade 5	Grade 6	-

Table 26. Available M24C64 products (package, voltage range, temperature grade)

Package	M24C64-F 1.7 V to 5.5 V	M24C64-R 1.8 V to 5.5 V	M24C64-W 2.5 V to 5.5 V
DIP8 (BN)	-	-	Grade6
SO8N (MN)	-	Grade 6	Grade 3 Grade 6
TSSOP8 (DW)	Grade 5	Grade 6	Grade 6
MLP8 (MB)	Grade 6	Grade 6	-

Table 27. Available M24128 products (package, voltage range, temperature grade)

Package	M24128-BF 1.7 V to 5.5 V	M24128-BR 1.8 V to 5.5 V	M24128-BW 2.5 V to 5.5 V
DIP8 (BN)	-	-	-
SO8N (MN)	-	Grade 6	Grade 3 Grade 6
TSSOP8 (DW)	-	Grade 6	Grade 6
MLP8 (MB)	Grade 6	Grade 6	-
WLCSP (CS)	Grade 6	Grade 6	-

10 Revision history

Table 28. **Document revision history**

Date	Revision	Changes
22-Dec-1999	2.3	TSSOP8 package in place of TSSOP14 (pp 1, 2, OrderingInfo, PackageMechData).
28-Jun-2000	2.4	TSSOP8 package data corrected
31-Oct-2000	2.5	References to Temperature Range 3 removed from Ordering Information Voltage range -S added, and range -R removed from text and tables throughout.
20-Apr-2001	2.6	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical data updated
16-Jan-2002	2.7	Test condition for I_{LI} made more precise, and value of I_{LI} for E2-E0 and $\overline{WC}$ added -R voltage range added
02-Aug-2002	2.8	Document reformatted using new template. TSSOP8 (3x3mm² body size) package (MSOP8) added. 5ms write time offered for 5V and 2.5V devices
04-Feb-2003	2.9	SO8W package removed. -S voltage range removed
27-May-2003	2.10	TSSOP8 (3x3mm² body size) package (MSOP8) removed
22-Oct-2003	3.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Write Operations, Read Operations. V_{IL}(min) improved to -0.45V.
01-Jun-2004	4.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade clarified
04-Nov-2004	5.0	Product List summary table added. Device Grade 3 added. 4.5-5.5V range is Not for New Design. Some minor wording changes. AEC-Q100-002 compliance. t_{NS}(max) changed. V_{IL}(min) is the same on all input pins of the device. Z_{WCL} changed.
05-Jan-2005	6.0	UFDFPN8 package added. Small text changes.

Table 28. Document revision history (continued)

Date	Revision	Changes
29-Jun-2006	7	Document converted to new ST template. M24C32 and M24C64 products (4.5 to 5.5V supply voltage) removed. M24C64 and M24C32 products (1.7 to 5.5V supply voltage) added. *Section 2.3: Chip Enable (E0, E1, E2)* and *Section 2.4: Write Control (WC)* modified, *Section 2.6: Supply voltage (V_{CC})* added and replaces *Power On Reset: VCC Lock-Out Write Protect* section. T_A added, *Note 1* updated and T_{LEAD} specified for PDIP packages in *Table 7: Absolute maximum ratings*. I_{CC0} added, I_{CC} voltage conditions changed and I_{CC1} specified over the whole voltage range in *Table 13: DC characteristics (M24xxx-W, device grade 6)*. I_{CC0} added, I_{CC} frequency conditions changed and I_{CC1} specified over the whole voltage range in *Table 15: DC characteristics (M24xxx-R - device grade 6)*. t_W modified in *Table 17: AC characteristics (M24xxx-W6, M24xxW3, M24xxR6)*. SO8N package specifications updated (see *Figure 15* and *Table 20*). Device grade 5 added, B and P Process letters added to *Table 24: Ordering information scheme*. Small text changes.
03-Jul-2006	8	I_{CC1} modified in *Table 13: DC characteristics (M24xxx-W, device grade 6)*. *Note 1* added to *Table 16: DC characteristics (M24xxx-F)* and table title modified.
17-Oct-2006	9	UFDFPN8 package specifications updated (see *Table 22*). M24128-BW- and M24128-BR part numbers added. Generic part number corrected in *Features on page 1*. I_{CC0} corrected in *Table 14* and *Table 13*. Packages are ECOPACK® compliant.
27-Apr-2007	10	Available packages and temperature ranges by product specified in *Table 25*, *Table 26* and *Table 27*. Notes modified below *Table 12: Input parameters*. V_{IH} max modified in DC characteristics tables (see *Table 13*, *Table 14*, *Table 15* and *Table 16*). C process code added to *Table 24: Ordering information scheme*. For M24xxx-R (1.8 V to 5.5 V range) products assembled from July 2007 on, t_W will be 5 ms (see *Table 17: AC characteristics (M24xxx-W6, M24xxW3, M24xxR6)*.
27-Nov-2007	11	Small text changes. *Section 2.5: V_{SS} ground* and *Section 4.9: ECC (error correction code) and write cycling* added. V_{IL} and V_{IH} modified in *Table 15: DC characteristics (M24xxx-R - device grade 6)*. JEDEC standard reference updated below *Table 7: Absolute maximum ratings*. Package mechanical data inch values calculated from mm and rounded to 4 decimal digits (see *Section 8: Package mechanical data*).

Table 28. Document revision history (continued)

Date	Revision	Changes
18-Dec-2007	12	Added *Section 2.6.2: Power-up conditions*, updated *Section 2.6.3: Device reset*, and *Section 2.6.4: Power-down conditions* in *Section 2.6: Supply voltage (V_{CC})*. Updated *Figure 5: Maximum R_P value versus bus parasitic capacitance (C) for an I^2C bus*. Replace M24128 and M24C64 by M24128-BFMB6 and M24C64-FMB6, respectively, in *Section 4.9: ECC (error correction code) and write cycling*. Added temperature grade 6 in *Table 10: Operating conditions (M24xxx-F)*. Updated test conditions for I_{LO} and V_{LO} in *Table 13: DC characteristics (M24xxx-W, device grade 6)*, *Table 14: DC characteristics (M24xxx-W, device grade 3)*, and *Table 15: DC characteristics (M24xxx-R - device grade 6)*. Test condition updated for I_{LO}, and V_{IH} and V_{IL} differentiate for 1.8 V ≤ V_{CC} < 2.5 V and 2.5 V ≤V_{CC} < 5.5 V in *Table 16: DC characteristics (M24xxx-F)*. Updated *Table 17: AC characteristics (M24xxx-W6, M24xxW3, M24xxR6)*, and *Table 18: AC characteristics (M24xxx-F)*. Updated *Figure 13: AC waveforms*. Added M24128-BF in *Table 27: Available M24128 products (package, voltage range, temperature grade)*. Process B removed from *Table 24: Ordering information scheme*.
30-May-2008	13	Small text changes. C *Process* option and Blank *Plating technology* option removed from *Table 24: Ordering information scheme*.
15-Jul-2008	14	WLCSP package added (see *Figure 3: M24128 WLCSP connections (top view, marking side, with balls on the underside)* and *Section 8: Package mechanical data*). *Section 4.9: ECC (error correction code) and write cycling* updated.