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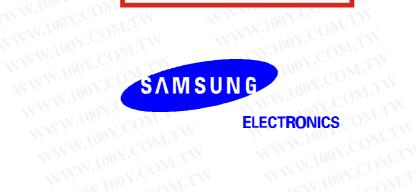
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S524A Series (I²C Bus) Serial EEPROM Data Sheet, Revision 1 Publication Number: 11-S5-24A Series-072001

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S524AB0X91/B0XB1

S524AD0XD1/D0XF1

S524AE0XH1

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Product	Density (Organization)	Page Buffer	Write Time (Max)	Write Protect	Endurance	Operating Voltage	Packa
S524A40X11	1K-bit (128 × 8)	16 bytes	5 ms	N H/W	1M	1.8V-5.5V	8DIP/SOP/
S524A40X10	1K-bit (128 × 8)	16 bytes	5 ms	H/W, S/W	1M	1.8V-5.5V	8DIP/SOP/
S524A40X21	2K-bit (256 × 8)	16 bytes	5 ms	H/W	1M	1.8V-5.5V	8DIP/SOP/
S524A40X20	2K-bit (256 × 8)	16 bytes	5 ms	H/W, S/W	1M	1.8V-5.5V	8DIP/SOP/
S524A40X41	4K-bit (512 × 8)	16 bytes	5 ms	H/W	1M	1.8V-5.5V	8DIP/SOP/
S524A40X40	4K-bit (512 × 8)	16 bytes	5 ms	H/W, S/W	1M	1.8V-5.5V	8DIP/SOP/
S524A60X81	8K-bit (1024 × 8)	16 bytes	5 ms	H/W	1M	1.8V-5.5V	8DIP/SOP/
S524A60X51	16K-bit (2048 × 8)	16 bytes	5 ms	H/W	1M	1.8V-5.5V	8DIP/SOP/
S524AB0X91	32K-bit (4096 × 8)	32 bytes	5 ms	H/W	1M	1.8V-5.5V	8DIP/SOP/
S524AB0XB1	64K-bit (8192 × 8)	32 bytes	5 ms	H/W	1M	1.8V-5.5V	8DIP/SOP/
S524AD0XD1	128K-bit (16384 × 8)	64 bytes	5 ms	H/W	500K	1.8V-5.5V	8DIP/TS
S524AD0XF1	256K-bit (32768 × 8)	64 bytes	5 ms	H/W	500K	1.8V-5.5V	8DIP/TS

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SAMSUNG ELECTRONICS

S524A40X10/40X20/40X40

1K/2K/4K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524A40X10/40X20/40X40 serial EEPROM has a 1,024/2,048/4,096-bit (128/256/512-byte) capacity, supporting the standard I²CTM-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). Important features are a hardware-based write protection circuit for the entire memory area and software-based write protection logic for the lower 128 bytes. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. The software-based method is one-time programmable and permanent. Using one-page write mode, you can load up to 16 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524A40X10/40X20/40X40 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 1K/2K/4K-bit (128/256/512-byte) storage area
- 16-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- Software-based write protection for the lower 128-byte EEPROM
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

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Operating Characteristics

- Operating voltage
 - 1.8 V to 5.5 V
- Operating current
 - Maximum write current: < 3 mA at 5.5 V
 - Maximum read current: < 200 μA at 5.5 V
 - Maximum stand-by current: < 5 μA at 5.5 V
- Operating temperature range
 - - 25°C to + 70°C (commercial)
 - – 40°C to + 85°C (industrial)
- Operating clock frequencies
 - 100 kHz at standard mode
 - 400 kHz at fast mode
- Electrostatic discharge (ESD)
 - 5,000 V (HBM)
 - 500 V (MM)

Packages

8-pin DIP, SOP, and TSSOP



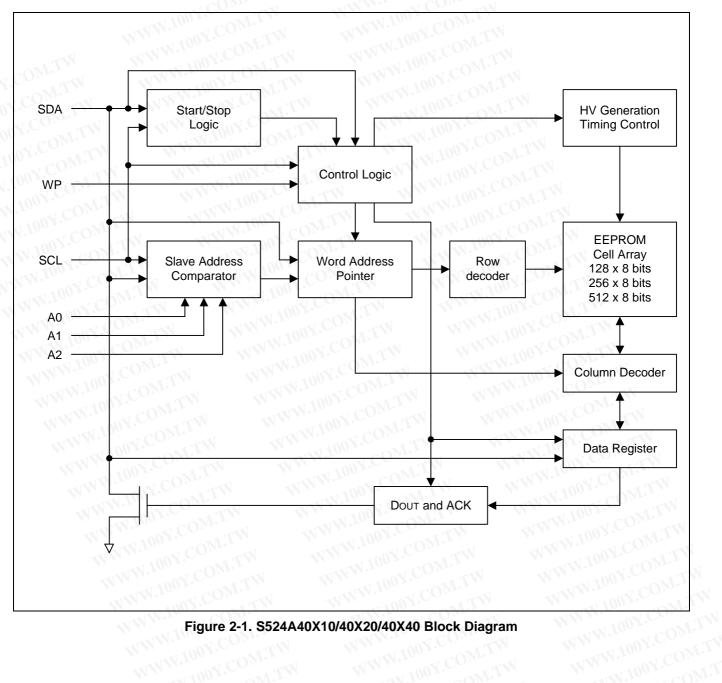


Figure 2-1. S524A40X10/40X20/40X40 Block Diagram WWW.100Y.CC WW.100Y.COM.TW

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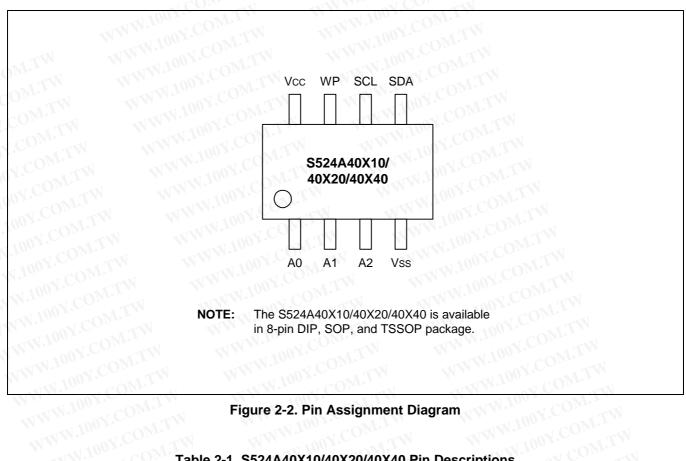


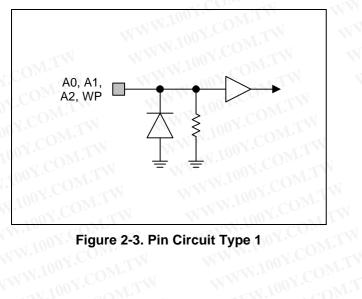
Figure 2-2. Pin Assignment Diagram

Table 2-1. S524A40X10/40X20/40X40 Pin Descriptions

Name	Туре	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS} .	OM.TV
V _{SS}	M 41 100	Ground pin.	$CO_{M',I}$
SDA	1/O M	Bi-directional data pin for the I 2 C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V $_{CC.}$ Typical values for this pull-up resistor are 4.7 k Ω (100 kHz) and 1 k Ω (400 kHz).	00 X .COM
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC} , the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS} , the write function is enabled. This pin is internally pulled down to V_{SS} .	N.1001Y.C
V _{CC}	- 1	Single power supply.	100 - 100

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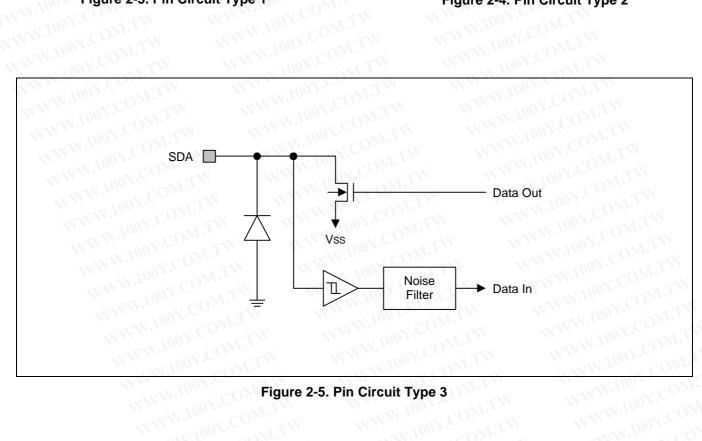


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Figure 2-3. Pin Circuit Type 1 WWW.100Y.CC

Figure 2-4. Pin Circuit Type 2 WWW.100Y.

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FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524A40X10/40X20/40X40 supports the I^2 C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as the "transmitter" and any device that gets data from the bus is the "receiver." The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0,A1 and A2 input pins, up to eight S524A40X10/40X20 (four for S524A40X40) devices can be connected to the same I²C-bus as slaves (see Figure 2-6). Both the master and slaves can operate as transmitter or receiver, but the master device determines which bus operating mode would be active.

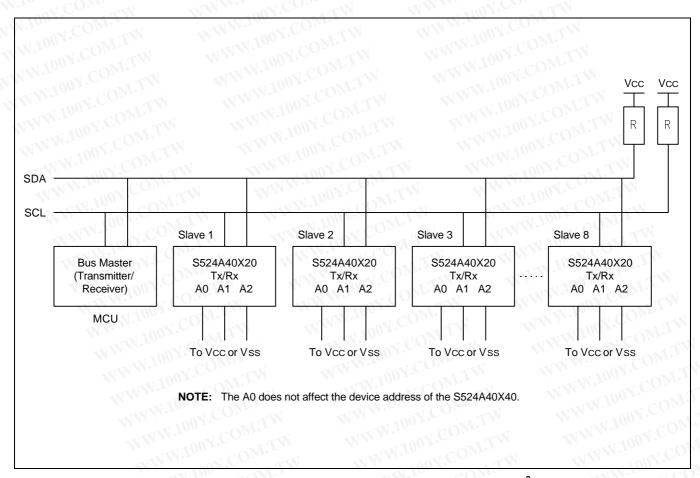


Figure 2-6. Typical Configuration (16 Kbits of Memory on the I²C-Bus)



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I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers

- A new data transfer can be initiated only when the bus is currently not busy.
- MSB is always transferred first in transmitting data.
- During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- <u>Start condition</u>: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- <u>Stop condition</u>: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition (see Figure 2-7).

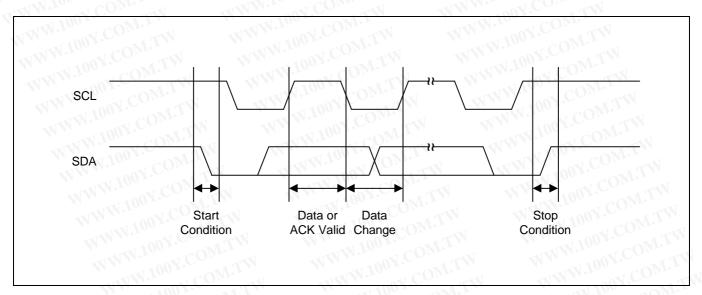


Figure 2-7. Data Transmission Sequence

- <u>Data valid</u>: Following a start condition, the data becomes valid if the data line remains stable for the duration
 of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock
 pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total
 number of bytes that can be transferred in one operation is theoretically unlimited.
- <u>ACK (Acknowledge)</u>: An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 2-8). But the slave does not send an ACK if an internal write cycle is still in progress.

In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.



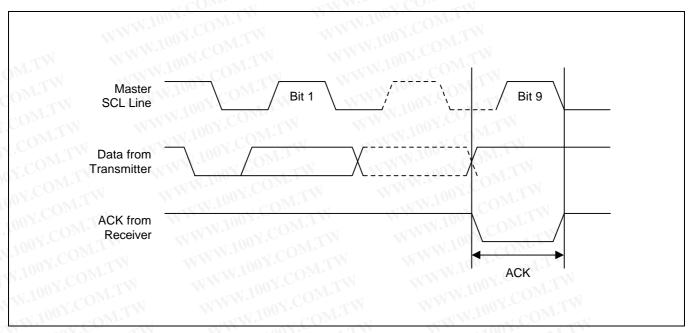


Figure 2-8. Acknowledge Response From Receiver

- <u>Slave Address</u>: After the master initiates a Start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the "device identifier". The identifier for the S524A40X10/40X20/40X40 is "1010B". The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1 and A2 pins. Using this addressing scheme, you can cascade up to eight S524A40X10/40X20 or four S524A40X40 on the bus (see Table 2-2 below). The b1 for S524A40X40 is used by the master to select which of the blocks of internal memory (1 block = 256 words) are to be accessed. The bit is in effect the most significant bit of the word address.
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is "1", a read operation is executed. If it is "0", a write operation is executed.

Function	De	evice I	dentif	ier	D. W. D	evice Addres	SS	R/W Bit
	b7	b6	b5	b4	b3	b2	b1 ^(note)	b0 CO
Read	W-101	0	011	0	A2	A1	A0	WWW. To TY.CO
Write	111	0	(1)	0	A2	A1 CO	A0	WWW. 0 W.C
Write-protect	0	1.	(1)	0	A2	A1, CO	A0	WWW.0 OX.C

Table 2-2. Slave Device Addressing

NOTE: The b1 for S524A40X40 corresponds to the MSB of the memory array address word.



BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the S524A40X10/40X20/40X40 slave device (see Figure 2-9).

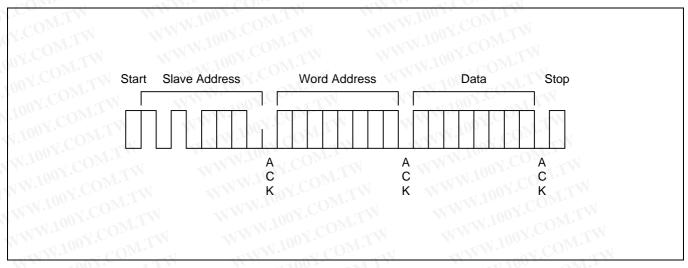


Figure 2-9. Byte Write Operation

Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to "0" onto the bus. Then the addressed S524A40X10/40X20/40X40 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the S524A40X10/40X20/40X40.

When the S524A40X10/40X20/40X40 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the S524A40X10/40X20/40X40 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the S524A40X10/40X20/40X40 begins the internal write cycle.

While the internal write cycle is in progress, all S524A40X10/40X20/40X40 inputs are disabled and the S524A40X10/40X20/40X40 does not respond to additional requests from the master.



PAGE WRITE OPERATION

The S524A40X10/40X20/40X40 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The S524A40X10/40X20/40X40 responds with an ACK each time it receives a complete byte of data (see Figure 2-10).

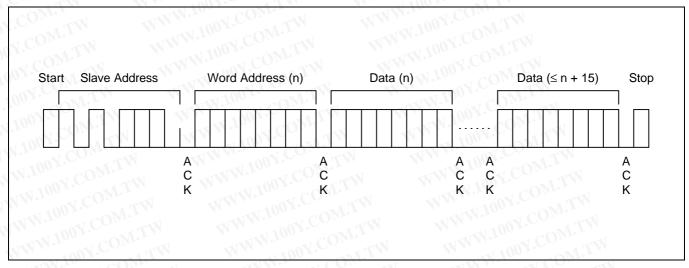


Figure 2-10. Page Write Operation

The S524A40X10/40X20/40X40 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.

If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the S524A40X10/40X20/40X40 word address pointer value "rolls over" and the previously received data is overwritten. If the master transmits less than 16 bytes and generates a stop condition, the S524A40X10/40X20/40X40 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.



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POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524A40X10/40X20/40X40 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524A40X10/40X20/40X40 remains busy with the write operation, no ACK is returned. When the S524A40X10/40X20/40X40 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 2-11).

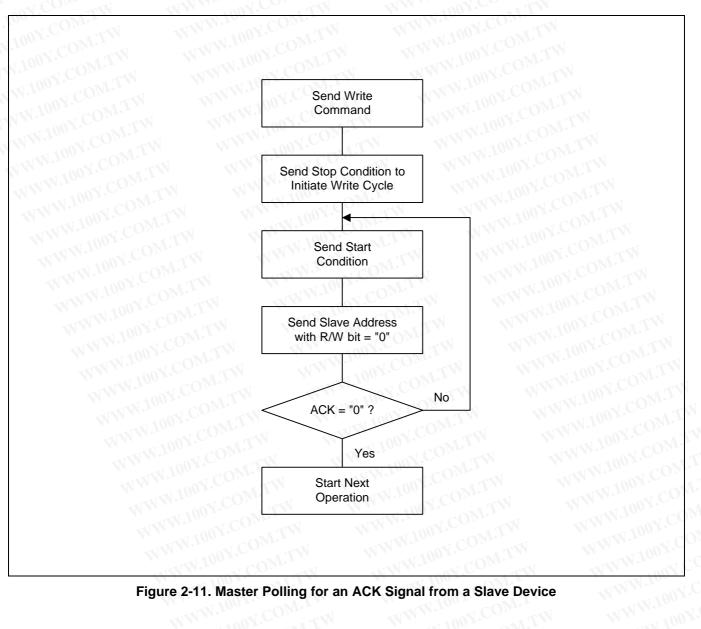


Figure 2-11. Master Polling for an ACK Signal from a Slave Device

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SOFTWARE-BASED WRITE PROTECTION

You can write-protect the lower 128 bytes of the EEPROM, locations 00H–7FH, in one operation. To do this, you simply write a value to a one-time, write-only register. Once you have applied this write protection, any write attempt to access the lower 128-byte area is ignored. In other words, the write protection is permanent. The effect of such a failed attempt is processed in the same way as an invalid I²C-bus protocol.

To enable write protection, you must execute a write operation to the write protection register. To access the write protection register, you use the device address "0110". The word address and data in this write operation can be any value and the timing and wave form characteristics are identical to a normal byte write operation (see Figure 2-12).

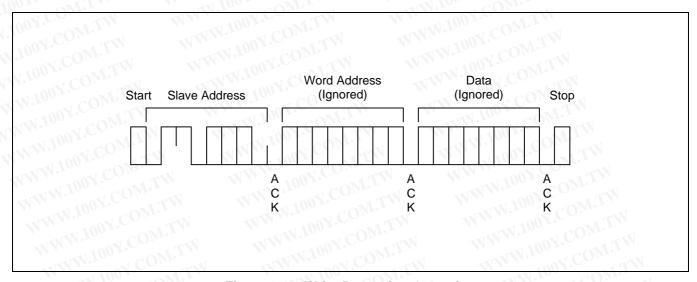


Figure 2-12. Write Protection Operation

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524A40X10/40X20/40X40. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to the memory is ignored.

The S524A40X10/40X20/40X40 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated. By connecting the WP pin to V_{SS} , the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.



CURRENT ADDRESS BYTE READ OPERATION

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The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address "n", the next read operation would access data at address "n+1".

When the S524A40X10/40X20/40X40 receives a slave address with the R/W bit set to "1", it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the S524A40X10/40X20/40X40 effectively stops the transmission (see Figure 2-13).

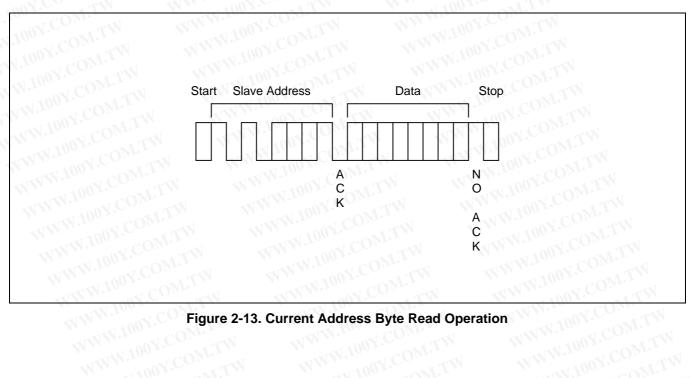


Figure 2-13. Current Address Byte Read Operation WWW.100Y.CO

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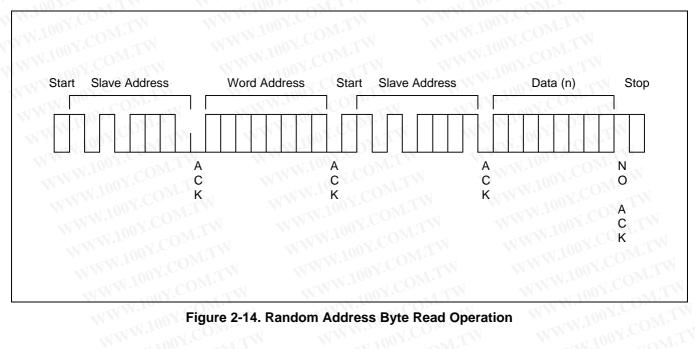
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RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. This operation is performed in the following steps:

- The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the S524A40X10/40X20/40X40 to the desired address.)
- When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to "1".
- The S524A40X10/40X20/40X40 then sends an ACK and the 8-bit data stored at the desired address.
- At this point, the master does not acknowledge the transmission, but generates a stop condition instead.
- In response, the S524A40X10/40X20/40X40 stops transmitting data and reverts to its stand-by mode (see Figure 2-14).



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SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time, however, the master responds with an ACK, indicating that it requires additional data.

The S524A40X10/40X20/40X40 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

Using this method, data is output sequentially with the data from address "n" followed by the data from "n+1". The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer "rolls over" and the S524A40X10/40X20/40X40 continues to transmit data for each ACK it receives from the master (see Figure 2-15).

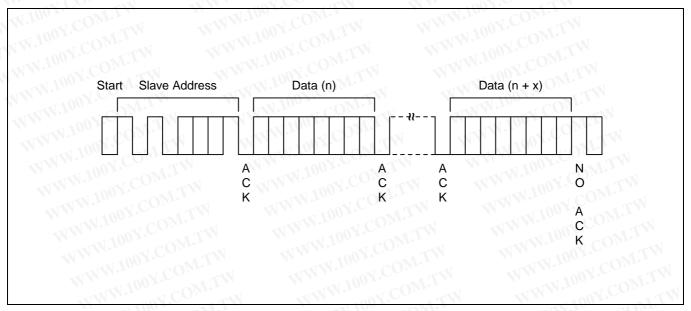


Figure 2-15. Sequential Read Operation



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Table 2-3. Absolute Maximum Ratings

W.100Y.COM.TW $(T_A = 25^{\circ}C)$

Parameter	Symbol	Conditions	Rating	Uni
Supply voltage	10 V _{CC}	- WWW.100	-0.3 to $+7.0$	V
Input voltage	V _{IN}	1.1.4 MM.10	-0.3 to +7.0	V
Output voltage	Vo	N.T MMN.)	-0.3 to +7.0	V
Operating temperature	TA	MIT - MAM	- 40 to + 85	°C
Storage temperature	T _{STG}	OM. TWY	-65 to +150	°C
Electrostatic discharge	V _{ESD}	HBM	5000	V
	M.10	MM	500	

Table 2-4. D.C. Electrical Characteristics $(T_A = -25^{\circ}\text{C to} + 70^{\circ}\text{C (C)}, -40^{\circ}\text{C to} + 85^{\circ}\text{C (I)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V})$

Parame	ter	Symbol	Conditions	Min	Тур	Max	Unit V
Input low voltage	e_OM.TV	V _{IL}	SCL, SDA, A0, A1, A2	<u> </u>	M.100 x.	0.3 V _{CC}	
Input high voltag	je M.	V _{IH}	NW.100Y.COM.TW	0.7 V _{CC}	1M.700.	COM	V
Input leakage current Output leakage current		ILI	$V_{IN} = 0$ to V_{CC}	- 📉	MM7100	10 10	μA μA
		I _{LO}	$V_O = 0$ to V_{CC}				
Output low volta	ge	V _{OL}	$I_{OL} = 0.15 \text{ mA}, V_{CC} = 1.8 \text{ V}$	N -	MATN'	0.2	V
	MMM.1003.COMITA		$I_{OL} = 2.1 \text{ mA}, V_{CC} = 2.5 \text{ V}$	W -	MAIN	0.4	
Supply current	Write	I _{CC1}	V _{CC} = 5.5 V, 400 kHz	TW-	TEN	3	mA
	N.100X.	I _{CC2}	V _{CC} = 1.8 V, 100 kHz	A.TY	AM	110 Y.C	
	Read	I _{CC3}	V _{CC} = 5.5 V, 400 kHz	W.Tan	_1/1	0.2	
	NW. 100	I _{CC4}	V _{CC} = 1.8 V, 100 kHz	OMITH	- 1	60	μA
Stand-by curren	MMM.TO	I _{CC5}	V _{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	CONFITY	-	5.10	μA
		I _{CC6}	V _{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	y.com.T	M =	1 1	

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Table 2-4. D.C. Electrical Characteristics (Continued)

 $(T_A = -25^{\circ}C \text{ to } + 70^{\circ}C \text{ (C)}, -40^{\circ}C \text{ to } + 85^{\circ}C \text{ (I)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V)}$

Parameter	Symbol	Conditions	Min	√ Тур	Max	Unit
Input capacitance	C _{IN}	25°C, 1MHz, V _{CC} = 5 V, V _{IN} = 0 V, A0, A1, A2, SCL and WP pin	COM:	IN -	10	pF
Input/output capacitance	C _{I/O}	25°C, 1MHz, $V_{CC} = 5 \text{ V}, V_{I/O} = 0 \text{ V},$ SDA pin	100X.CO	M.TW W.TW	10	

Table 2-5. A.C. Electrical Characteristics

 $(T_A = -25^{\circ}C \text{ to} + 70^{\circ}C \text{ (C)}, -40^{\circ}C \text{ to} + 85^{\circ}C \text{ (I)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V)}$

Parameter	Symbol	Conditions		8 to 5.5 V rd Mode)		5 to 5.5 V Mode)	Unit
	MI	TW.100Y.CC	Min	Max	Min	Max	
External clock frequency	F _{CLK}	W.HOY.C	0110	100	1.10	400	kHz
Clock high time	t _{HIGH}	100x.	4	- 1	0.6	COM	μs
Clock low time	t _{LOW}	M. 100 z	4.7	N - 1	1.3	V.CON.	N
Rising time	t _R	SDA, SCL	V.COM.	1	MAN TO	0.3	W
Falling time	t_{F}	SDA, SCL	ON.COM	0.3	MATMIN	0.3	TW
Start condition hold time	t _{HD:STA}	W-WW.	0014 ^{ON}	TW	0.6	100X-COM	WII
Start condition setup time	t _{SU:STA}	AMM.	4.7	MT	0.6	1004.00	WIM
Data input hold time	t _{HD:DAT}	-1/1/1/	1001.00	OV. EV	0	N.10 0 Y.C	OM.TV
Data input setup time	t _{SU:DAT}	- 1/1/1	0.25	WEMO	0.1	W.1007.0	T.MO
Stop condition setup time	t _{SU:STO}	- 417	4001	CONTITU	0.6	WW. ±00 Y	COM
Bus free time	t _{BUF}	Before new transmission	4.7	Y.CONT	1.3	MANA 100	Y.COM
Data output valid from clock low ^(note)	t _{AA}	LTW -	0.3	3.5	TW -	0.9	OX.CO
Noise spike width	t _{SP}	M. TV	WAM.	100	CTV +	50	ns
Write cycle time	t _{WR}	OM.	NAM IN	5.CO	174	5	ms

NOTES:

- 1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
- 2. When acting as a transmitter, the S524A40X10/40X20/40X40 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.



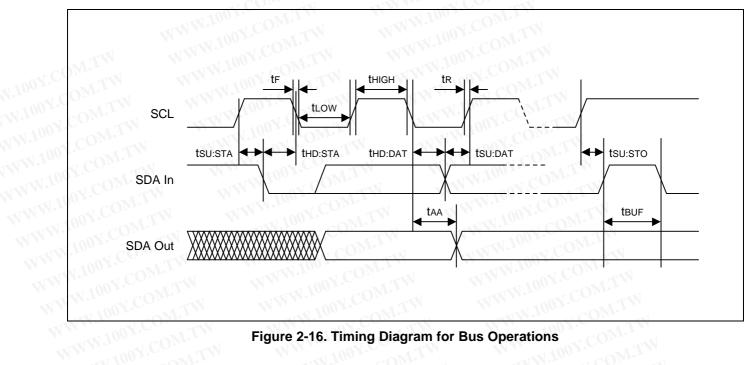


Figure 2-16. Timing Diagram for Bus Operations

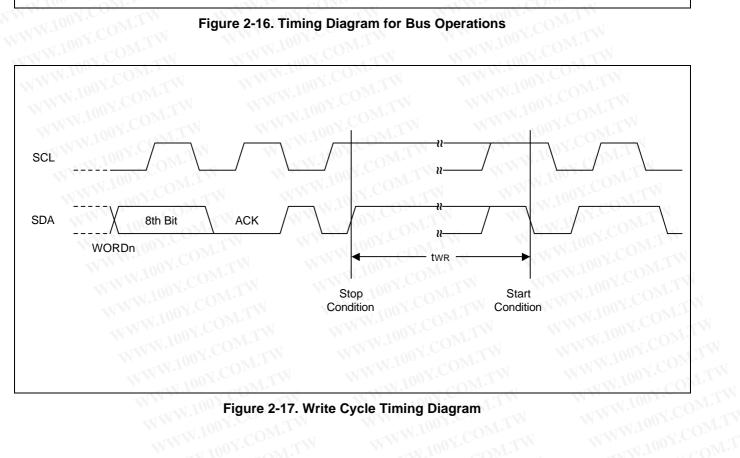


Figure 2-17. Write Cycle Timing Diagram WWW.100Y.COM.TW WWW.100Y WWW.100Y.COM.

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WWW.100Y.

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S524A40X11/40X21/ 40X41/60X81/60X51

1K/2K/4K/8K/16K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524A40X11/40X21/40X41/60X81/60X51 serial EEPROM has a 1,024/2,048/4,096/8,192/16,384-bit capacity, supporting the standard I^2C^{TM} -bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 16 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524A40X11/40X21/40X41/60X81/60X51 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 1K/2K/4K/8K/16K-bit (128/256/512/1,024/2,048-byte) storage area
- 16-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

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Operating Characteristics

- Operating voltage
 - 1.8 V to 5.5 V
- Operating current
 - Maximum write current: < 3 mA at 5.5 V
 - Maximum read current: < 200 μA at 5.5 V
 - Maximum stand-by current: < 5 μA at 5.5 V
- Operating temperature range
 - - 25°C to + 70°C (commercial)
 - -40° C to +85°C (industrial)
- Operating clock frequencies
 - 100 kHz at standard mode
 - 400 kHz at fast mode
- Electrostatic discharge (ESD)
 - 5,000 V (HBM)
 - 500 V (MM)

Packages

• 8-pin DIP, SOP, and TSSOP



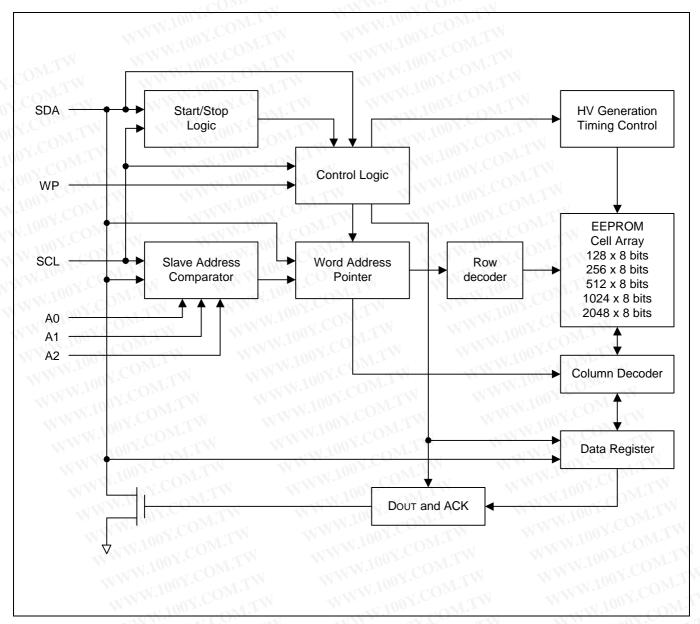


Figure 3-1. S524A40X11/40X21/40X41/60X81/60X51 Block Diagram

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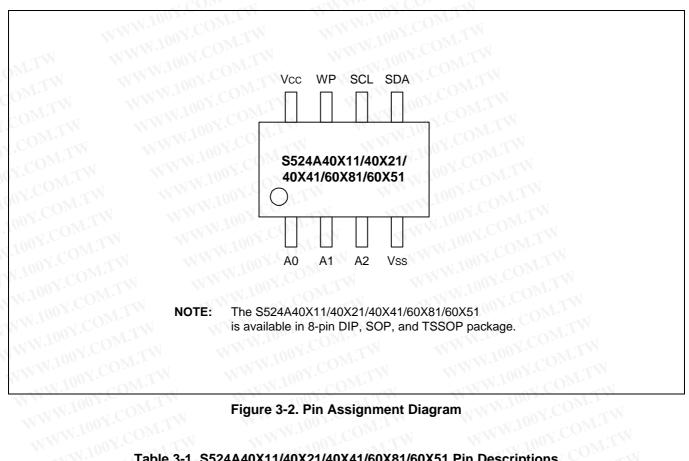
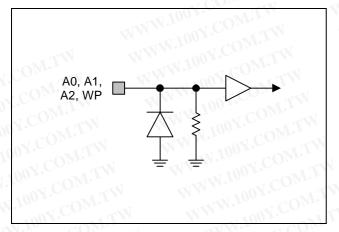


Figure 3-2. Pin Assignment Diagram

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS} .	OM.TV
V _{SS}	MAN - 100	Ground pin.	COMIL
SDA	1/0	Bi-directional data pin for the I^2 C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to $V_{CC.}$ Typical values for this pull-up resistor are 4.7 k Ω (100 kHz) and 1 k Ω (400 kHz).	7.C(3)). 107.CO)
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC} , the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS} , the write function is enabled. This pin is internally pulled down to V_{SS} .	N.1001Y.C
V _{CC}	- 1	Single power supply.	100 - 100

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Figure 3-3. Pin Circuit Type 1

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Figure 3-4. Pin Circuit Type 2

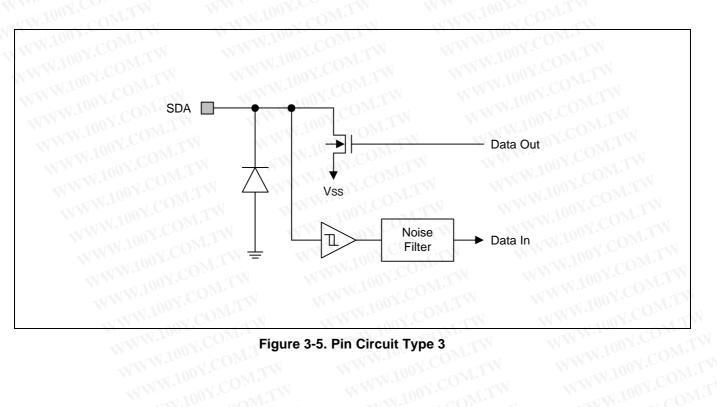


Figure 3-5. Pin Circuit Type 3 WWW.100Y.COM.TW

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FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524A40X11/40X21/40X41/60X81/60X51 supports the I^2 C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as the "transmitter" and any device that gets data from the bus is the "receiver." The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight S524A40X11/40X21 (four S524A40X41, two for S524A60X81, one for S524A60X51) devices can be connected to the same I²C-bus as slaves (see Figure 3-6). Both the master and slaves can operate as transmitter or receiver, but the master device determines which bus operating mode would be active.

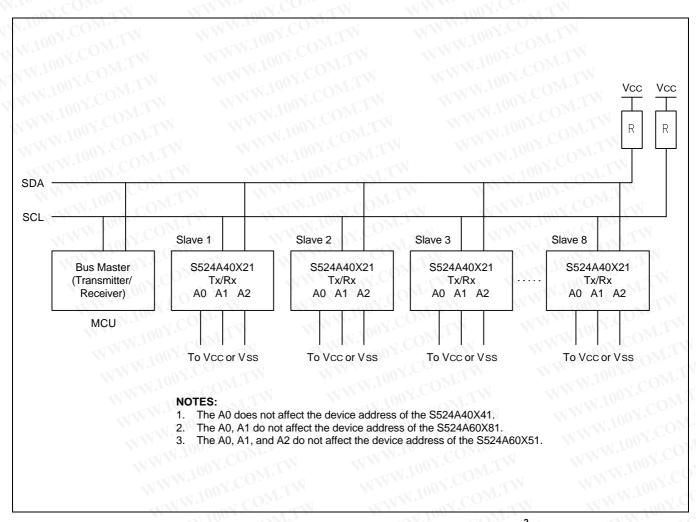


Figure 3-6. Typical Configuration (16 Kbits of Memory on the I²C-Bus)

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I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers

- A new data transfer can be initiated only when the bus is currently not busy.
- MSB is always transferred first in transmitting data.
- During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- <u>Start condition</u>: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- <u>Stop condition</u>: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition (see Figure 3-7).

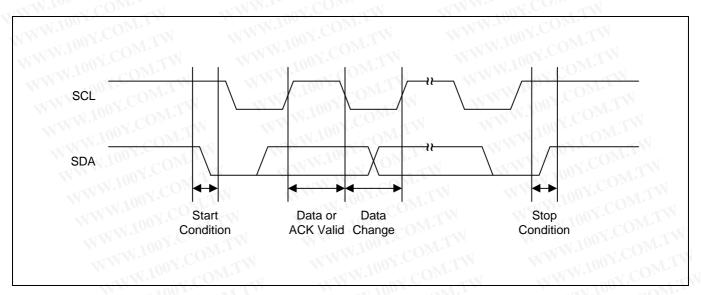


Figure 3-7. Data Transmission Sequence

- <u>Data valid</u>: Following a start condition, the data becomes valid if the data line remains stable for the duration
 of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock
 pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total
 number of bytes that can be transferred in one operation is theoretically unlimited.
- <u>ACK (Acknowledge)</u>: An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 3-8). But the slave does not send an ACK if an internal write cycle is still in progress.
 - In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.



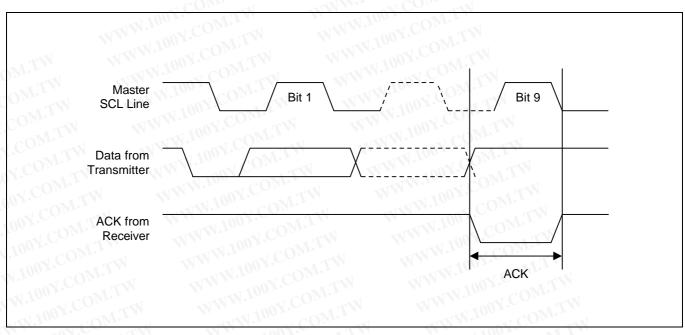


Figure 3-8. Acknowledge Response From Receiver

- <u>Slave Address</u>: After the master initiates a Start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the "device identifier". The identifier for the S524A40X11/40X21/40X41/60X81/60X51 is "1010B". The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1 and A2 pins. Using this addressing scheme, you can cascade up to eight S524A40X11/40X21 or four S524A40X41 or two S524A60X81 or one S524A60X51 on the bus (see Table 3-2 below). The b1 for S524A40X41 or the b1, b2 for S524A60X81 or the b1, b2, b3 for S524A60X51 are used by the master to select which of the blocks of internal memory (1 block = 256 words) are to be accessed. The bits are in effect the most significant bits of the word address.
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is "1", a read operation is executed. If it is "0", a write operation is executed.

Device	Device Identifier			fier Device Address R/W Bi				R/W Bit
	b7	b6	b5	b4	b3	b2	b1	b0 COM
S524A40X11/40X21	N.100	0	1.7	0	A2	A1.00	A0	R/W
S524A40X41	110	0	11	0	A2	1.100 A1 CO	В0	R/W
S524A60X81	11.1	0	1	0	A2	1 B1 CC	B0	R/W
S524A60X51	100	0	1	0	B2	B1	В0	R/W

Table 3-2. Slave Device Addressing

NOTE: The B2, B1, B0 correspond to the MSB of the memory array address word.



BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the S524A40X11/40X21/40X41/60X81/60X51 slave device (see Figure 3-9).

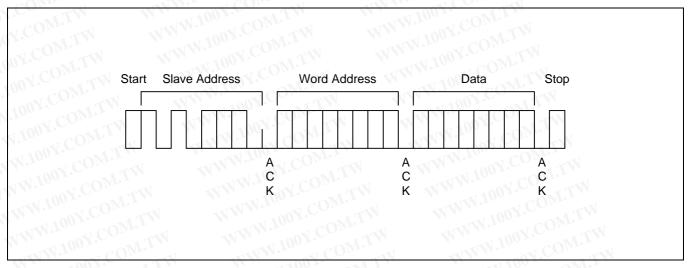


Figure 3-9. Byte Write Operation

Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to "0" onto the bus. Then the addressed S524A40X11/40X21/40X41/60X81/60X51 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the S524A40X11/40X21/40X41/60X81/60X51.

When the S524A40X11/40X21/40X41/60X81/60X51 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the S524A40X11/40X21/40X41/60X81/60X51 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the S524A40X11/40X21/40X41/60X81/60X51 begins the internal write cycle.

While the internal write cycle is in progress, all S524A40X11/40X21/40X41/60X81/60X51 inputs are disabled and the S524A40X11/40X21/40X41/60X81/60X51 does not respond to additional requests from the master.



PAGE WRITE OPERATION

The S524A40X11/40X21/40X41/60X81/60X51 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The S524A40X11/40X21/40X41/60X81/60X51 responds with an ACK each time it receives a complete byte of data (see Figure 3-10).

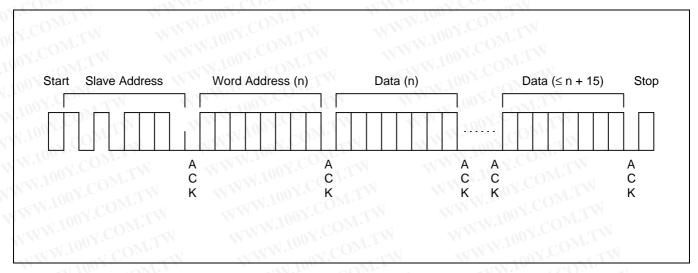


Figure 3-10. Page Write Operation

The S524A40X11/40X21/40X41/60X81/60X51 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.

If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the S524A40X11/40X21/40X41/60X81/60X51 word address pointer value "rolls over" and the previously received data is overwritten. If the master transmits less than 16 bytes and generates a stop condition, the S524A40X11/40X21/40X41/60X81/60X51 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.



DATA SHEET

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524A40X11/40X21/40X41/60X81/60X51 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524A40X11/40X21/40X41/60X81/60X51 remains busy with the write operation, no ACK is returned. When the S524A40X11/40X21/40X41/60X81/60X51 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 3-11).

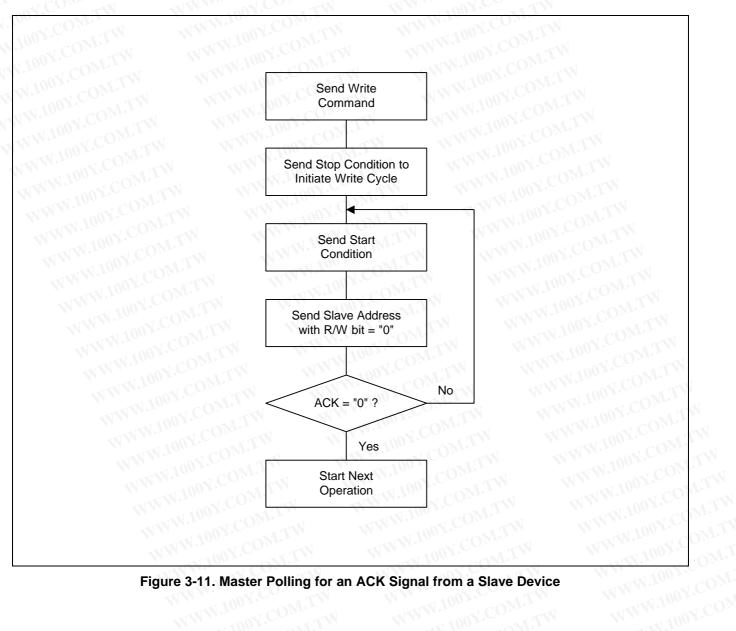


Figure 3-11. Master Polling for an ACK Signal from a Slave Device

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S524A40X11/40X21/40X41/60X81/60X51 SERIAL EEPROM

DATA SHEET

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524A40X11/40X21/40X41/60X81/60X51. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to the memory is ignored.

The S524A40X11/40X21/40X41/60X81/60X51 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated. By connecting the WP pin to V_{SS} , the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address "n", the next read operation would access data at address "n+1".

When the S524A40X11/40X21/40X41/60X81/60X51 receives a slave address with the R/W bit set to "1", it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the S524A40X11/40X21/40X41/60X81/60X51 effectively stops the transmission (see Figure 3-12).

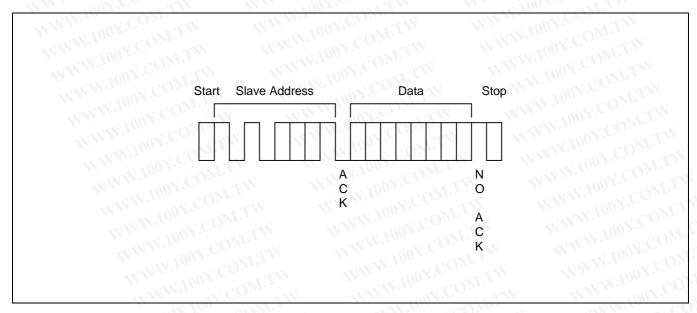


Figure 3-12. Current Address Byte Read Operation



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RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. This operation is performed in the following steps:

- The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the S524A40X11/40X21/40X41/60X81/60X51 to the desired address.)
- 2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to "1".
- The S524A40X11/40X21/40X41/60X81/60X51 then sends an ACK and the 8-bit data stored at the desired address.
- At this point, the master does not acknowledge the transmission, but generates a stop condition instead. 4.
- In response, the S524A40X11/40X21/40X41/60X81/60X51 stops transmitting data and reverts to its stand-by mode (see Figure 3-13).

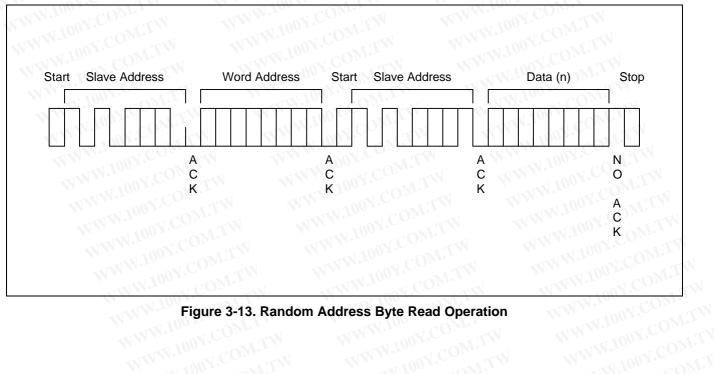


Figure 3-13. Random Address Byte Read Operation

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DATA SHEET

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time, however, the master responds with an ACK, indicating that it requires additional data.

The S524A40X11/40X21/40X41/60X81/60X51 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

Using this method, data is output sequentially with the data from address "n" followed by the data from "n+1". The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer "rolls over" and the S524A40X11/40X21/40X41/60X81/60X51 continues to transmit data for each ACK it receives from the master (see Figure 3-14).

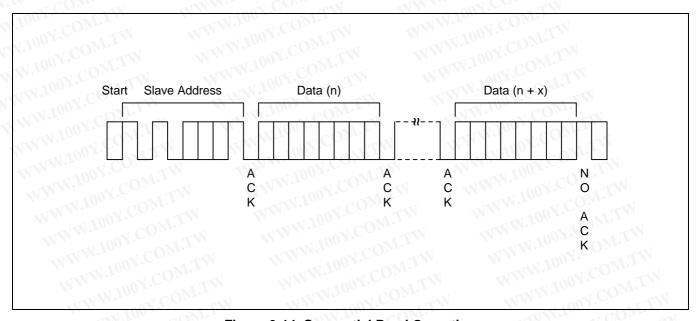


Figure 3-14. Sequential Read Operation

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ELECTRICAL DATA

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Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V _{cc}	OWITH - WWW.	-0.3 to +7.0	V
Input voltage	V _{IN}	CONTLA - MAIN	- 0.3 to + 7.0	V
Output voltage	Vo	COWITY - WW	- 0.3 to + 7.0	V
Operating temperature	TA	A CONTINUE AND	- 40 to + 85	°C
Storage temperature	T _{STG}	ON COM.	- 65 to + 150	°C
Electrostatic discharge	V _{ESD}	НВМ	5000	V
	WWW.	CO MM	500	

Table 3-4. D.C. Electrical Characteristics

TW.100Y.COM.TW $(T_{\Delta} = -25^{\circ}C \text{ to} + 70^{\circ}C (C), -40^{\circ}C \text{ to} + 85^{\circ}C (I), V_{CC} = 1.8 \text{ V to } 5.5 \text{ V})$

Paramet	er	Symbol	Conditions Min		Тур	Max	Unit
Input low voltage	COM	V _{IL}	SCL, SDA, A0, A1, A2	- 1	WW-100	0.3 V _{CC}	V
Input high voltage Input leakage current		V _{IH}	WW.100X.COM.TW	0.7 V _{CC}	W 14.10	COM.	V
			$V_{IN} = 0$ to V_{CC}	<u> </u>	WWW.I	10	μΑ
Output leakage c	urrent	nt I_{LO} $V_O = 0$ to V_{CC}		10	μA		
Output low voltage		V _{OL}	$I_{OL} = 0.15 \text{ mA}, V_{CC} = 1.8 \text{ V}$	TW-	WW.	0.2	V
		COWIT	$I_{OL} = 2.1 \text{ mA}, V_{CC} = 2.5 \text{ V}$	TV	WW	0.4	
Supply current	pply current Write	CI _{CC1}	V _{CC} = 5.5 V, 400 kHz	177	-111	3	mA
		I _{CC2}	V _{CC} = 1.8 V, 100 kHz	WEM	- 11	1,007	
	Read	I _{CC3}	V _{CC} = 5.5 V, 400 kHz	-ON-TW	- 1	0.2	
	WWW	I _{CC4}	V _{CC} = 1.8 V, 100 kHz	CONLIN	_	60	μA
Stand-by current	MMM	I _{CC5}	V _{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	Y.COM.	_	5	μА
		I _{CC6}	V _{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	OY.COM	TVL CTW	11	

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Table 3-4. D.C. Electrical Characteristics (Continued)

 $(T_A = -25^{\circ}C \text{ to } + 70^{\circ}C \text{ (C)}, -40^{\circ}C \text{ to } + 85^{\circ}C \text{ (I)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V)}$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input capacitance	C _{IN}	25 °C, 1MHz, V _{CC} = 5 V, V _{IN} = 0 V, A0, A1, A2, SCL and WP pin	M.TW OM.TV	_	10	pF
Input/output capacitance	C _{I/O}	25 °C, 1MHz, V _{CC} = 5 V, V _{I/O} = 0 V, SDA pin	COMI.	r ZW TW	10	

Table 3-5. A.C. Electrical Characteristics

 $(T_A = -\,25^{\circ}C$ to + $70^{\circ}C$ (C), $-\,40^{\circ}C$ to + $85^{\circ}C$ (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		8 to 5.5 V rd Mode)		5 to 5.5 V Mode)	Unit
	WW	N.100X.COD	Min	Max	Min	Max	
External clock frequency	F _{CLK}	W.100Y.CO	0	100	.1000	400	kHz
Clock high time	t _{HIGH}	N.1001.	4	-71/1/	0.6	DM:	μs
Clock low time	t _{LOW}	WW.1002	4.7	- 1	1.3	COM-TAN	
Rising time	t _R	SDA, SCL	COM.	1	MM-100	0.3	Ŋ.
Falling time	t _F	SDA, SCL	I.COZII.	0.3	MAN-100	0.3	N
Start condition hold time	t _{HD:STA}	MATA	X.C4	- W	0.6	N.Con	IN
Start condition setup time	t _{SU:STA}	WAW.	4.7	- WI	0.6	007.COS	TW
Data input hold time	t _{HD:DAT}	WIN W.	0010	LIV	0	1001-60	WT.IV
Data input setup time	t _{SU:DAT}	AMA	0.25	M.T.W	0.1	11.1007.00	M.TV
Stop condition setup time	t _{SU:STO}	-4144	4	DM.TW	0.6	W.1001.	OM.T
Bus free time	t _{BUF}	Before new transmission	4.7	COMTW	1.3	1. 100 X	COM:
Data output valid from clock low ^(note)	t _{AA}	W - W	0.3	3.5	N - 1	0.9	X.CO
Noise spike width	t _{SP}	TW -	MAN	100	W -	50	ns
Write cycle time	t _{WR}	TV	MATMY	5	-WT	5	ms

NOTES

- 1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
- When acting as a transmitter, the S524A40X11/40X21/40X41/60X81/60X51 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.



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DATA SHEET

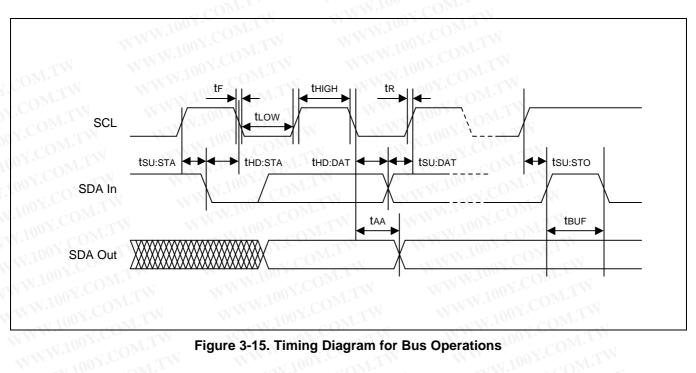


Figure 3-15. Timing Diagram for Bus Operations

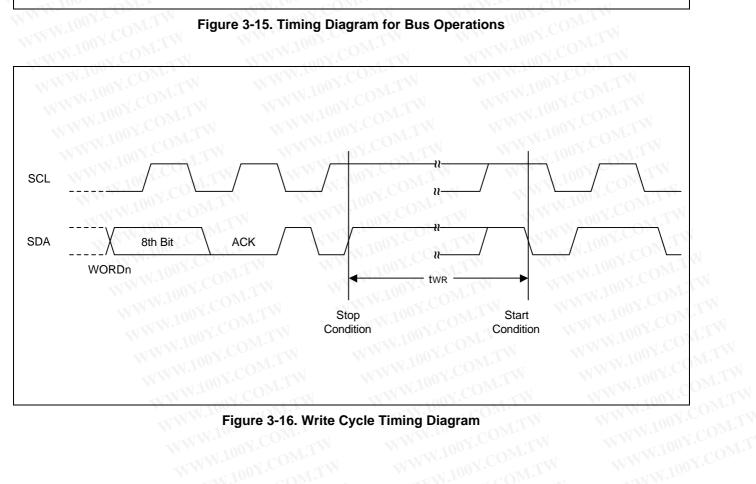


Figure 3-16. Write Cycle Timing Diagram WWW.toox.CO WWW.100Y.COM.TW

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S524AB0X91/B0XB1

32K/64K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524AB0X91/B0XB1 serial EEPROM has a 32K/64K-bit (4,096/8,192 bytes) capacity, supporting the standard I²C[™]-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 32 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524AB0X91/B0XB1 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 32K/64K-bit (4,096/8,192 bytes) storage area
- 32-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

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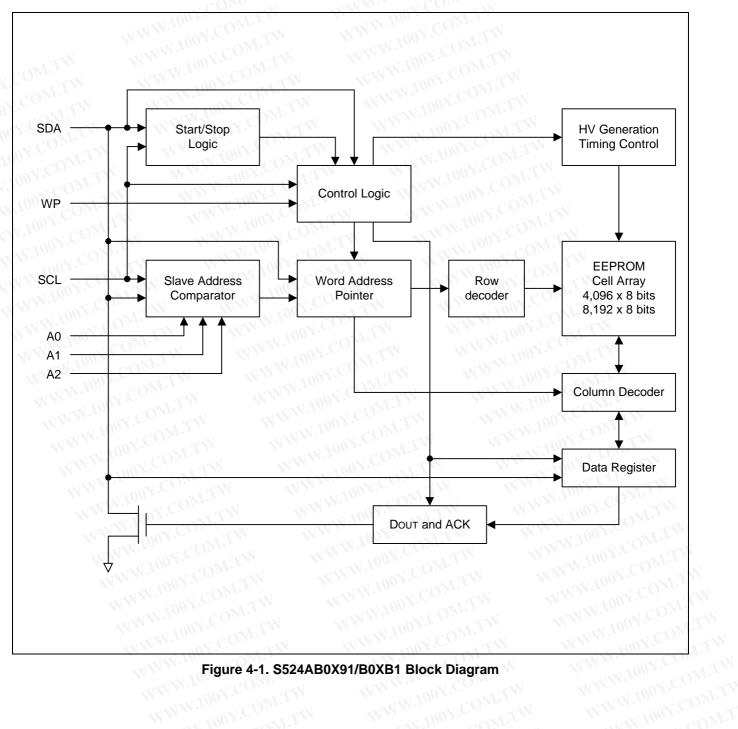
Operating Characteristics

- Operating voltage
 - 1.8 V to 5.5 V
- Operating current
 - Maximum write current: < 3 mA at 5.5 V
 - Maximum read current: < 400 μA at 5.5 V
 - Maximum stand-by current: < 5 μA at 5.5 V
- Operating temperature range
 - - 25°C to + 70°C (commercial)
 - – 40°C to + 85°C (industrial)
- Operating clock frequencies
 - 100 kHz at standard mode
 - 400 kHz at fast mode
- Electrostatic discharge (ESD)
 - 5,000 V (HBM)
 - 500 V (MM)

Packages

• 8-pin DIP, SOP, and TSSOP





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Figure 4-1. S524AB0X91/B0XB1 Block Diagram WWW.100Y.CO. 1.100Y.COM.TW

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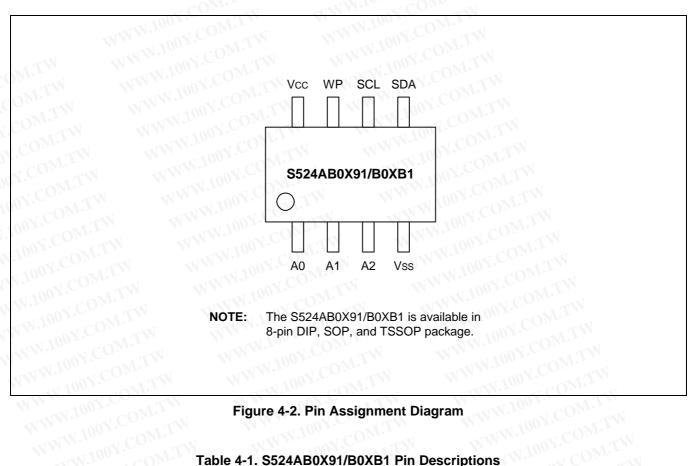


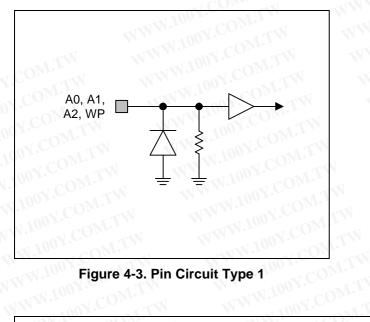
Figure 4-2. Pin Assignment Diagram

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS} .	OM.TW OM.TW
V _{SS} \checkmark	WW. 100	Ground pin.	COALIA
SDA	1/0	Bi-directional data pin for the I^2 C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V_{DD} . Typical values for this pull-up resistor are 4.7 K Ω (100 KHz) and 1 K Ω (400 KHz).	M.COM.
SCL	Input	Schmitt trigger input pin for serial clock input.	1002
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC} , the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS} , the write function is enabled. This pin is internally pulled down to V_{SS} .	M. 100 X.C. M. 100 X.C. M. 100 X.C.
V _{CC}	_	Single power supply.	MAFin

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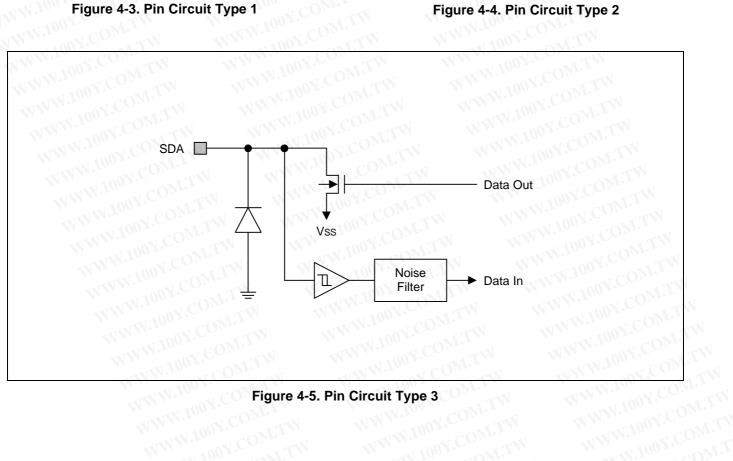




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Figure 4-3. Pin Circuit Type 1

Figure 4-4. Pin Circuit Type 2



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FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524AB0X91/B0XB1 supports the I^2 C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as a "transmitter" and any device that gets data from the bus is a "receiver." The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight S524AB0X91/B0XB1 devices can be connected to the same I²C-bus as slaves (see Figure 4-6). Both the master and slaves can operate as a transmitter or a receiver, but the master device determines which bus operating mode would be active.

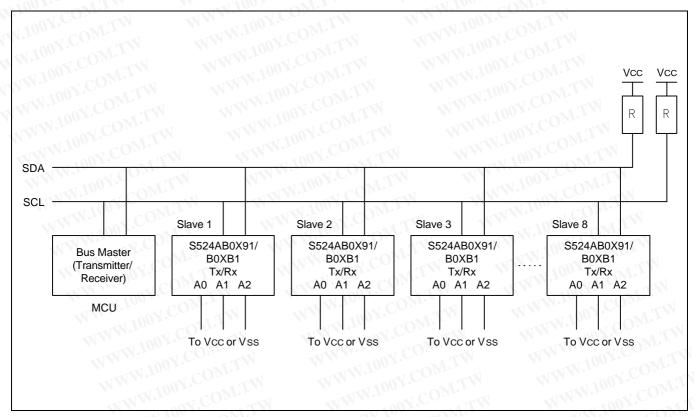


Figure 4-6. Typical Configuration



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I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

- A new data transfer can be initiated only when the bus is currently not busy.

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- MSB is always transferred first in transmitting data.
- During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain in High level when the bus is not active.
- <u>Start condition</u>: A start condition is initiated by a High-to-Low transition of the SDA line while SCL remains in High level. All bus commands must be preceded by a start condition.
- <u>Stop condition</u>: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains in High level. All bus operations must be completed by a stop condition (see Figure 4-7).

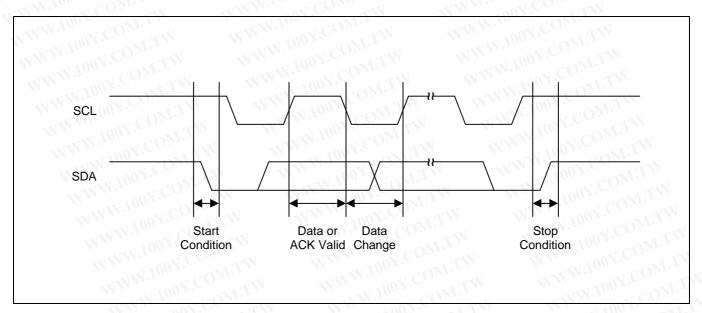


Figure 4-7. Data Transmission Sequence

- <u>Data valid</u>: Following a start condition, the data becomes valid if the data line remains stable for the duration
 of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock
 pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total
 number of bytes that can be transferred in one operation is theoretically unlimited.
- <u>ACK (Acknowledge)</u>: An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it has successfully received the eight bits of data (see Figure 4-8). But the slave does not send an ACK if an internal write cycle is still in progress.

In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected but no stop condition, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.



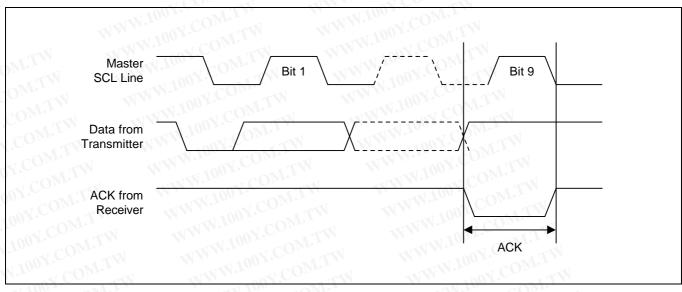


Figure 4-8. Acknowledge Response From Receiver

- <u>Slave Address</u>: After the master initiates a start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the "device identifier." The identifier for the S524AB0X91/B0XB1 is "1010B". The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1, and A2 pins. Using this addressing scheme, you can cascade up to eight S524AB0X91/B0XB1s on the bus (see Figure 4-9 below).
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is "1", a read operation is executed. If it is "0", a write operation is executed.

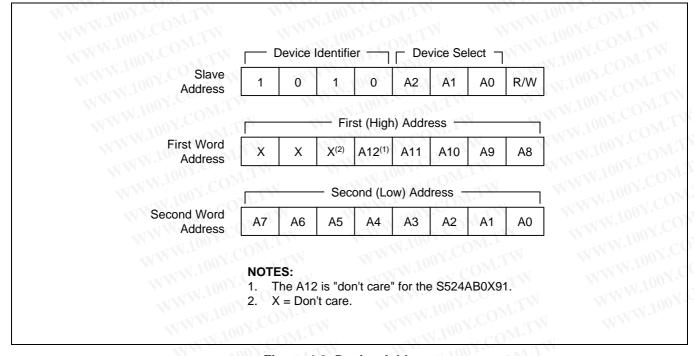


Figure 4-9. Device Address



BYTE WRITE OPERATION

A write operation requires 2-byte word addresses, the first (high) word address and the second (low) word address. In a byte write operation, the master transmits the slave address, the first word address, the second word address, and one data byte to the S524AB0X91/B0XB1 slave device (see Figure 4-10).

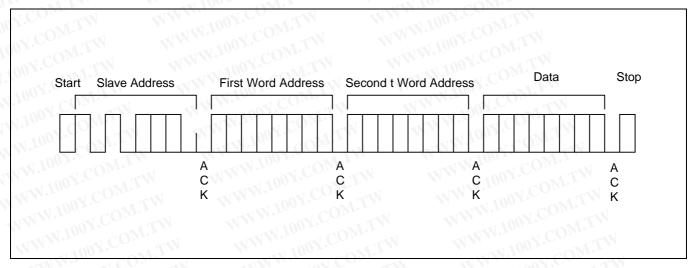


Figure 4-10. Byte Write Operation

Following a start condition, the master puts the device identifier (4 bits), the device address (3 bits), and an R/W bit set to "0" onto the bus. Upon the receipt of the slave address, the S524AB0X91/B0XB1 responds with an ACK. And the master transmits the first word address, the second word address, and one byte data to be written into the addressed memory location.

The master terminates the transfer by generating a stop condition, at which time the S524AB0X91/B0XB1 begins the internal write cycle. While the internal write cycle is in progress, all S524AB0X91/B0XB1 inputs are disabled and the S524AB0X91/B0XB1 does not respond to any additional request from the master.



PAGE WRITE OPERATION

The S524AB0X91/B0XB1 can also perform 32-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 31 additional bytes. The S524AB0X91/B0XB1 responds with an ACK each time it receives a complete byte of data (see Figure 4-11).

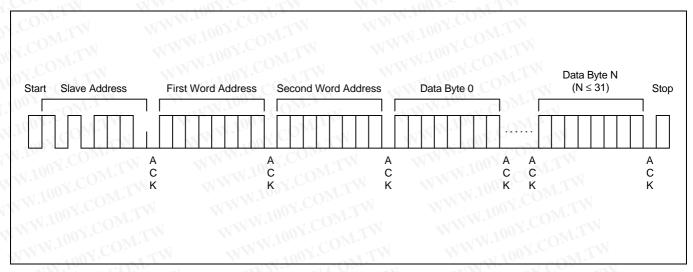


Figure 4-11. Page Write Operation

The S524AB0X91/B0XB1 automatically increments the word address pointer each time it receives a complete data byte. When one byte is received, the internal word address pointer increments to the next address so that the next data byte can be received.

If the master transmits more than 32 bytes before it generates a stop condition to end the page write operation, the S524AB0X91/B0XB1 word address pointer value "rolls over" and the previously received data is overwritten. If the master transmits less than 32 bytes and generates a stop condition, the S524AB0X91/B0XB1 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there would be no response to additional requests from the master until the internal write cycle is completed.



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POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524AB0X91/B0XB1 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device to determine whether the write cycle is completed.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524AB0X91/B0XB1 remains busy with the write operation, no ACK is returned. When the S524AB0X91/B0XB1 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 4-12).

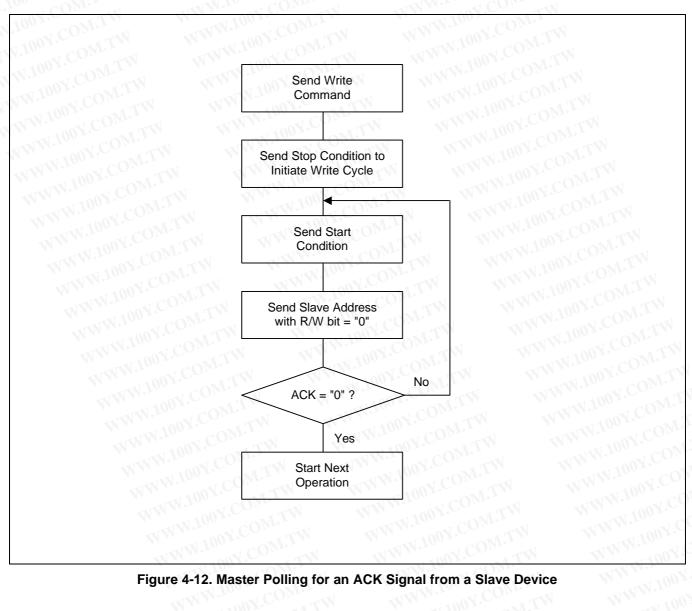


Figure 4-12. Master Polling for an ACK Signal from a Slave Device

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HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524AB0X91/B0XB1. This write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC} , any attempt to write a value to it is ignored. The S524AB0X91/B0XB1 will acknowledge slave and word addresses, but it will not generate an acknowledge after receiving the first byte of data. In this situation, the write cycle will not be started when a stop condition is generated. By connecting the WP pin to V_{SS} , the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to protect data from being overwritten. Whenever the write function is disabled, a slave address and word addresses are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address "n", the next read operation would be to access data at address "n+1".

When the S524AB0X91/B0XB1 receives a slave address with the R/W bit set to "1", it issues an ACK and sends the eight bits of data. In a current address byte read operation, the master does not acknowledge the data, and it generates a stop condition, forcing the S524AB0X91/B0XB1 to stop the transmission (see Figure 4-13).

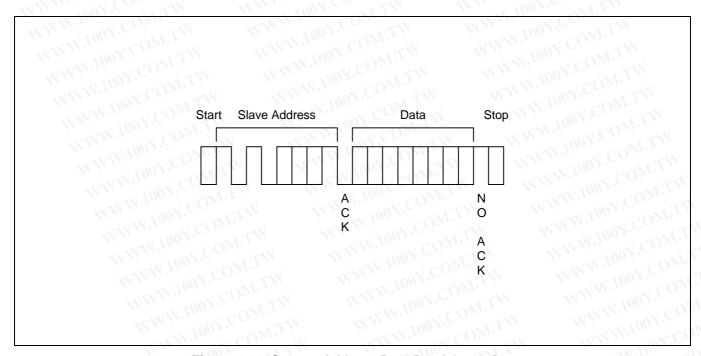


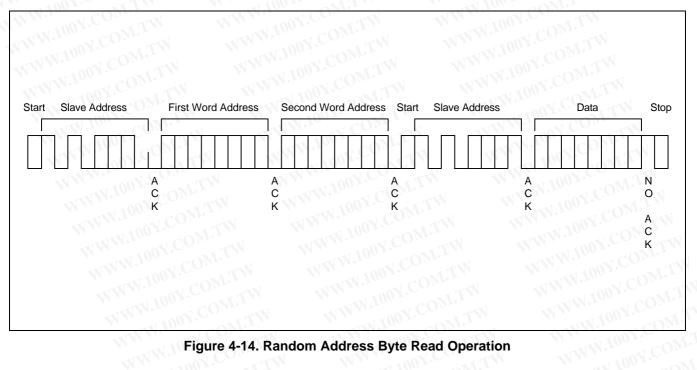
Figure 4-13. Current Address Byte Read Operation



RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. This operation is performed in the following steps:

- The master first issues a start condition, the slave address, and the word address (the first and the second addresses) to be read. (This step sets the internal word address pointer of the S524AB0X91/B0XB1 to the desired address.)
- When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to "1".
- The S524AB0X91/B0XB1 then sends an ACK and the 8-bit data stored at the pointed address.
- At this point, the master does not acknowledge the transmission, generating a stop condition.
- 5. The S524AB0X91/B0XB1 stops transmitting data and reverts to stand-by mode (see Figure 4-14).



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SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: current address sequential read operation, and random address sequential read operation. The first data is sent in either of the two ways, current address byte read operation or random address byte read operation described earlier. If the master responds with an ACK, the S524AB0X91/B0XB1 continues transmitting data. If the master does not issue an ACK, generating a stop condition, the slave stops transmission, ending the sequential read operation.

Using this method, data is output sequentially from address "n" followed by address "n+1". The word address pointer for read operations increments to all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer "rolls over" and the S524AB0X91/B0XB1 continues to transmit data for each ACK it receives from the master (see Figure 4-15).

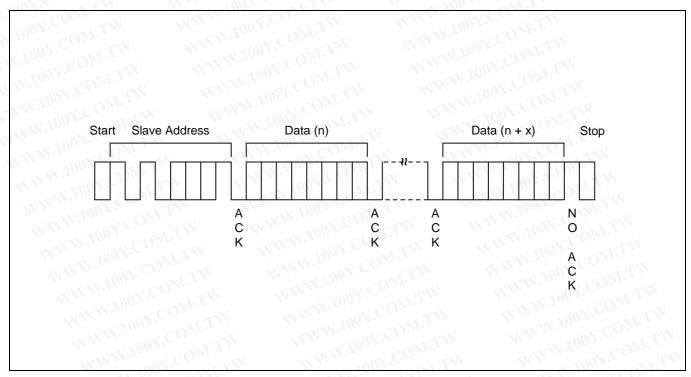


Figure 4-15. Sequential Read Operation



ELECTRICAL DATA

WWW.100Y.COM.TW Table 4-2. Absolute Maximum Ratings

 $(T_A = 25^{\circ}C)$

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V _{cc}	WITH - WINN	-0.3 to +7.0	V
Input voltage	V _{IN}	Mil - MAN	-0.3 to +7.0	V
Output voltage	Vo	ON.THE	-0.3 to +7.0	V
Operating temperature	TA	COW. I. WAY	- 40 to + 85	°C
Storage temperature	T _{STG}	COM.	- 65 to + 150	°C
Electrostatic discharge	V _{ESD}	HBM	5000	V
	WW. To.	MM N	500	1

Table 4-3. D.C. Electrical Characteristics

 $(T_A = -25^{\circ}C \text{ to} + 70^{\circ}C \text{ (Commercial)}, -40^{\circ}C \text{ to} + 85^{\circ}C \text{ (Industrial)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V})$

Paramet	er	Symbol	Conditions	Min	Тур	Max	Unit
Input low voltage	· COM!	V _{IL}	SCL, SDA, A0, A1, A2	_ ~	NN-100	0.3 V _{CC}	V
Input high voltage	MOD E	V _{IH}	WW.100Y.COM.TW	0.7 V _{CC}	W\ \\ 10	A COM	V
Input leakage cur	ge current I _{LI} V		$V_{IN} = 0$ to V_{CC}	\	N-W-W.1	10	μA
Output leakage c	tput leakage current I _{LO}		$V_O = 0$ to V_{CC}		WWW	10	μA
Output low voltage		V _{OL}	$I_{OL} = 0.15 \text{ mA}, V_{CC} = 1.8 \text{ V}$	TW-	W-WW	0.2	V
		COMIT	$I_{OL} = 2.1 \text{ mA}, V_{CC} = 2.5 \text{ V}$	CTV	MM	0.4	
Supply current	Write	CI _{CC1}	$V_{CC} = 5.5 \text{ V}, 400 \text{ kHz}$	N TW	-111	3	mA
	W.100	I _{CC2}	V _{CC} = 1.8 V, 100 kHz	WIN	- 1/	1,007	
	Read	I _{CC3}	V _{CC} = 5.5 V, 400 kHz	ONETAI	- 1	0.4	
	WW.	I _{CC4}	V _{CC} = 1.8 V, 100 kHz	CONTIN	_	60	μA
Stand-by current	MMM	I _{CC5}	V _{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	X = OM	M _	5	μA
		I _{CC6}	V _{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	OY.COM	TVL CTW	1	

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Table 4-3. D.C. Electrical Characteristics (Continued)

 $(T_A = -25^{\circ}C \text{ to } + 70^{\circ}C \text{ (Commercial)}, -40^{\circ}C \text{ to } + 85^{\circ}C \text{ (Industrial)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V)}$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input capacitance	C _{IN}	25°C, 1MHz, V _{CC} = 5 V, V _{IN} = 0 V, A0, A1, A2, SCL and WP pin	cow_{TA}	- N	10	pF
Input/Output capacitance	C _{I/O}	25° C, 1MHz, V _{CC} = 5 V, V _{I/O} = 0 V, SDA pin	Y.COM	TW TW	10	

Table 4-4. A.C. Electrical Characteristics

 $(T_A = -25^{\circ}C \text{ to } + 70^{\circ}C \text{ (Commercial)}, -40^{\circ}C \text{ to } + 85^{\circ}C \text{ (Industrial)}, V_{CC} = 1.8 \text{ V to } 5.5 \text{ V)}$

Parameter	Symbol	mbol Conditions		V _{CC} = 1.8 to 5.5 V (Standard Mode)		V _{CC} = 2.5 to 5.5 V (Fast Mode)		
	MM	N.100Y. CON	Min	Max	Min	Max		
External clock frequency	F _{clk}	W.1007.CO	0	100 (1)	1000	400 (1)	kHz	
Clock High time	t _{HIGH}	M.1001.	4	-	0.6	DM: T	μs	
Clock Low time	t _{LOW}	M.700 2.	4.7	- 111	1.3	COM	μs	
Rising time	t _R	SDA, SCL	COM.	1	MM.Too	0.3	μs	
Falling time	t _F	SDA, SCL	COM	0.3	MA	0.3	N μs	
Start condition hold time	t _{HD:STA}	MATH	V.C4	- W	0.6	N.Con	Mμs	
Start condition setup time	t _{SU:STA}	WAW	4.7	TW -	0.6	DOY.COM	μs	
Data input hold time	t _{HD:DAT}	WELL AND	0010	LIV	0	1001-001	μs	
Data input setup time	t _{SU:DAT}	AMA	0.25	MIT	0.1	11.1007	μs	
Stop condition setup time	t _{SU:STO}	-M.M.	104	OM.TW	0.6	N.100	μs	
Bus free time	t _{BUF}	Before new transmission	4.7	COMITY	1.3	MAN 100X	μs	
Data output valid from clock low ⁽²⁾	t _{AA}	W - W	0.3	3.5	- V	0.9	μѕ	
Noise spike width	t _{SP}	TW-	MANT	100	W -	50	ns	
Write cycle time	t _{WR}	TVI-	MATMI	5	- WT	5	ms	

NOTES:

- 1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
- When acting as a transmitter, the S524AB0X91/B0XB1 must provide an internal minimum delay time to bridge the
 undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a
 start or stop condition.



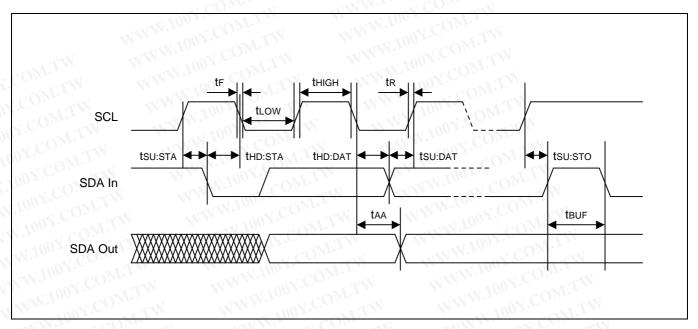
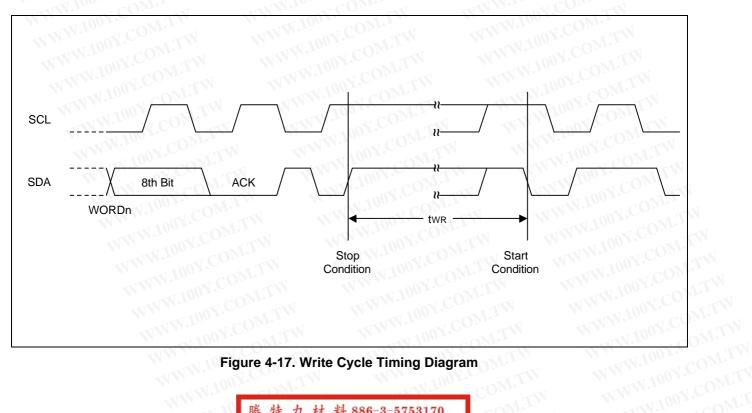


Figure 4-16. Timing Diagram for Bus Operations



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\$524AD0XD1/D0XF1

128K/256K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524AD0XD1/D0XF1 serial EEPROM has a 128K/256K-bit (16,384/32,768 bytes) capacity, supporting the standard I²C[™]-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 64 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524AD0XD1/D0XF1 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 128K/256K-bit (16,384/32,768 bytes) storage area
- 64-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 500,000 erase/write cycles
- 50 years data retention

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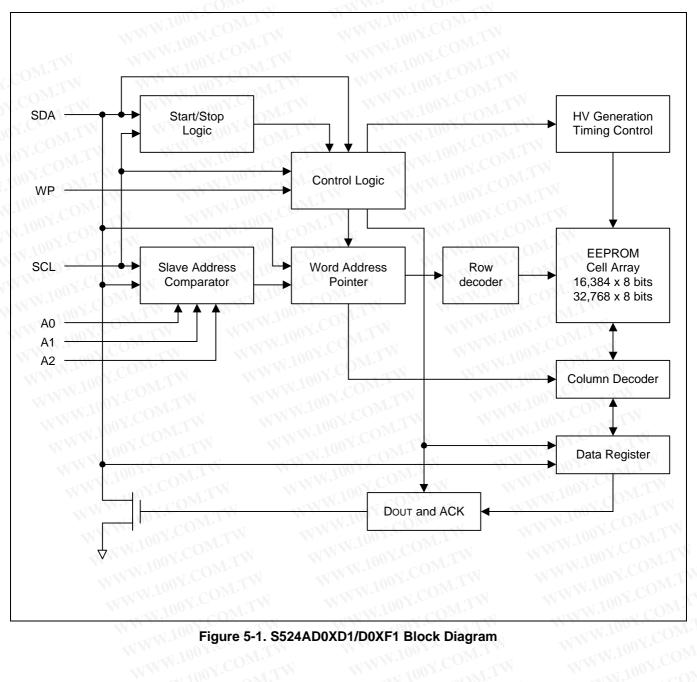
Operating Characteristics

- Operating voltage
 - 1.8 V to 5.5 V
- Operating current
 - Maximum write current: < 3 mA at 5.5 V
 - Maximum read current: < 400 μA at 5.5 V
 - Maximum stand-by current: < 5 μA at 5.5 V
- Operating temperature range
 - - 25°C to + 70°C (commercial)
 - - 40°C to + 85°C (industrial)
- Operating clock frequencies
 - 400 kHz at standard mode
 - 1 MHz at fast mode
- Electrostatic discharge (ESD)
 - 5,000 V (HBM)
 - 500 V (MM)

Packages

8-pin DIP, and TSSOP





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Figure 5-1. S524AD0XD1/D0XF1 Block Diagram WWW.100 WWW.100Y.COM.T

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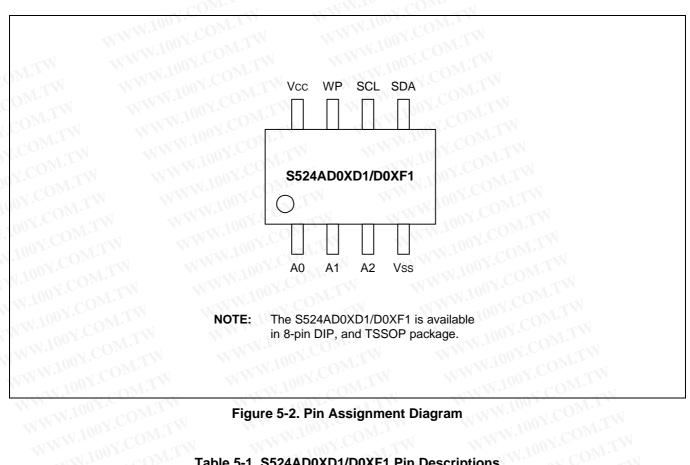


Figure 5-2. Pin Assignment Diagram

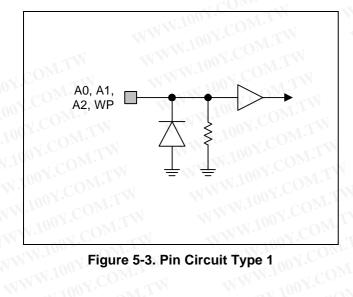
Table 5-1. S524AD0XD1/D0XF1 Pin Descriptions

Name	Туре	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS} .	OM.TW
V _{SS}	M.W. 1002	Ground pin.	COM
SDA	I/O	Bi-directional data pin for the I 2 C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V $_{DD}$. Typical values for this pull-up resistor are 4.7 K Ω (100 KHz) and 1 K Ω (400 KHz).	7.C(3M) 1007.CON
SCL	Input	Schmitt trigger input pin for serial clock input.	1002
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC} , the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS} , the write function is enabled. This pin is internally pulled down to V_{SS} .	N.100X N.100X N.100X
V _{CC}	`	Single power supply.	MAG

WWW.100X.

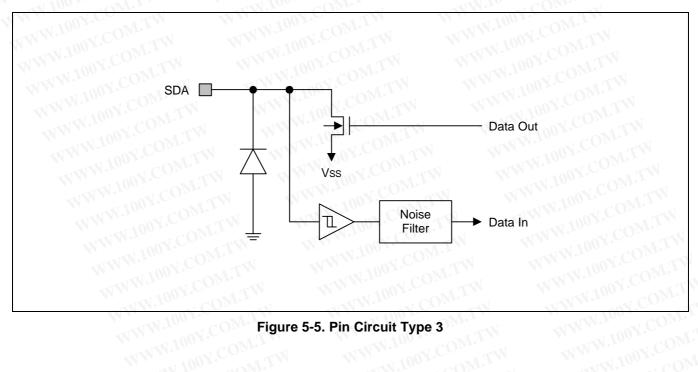
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W.100Y.COM. NW.100Y.COM.TW WW.100Y.COM.TW WW Noise SCL -Eilter COM.TW WWW.100Y YWW.100Y.COM.TW WWW.100\\\

Figure 5-4. Pin Circuit Type 2



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WWW.100Y.COM.TW Figure 5-5. Pin Circuit Type 3 WWW.100Y.COM.

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FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524AD0XD1/D0XF1 supports the I^2 C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as a "transmitter" and any device that gets data from the bus is a "receiver." The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight S524AD0XD1/D0XF1 devices can be connected to the same I²C-bus as slaves (see Figure 5-6). Both the master and slaves can operate as a transmitter or a receiver, but the master device determines which bus operating mode would be active.

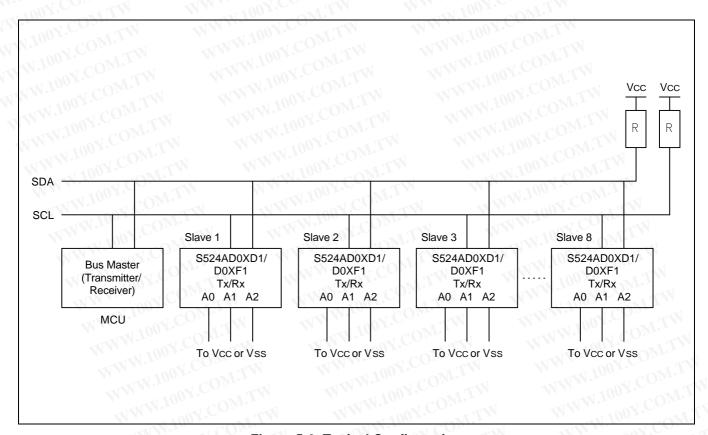


Figure 5-6. Typical Configuration



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I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers

- A new data transfer can be initiated only when the bus is currently not busy.
- MSB is always transferred first in transmitting data.
- During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain in High level when the bus is not active.
- <u>Start condition</u>: A start condition is initiated by a High-to-Low transition of the SDA line while SCL remains in High level. All bus commands must be preceded by a start condition.
- <u>Stop condition</u>: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains in High level. All bus operations must be completed by a stop condition (see Figure 5-7).

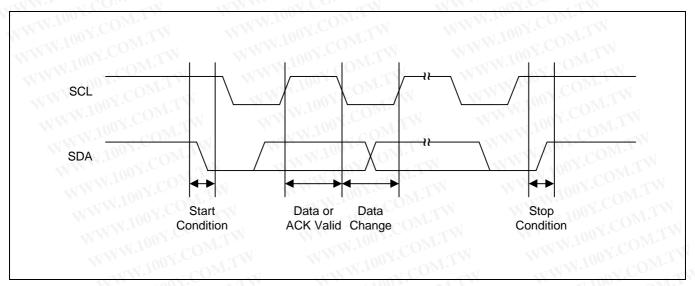


Figure 5-7. Data Transmission Sequence

- <u>Data valid</u>: Following a start condition, the data becomes valid if the data line remains stable for the duration
 of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock
 pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total
 number of bytes that can be transferred in one operation is theoretically unlimited.
- <u>ACK (Acknowledge)</u>: An ACK signal indicates that a data transfer is completed successfully. The transmitter
 (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master
 generates, the receiver pulls the SDA line low to acknowledge that it has successfully received the eight bits
 of data (see Figure 5-8). But the slave does not send an ACK if an internal write cycle is still in progress.

In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected but no stop condition, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.



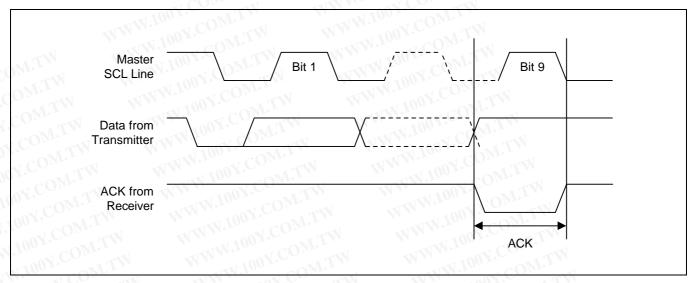


Figure 5-8. Acknowledge Response from Receiver

- <u>Slave Address</u>: After the master initiates a start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the "device identifier." The identifier for the S524AD0XD1/D0XF1 is "1010B". The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1, and A2 pins. Using this addressing scheme, you can cascade up to eight S524AD0XD1/D0XF1s on the bus (see Figure 5-9 below).
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is "1", a read operation is executed. If it is "0", a write operation is executed.

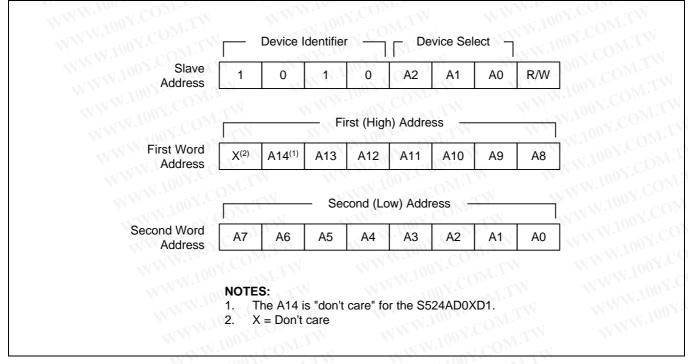


Figure 5-9. Device Address



BYTE WRITE OPERATION

A write operation requires 2-byte word addresses, the first (high) word address and the second (low) word address. In a byte write operation, the master transmits the slave address, the first word address, the second word address, and one data byte to the S524AD0XD1/D0XF1 slave device (see Figure 5-10).

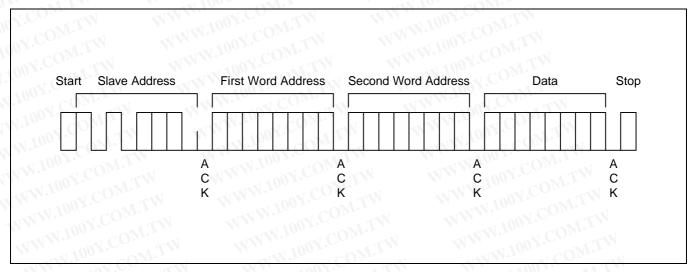


Figure 5-10. Byte Write Operation

Following a start condition, the master puts the device identifier (4 bits), the device address (3 bits), and an R/W bit set to "0" onto the bus. Upon the receipt of the slave address, the S524AD0XD1/D0XF1 responds with an ACK. And the master transmits the first word address, the second word address, and one byte data to be written into the addressed memory location.

The master terminates the transfer by generating a stop condition, at which time the S524AD0XD1/D0XF1 begins the internal write cycle. While the internal write cycle is in progress, all S524AD0XD1/D0XF1 inputs are disabled and the S524AD0XD1/D0XF1 does not respond to any additional request from the master.



PAGE WRITE OPERATION

The S524AD0XD1/D0XF1 can also perform 64-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 63 additional bytes. The S524AD0XD1/D0XF1 responds with an ACK each time it receives a complete byte of data (see Figure 5-11).

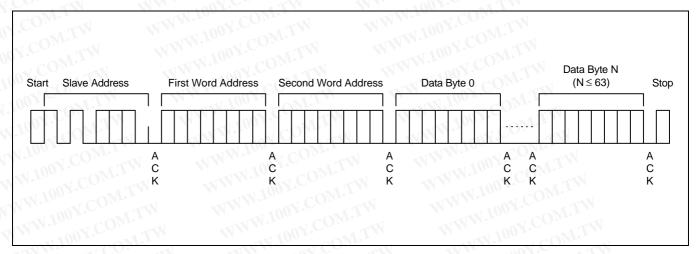


Figure 5-11. Page Write Operation

The S524AD0XD1/D0XF1 automatically increments the word address pointer each time it receives a complete data byte. When one byte is received, the internal word address pointer increments to the next address so that the next data byte can be received.

If the master transmits more than 64 bytes before it generates a stop condition to end the page write operation, the S524AD0XD1/D0XF1 word address pointer value "rolls over" and the previously received data is overwritten. If the master transmits less than 64 bytes and generates a stop condition, the S524AD0XD1/D0XF1 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there would be no response to additional requests from the master until the internal write cycle is completed.

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DATA SHEET

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524AD0XD1/D0XF1 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device to determine whether the write cycle is completed.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524AD0XD1/D0XF1 remains busy with the write operation, no ACK is returned. When the S524AD0XD1/D0XF1 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 5-12).

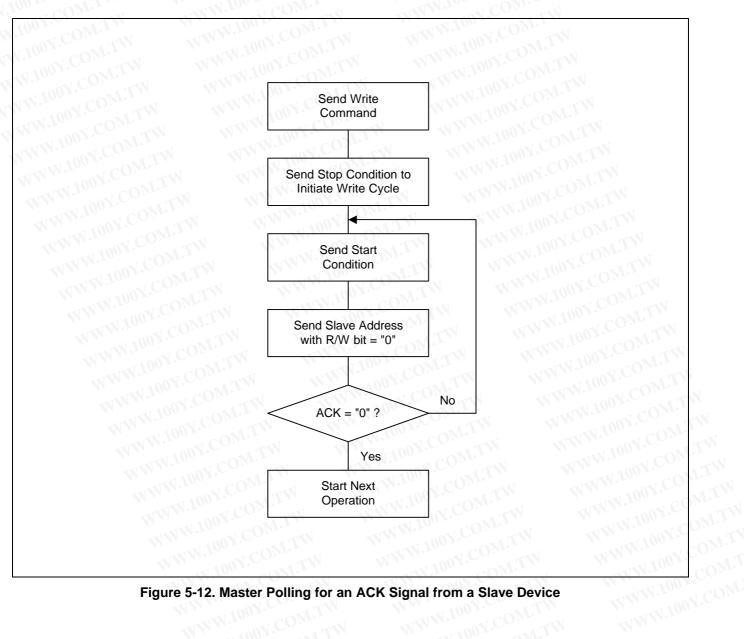


Figure 5-12. Master Polling for an ACK Signal from a Slave Device

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HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524AD0XD1/D0XF1. This write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC} , any attempt to write a value to it is ignored. The S524AD0XD1/D0XF1 will acknowledge slave address, word address, and data bytes. But the write cycle will not be started when a stop condition is generated. By connecting the WP pin to V_{SS} , the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to protect data from being overwritten.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address "n", the next read operation would be to access data at address "n+1".

When the S524AD0XD1/D0XF1 receives a slave address with the R/W bit set to "1", it issues an ACK and sends the eight bits of data. In a current address byte read operation, the master does not acknowledge the data, and it generates a stop condition, forcing the S524AD0XD1/D0XF1 to stop the transmission (see Figure 5-13).

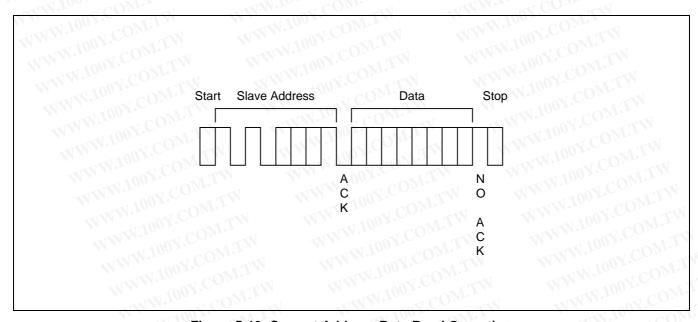


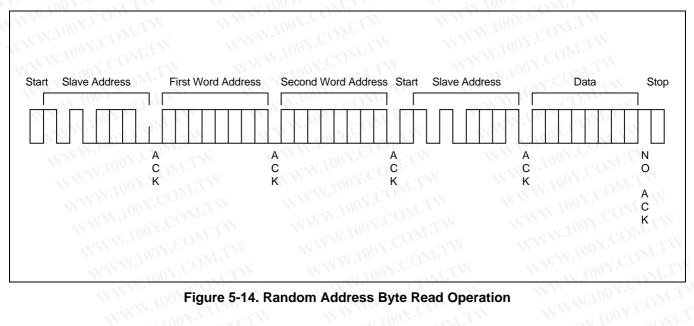
Figure 5-13. Current Address Byte Read Operation



RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. This operation is performed in the following steps:

- The master first issues a start condition, the slave address, and the word address (the first and the second addresses) to be read. (This step sets the internal word address pointer of the S524AD0XD1/D0XF1 to the desired address.)
- When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to "1".
- The S524AD0XD1/D0XF1 then sends an ACK and the 8-bit data stored at the pointed address.
- At this point, the master does not acknowledge the transmission, generating a stop condition.
- 5. The S524AD0XD1/D0XF1 stops transmitting data and reverts to stand-by mode (see Figure 5-14).



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SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: current address sequential read operation, and random address sequential read operation. The first data is sent in either of the two ways, current address byte read operation or random address byte read operation described earlier. If the master responds with an ACK, the S524AD0XD1/D0XF1 continues transmitting data. If the master does not issue an ACK, generating a stop condition, the slave stops transmission, ending the sequential read operation.

Using this method, data is output sequentially from address "n" followed by address "n+1". The word address pointer for read operations increments to all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer "rolls over" and the S524AD0XD1/D0XF1 continues to transmit data for each ACK it receives from the master (see Figure 5-15).



Figure 5-15. Sequential Read Operation



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ELECTRICAL DATA

WWW.100Y.COM.TW Table 5-2. Absolute Maximum Ratings

WWW.100Y

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Parameter	Symbol	Conditions	Rating	Uni
Supply voltage	V _{CC}	ONITY - WWW.1	- 0.3 to + 7.0	V
Input voltage	V _{IN}	CONT MAIN	-0.3 to +7.0	V
Output voltage	Vo	COW.I	-0.3 to +7.0	V
Operating temperature	T _A	A CONTRACTOR	- 40 to +85	°C
Storage temperature	T _{STG}	OX.COM.	- 65 to + 150	°C
Electrostatic discharge	V _{ESD}	HBM	5000	V
	WWW	MM	500	

Table 5-3. D.C. Electrical Characteristics

W.100Y.COM.TW $(T_A = -25 \degree C \text{ to + 70 } \degree C \text{ (Commercial)}, -40 \degree C \text{ to + 85 } \degree C \text{ (Industrial)}, V_{CC} = 1.8 \text{ V to 5.5 V)}$

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Parameter	OMIT	Symbol	Conditions	Min	Тур	Max	Unit
Input low voltage	COM.T	V _{IL}	SCL, SDA, A0, A1, A2	-//	M. 700,	0.3 V _{CC}	V
Input high voltage	COM	V_{IH}	WW.100Y.COM.TW	0.7 V _{CC}	MA+100	A COM.	V
Input leakage curre	nt N	I _{LI}	$V_{IN} = 0$ to V_{CC}	- 1	VW#1.10	10	μA
Output leakage current		I _{LO}	$V_O = 0$ to V_{CC}		WV E W.	10	10 μA 0.2 V
Output Low voltage		V _{OL}	$I_{OL} = 0.15 \text{ mA}, V_{CC} = 1.8 \text{ V}$	- W	WAIN	0.2	V
		OM.I.	$I_{OL} = 2.1 \text{ mA}, V_{CC} = 2.5 \text{ V}$	W		0.4	
Supply current	Write	I _{CC1}	V _{CC} = 5.5 V, 400 kHz	TT T	4M	3	mA
	V Jack	I _{CC2}	V _{CC} = 1.8 V, 100 kHz	M.T . N	-11	1007	
	Read	I _{CC3}	V _{CC} = 5.5 V, 400 kHz	W T W	- 1	0.4	
	W.10	I _{CC4}	V _{CC} = 1.8 V, 100 kHz	CONTITU	_ *	60	μA
Stand-by current	WWW.1	I _{CC5}	V _{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	COMIT	W _	5	μΑ
		I _{CC6}	V _{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	N.COM	TW -	WW.	



Table 5-3. D.C. Electrical Characteristics (Continued)

 $(T_A = -25 \,^{\circ}\text{C to} + 70 \,^{\circ}\text{C (Commercial)}, -40 \,^{\circ}\text{C to} + 85 \,^{\circ}\text{C (Industrial)}, V_{CC} = 1.8 \,\text{V to} 5.5 \,\text{V})$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input capacitance	C _{IN}	25 °C, 1MHz, V _{CC} = 5 V, V _{IN} = 0 V, A0, A1, A2, SCL and WP pin	M.COM.	IM -	10	pF
Input/Output capacitance	C _{I/O}	25 °C, 1MHz, $V_{CC} = 5$ V, $V_{I/O} = 0$ V, SDA pin	100X·CO	M.TW	10	

Table 5-4. A.C. Electrical Characteristics

 $(T_A = -25 \, ^{\circ}\text{C to} + 70 \, ^{\circ}\text{C (Commercial)}, -40 \, ^{\circ}\text{C to} + 85 \, ^{\circ}\text{C (Industrial)}, \, V_{CC} = 1.8 \, \text{V to} 5.5 \, \text{V})$

Parameter	Symbol	Conditions	V _{CC} = 1.8 (Standar			_{CC} = 2.5 to 5.5 V (Fast Mode)	
	WWW	Ton T. COM	Min	Max	Min	Max	
External clock frequency	F _{clk}	Witan COL	0	400	0.CO	1000	kHz
Clock High time	t _{HIGH}	M. To T.CO	0.6	41/11/1	0.5	WILL	μs
Clock Low time	t _{LOW}	MAN TOOX C	1.3	-1/1/1/	0.5	OM-TW	μs
Rising time	t _R	SDA, SCL	WI.TW	0.3	777.700Y	0.3	μs
Falling time	t _F	SDA, SCL	$CO_{\overline{M},TV}$	0.3	100	0.1	μs
Start condition hold time	t _{HD:STA}	MM = 100	0.6		0.25	Y.COM.T	μs
Start condition setup time	t _{SU:STA}	MA. W.10	0.6	_	0.25	OM.	μs
Data input hold time	t _{HD:DAT}	1.WA	O.O.	TAN _	0	no - CON	μs
Data input setup time	t _{SU:DAT}	-WW	0.1	V. I	0.1	700 X CO	μs
WP hold time	t _{HD:WP}	-	1.3	M. TW	1.3	M.Ing.	μs
WP setup time	t _{SU:WP}	- WW	0.6	OM: TW	0.6	W. IOT.C	μs
Stop condition setup time	t _{SU:STO}	W - W	0.6	COM-	0.25	1007	μs
Bus free time	t _{BUF}	Before new transmission	1.3	CO. W.TV	0.5	MMM.100	μs
Data output valid from clock low	t _{AA}	LTW -	0.1	0.9	0.05	0.55	μs
Noise spike width	t _{SP}	MITH	WALL TOWN!	50	TW_	50	ns
Write cycle time	t _{WR}	OM.TW		100 5	$V.L.\overline{\overline{L}}$	5	ms

NOTES:

- 1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
- When acting as a transmitter, the S524AD0XD1/D0XF1 must provide an internal minimum delay time to bridge the
 undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a
 start or stop condition.



DATA SHEET

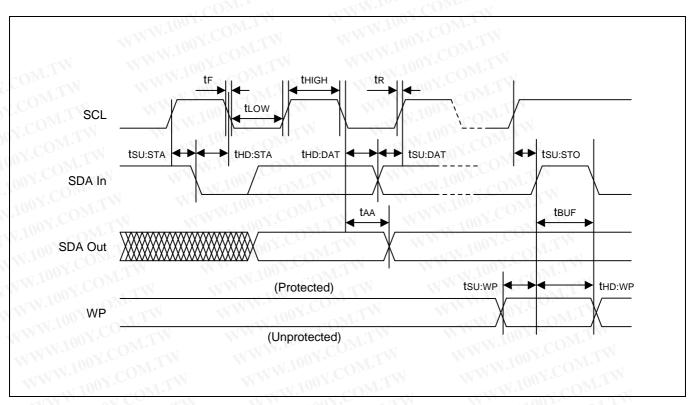


Figure 5-16. Timing Diagram for Bus Operations

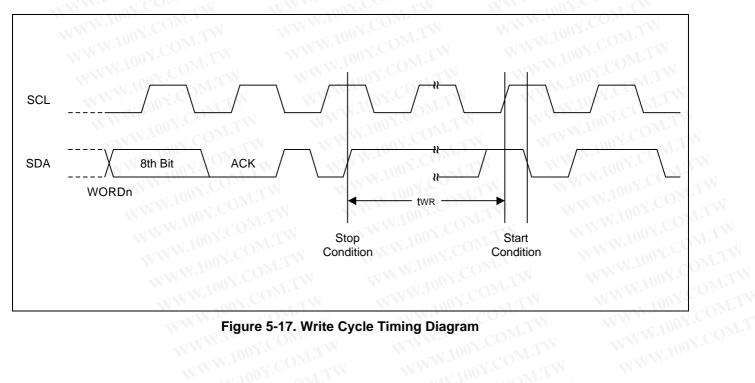


Figure 5-17. Write Cycle Timing Diagram WWW.100Y.CO WWW.100Y.COM.TW

WWW.100Y.COM.





S524AE0XH1

512K-bit Serial EEPROM for Low Power Preliminary

Data Sheet

OVERVIEW

The S524E0XH1 serial EEPROM has a 512K-bit (65,536 bytes) capacity, supporting the standard I²CTM-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 128 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524E0XH1 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 512K-bit (65,536 bytes) storage area
- 128-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 500,000 erase/write cycles
- 50 years data retention

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

Operating Characteristics

- Operating voltage
 - 1.8 V to 5.5 V
- Operating current
 - Maximum write current: < 3 mA at 5.5 V</p>
 - Maximum read current: < 400 μA at 5.5 V
 - Maximum stand-by current: < 5 μA at 5.5 V
- Operating temperature range
 - - 25°C to + 70°C (commercial)
 - - 40°C to + 85°C (industrial)
- Operating clock frequencies
 - 400 kHz at standard mode
 - 1 MHz at fast mode
- Electrostatic discharge (ESD)
 - 5,000 V (HBM)
 - 500 V (MM)

Packages

8-pin DIP, and SOP





W.100Y.COM.TW

WWW.100Y.COM.TW **Packaging Information**

Data Sheet

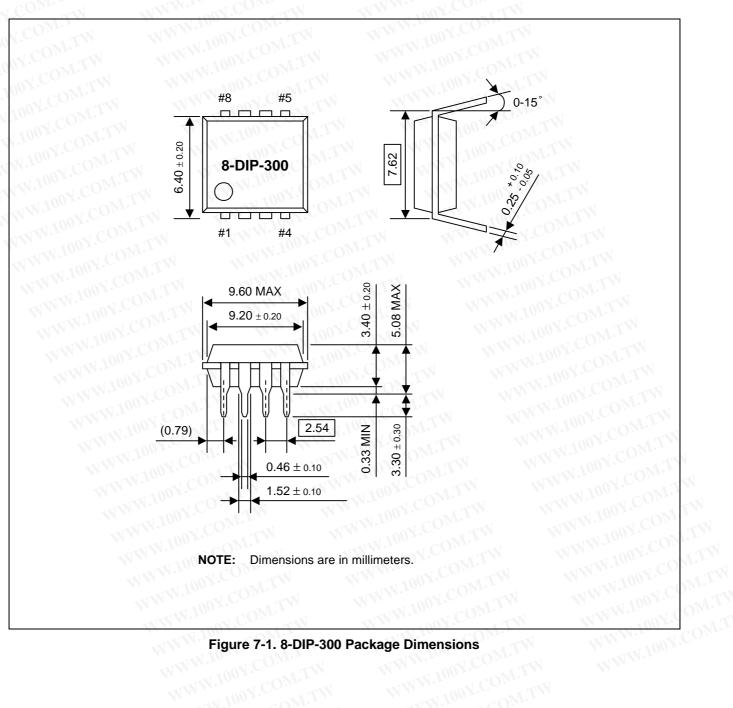


Figure 7-1. 8-DIP-300 Package Dimensions WWW.100Y.CO.

WWW.100Y.COM.TW



N.100Y.COM.TW

PACKAGING INFORMATION DATA SHEET

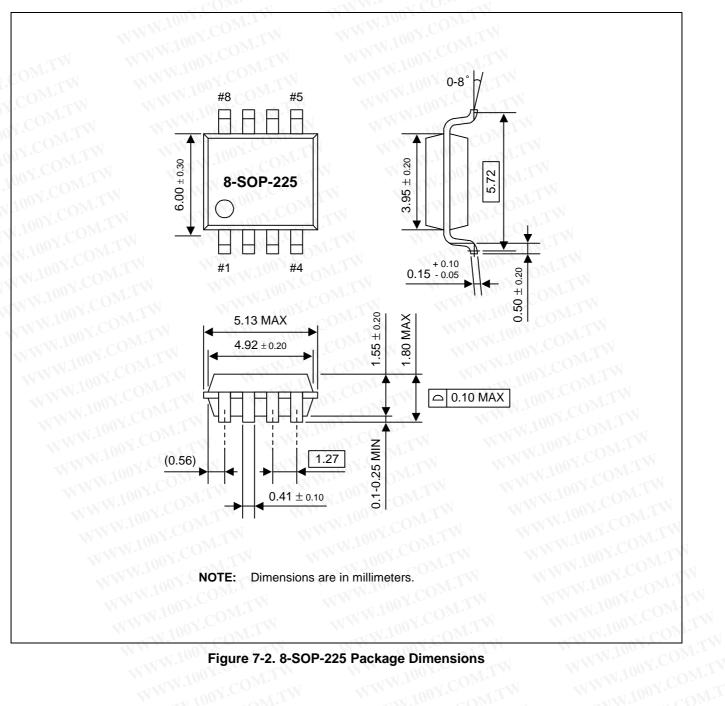
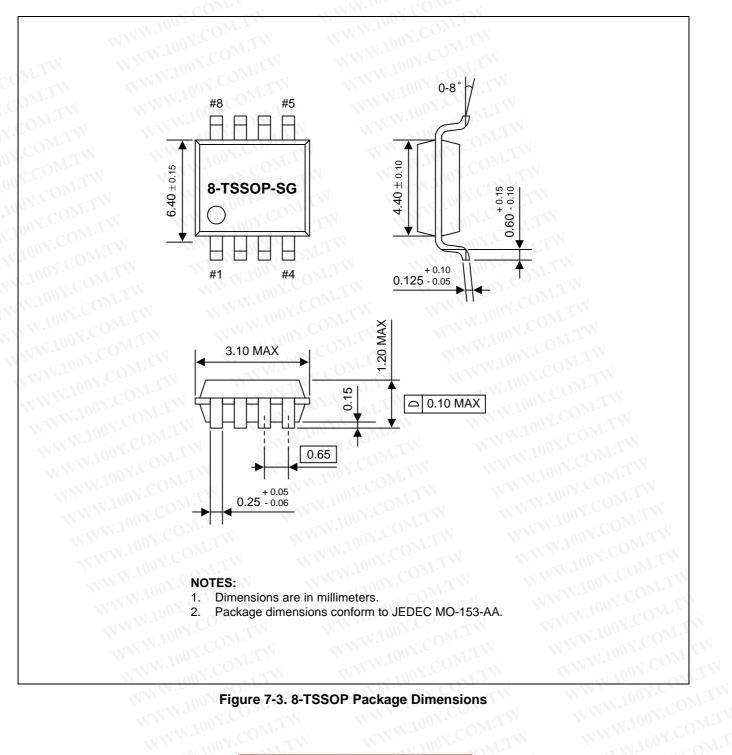


Figure 7-2. 8-SOP-225 Package Dimensions WWW.1003 WWW.100Y.COM.T

WWW.100Y.COM.TW 勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw 100Y.COM.TW



WWW.100Y.COM.T **DATA SHEET** PACKAGING INFORMATION



MMM:100X:CC

WWW.100Y.COM. 勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw

WWW.100X.

WWW.100Y.COM.T

OY.COM.TW





Interfacing S524A Series Serial EEPROM to the S3C8095/S3C72F5 Microcontroller

Application Note

OVERVIEW

This application note describes an interface between the S524A40X21 serial EEPROM and Samsung S3C8095/S3C72F5 microcontroller. The S524A series support the standard I²C™-bus serial data transmission protocol. S3C8095 is a 8-bit general purpose microcontroller, and S3C72F5 is a 4-bit general purpose microcontroller.

A typical circuit configuration between S3C8095/S3C72F5 and S524A40X21 is shown in Figure 8-1 and 8-2. As shown below, using the address inputs (A0, A1, A2), up to eight S524A40X21s can be connected to the same bus. The limited number of S524A series products (1 to 16 K-bit) which can be connected is shown in Table 8-1. The interface to the S3C8095/S3C72F5 uses there 2 I/O port lines. One of the lines is used to generate the serial clock (SCL), and the other is used as a bidirectional data line (SDA). It is recommended that an external pull-up resistor is configured to the SCL, SDL line. The S3C8095/S3C72F5 operate as a master which initiates a data transfer by generating the start condition on the bus, and a slave device S524A40X21 responds to the command issued by a master. The demonstration program which follows shows how the S524A40X21 serial EEPROM can be interfaced to the S3C8095/S3C72F5 microcontroller.

Table 8-1. S524A Series (1 to 16K-bit)

Device	EEPROM Size	Max Device Per Bus	Device Address Used
S524A40X10/40X11	1K-bit	8	A0, A1, A2
S524A40X20/40X21	2K-bit	8	A0, A1, A2
S524A40X40/40X41	4K-bit	1007. 4.17	A1, A2
S524A60X81	8K-bit	2	A2
S524A60X51	16K-bit	No. 100X.CA	WW. TIEDY.COM.

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw



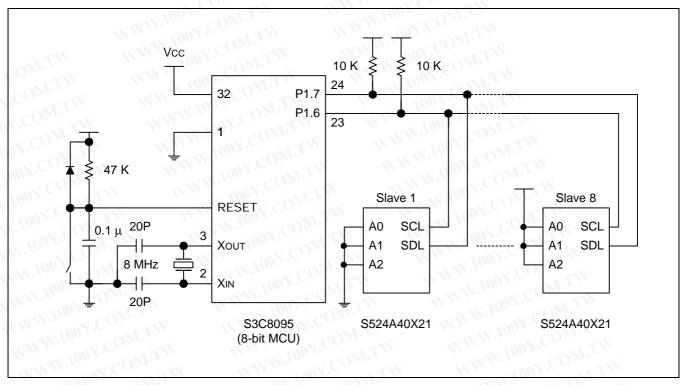


Figure 8-1. Typical Circuit Configuration 1

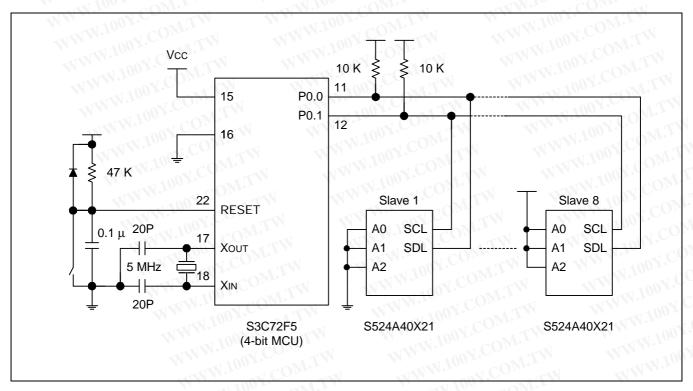


Figure 8-2. Typical Circuit Configuration 2



;This program demonstrates how the S524A40X21 serial EEPROM can be interfaced to the S3C8095 ;microcontroller. This software includes random address byte read and byte write operation. ;If you use the 8 MHz crystal in Figure 8-1, SCL frequency will be approximately 50 kHz. R14 = Word-address R15 = Write-data to the EEPROM ReadData = Read-data from the EEPROM Equation Table EQU ; SDA port (P1.7) SCL EQU 6H ; SCL port (P1.6) EQU 40H ReadData 勝 特 力 材 料 886-3-5753170 Random Address Byte Read 胜特力电子(上海) 86-21-34970699 ; Start \rightarrow Slave Addr.(A0) \rightarrow Word Addr. \rightarrow Start \rightarrow #A1h \rightarrow Data 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw Read1Byte: PUSH R0 PUSH R1 PUSH R2 CALL IICbus_Start IIC bus protocol start LD R0,#0A0h Slave address (A0) , τοντε (8bit) count ; Rotate left Data (= R0) ; Bit value check/Ω CLR R2 RD_TxStart LD R1.#8 ; Bit value check(0 or 1) ; Data "0" transfor RD_DataShift RLC R0 , υαιυe check(0 or ; Data "0" transfer C, RD_Data_1 JP RD_Data_0 AND P1,#0FFh-(01<<SDA) CALL IIC_Clock_1Bit ; SDA (P1.7) = Input Mode ; Acknowledge olar! RD_Count8bit DJNZ R1,RD_DataShift WWW.100Y.COM.TV P1CONH,#00111111B AND OR P1,#01<<SCL NOP NOP NOP ; Ack in? P1.#01<<SDA TM JΡ NZ,CommuniFail AND P1,#0FFh-(01<<SCL) ; SDA (P1.7) = Output Mode P1CONH,#01000000B OR (next page continued)



8-3

			241 100	OWI-	
		-ow.TW	MAN TOOX.	CONTA	
	CP JR CP	R2,#02 UGE,RxData	MMM.100	TxCount = R2	
	JR	R2,#01 UGE,ReStart			
Y. M. TW	LD	R0,R14	WW.1	TxCount++	
	INC	R0,K14 R2		TxCount++	
	JR	RD_TxStart	WW	TOOX CONTAIN	
; ReStart	OR	P1,#11000000B	MM	P1.7/P1.6 ← High ((SDA.SCL)
	NOP	WWW.TI 100Y.COM.TY	M Mil	W.100Y.COM.T	, ,
	NOP				
	NOP AND	P1,#0FFh-(01< <sda)< td=""><td>W W</td><td>IIC Start Condition</td><td></td></sda)<>	W W	IIC Start Condition	
	NOP	11,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	TW V	No Start Condition	
	NOP				
	NOP NOP				
	AND	P1,#0FFh-(01< <scl)< td=""><td></td><td></td><td></td></scl)<>			
N. W. 100X.					
	LD	R0,#0A1h	M.TW ;	Slave Address for r	reading
	INC JR	R2 RD_TxStart	.COM .	TxCount++	
; WWW.too	A'CON	THE TROUBLE			
RxData	AND NOP	P1CONH,#00111111B	ON.COM.TW	SDA (P1.7) = Input	Mode
MM	LD	R1,#8		- WW.	
RotateLoop	OR TM	P1,#01< <scl P1,#01<<sda< td=""><td>100Y.CO.M.T</td><td>SCL ← High Data value check</td><td></td></sda<></scl 	100Y.CO.M.T	SCL ← High Data value check	
	JR	NZ,SetCF	100 Y. COMP.	Data value check	
	RCF	COM. TW WWW			
-17	JR	DataRotate			
, SetCF	SCF				
DataRotate	RLC	R0			
	AND	P1,#0FFh-(01< <scl)< td=""><td>W.1007.</td><td>SCL ← Low</td><td>M.1001. COM.11</td></scl)<>	W.1007.	SCL ← Low	M.1001. COM.11
	DJNZ LD	R1,RotateLoop ReadData,R0	VW 100Y.	End of 1byte(8bit)	M.100Y.COM.T.
	WWW	rredabata, rro			
	OR	P1CONH,#01000000B	WW 100X	SDA (P1.7) = Outp	
	OR	P1,#01< <sda< td=""><td>MMM</td><td>SDA ← High (ACK: finished</td><td>=High): communication</td></sda<>	MMM	SDA ← High (ACK: finished	=High): communication
	NOP		WWW.L.	mistieu	
	NOP	MM:Ing COW.		ON.COM.	WWW.100Y.CO
	OR	P1,#01< <scl< td=""><td>WWW;1</td><td>SCL ← High (9th cl</td><td>lock)</td></scl<>	WWW;1	SCL ← High (9th cl	lock)
	NOP NOP				lock)
	A A ! D	D4 #0551 (04 001)	J WWY	VION COM.	
	AND NOP	P1,#0FFh-(01< <scl)< td=""><td>ov - TVV</td><td>$SCL \leftarrow Low$</td><td></td></scl)<>	ov - TVV	$SCL \leftarrow Low$	
;	(next p	age continued)		WW.100X.COM.T WW.100X.COM.T WWW.100X.COM	
				MM.100X.COW	

WWW.1007.C

WWW.100Y.COM. IICbus_Stop GenlicStop CALL RO JOY CONTIN POP POP POP RET ; Data "1" trasfer RD Data 1 OR P1.#01<<SDA IIC_Clock_1Bit CALL JΡ RD Count8bit 勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 Byte Write Operation 胜特力电子(深圳) 86-755-83298787 ; Start \rightarrow Slave Addr.(A0) \rightarrow Word addr. \rightarrow Data Http://www.100y.com.tw WWW.100Y.COM.TW IICbus_Start Write1Byte: PUSH R0 PUSH R1 WWW.100Y.COM.TW PUSH R2 CALL IIC bus protocol start Slave address LD R0,#0A0h CLR R2 ; 1 Byte (8bit) count WR_TxStart LD R1,#8 WR_DataShift RLC P1,#0FFh-(01<<SDA) R0 JR Data "0" transfer WR_Data_0 AND 1byte check CALL WR_Count8bit DJNZ R1,WR_DataShift SDA (P1.7) = Input Mode
Acknowledge clast AND P1CONH.#00111111B WWW.100Y.COM.TW OR P1,#01<<SCL WWW.100Y.CON NOP WWW.100Y.COM.TW NOP ; Ack in ? NOP P1,#01<<SDA TM NZ,CommuniFail JR ; SDA(P1.7) = Output Mode AND P1,#0FFh-(01<<SCL) WWW.100Y.COM.TW OR P1CONH,#01000000B WWW.100Y.COM.TW CP R2,#2 JR UGE,TxStop CP R2,#1 JR UGE, Write Data LD R0,R14 Word Address ; TxCount++ **INC** R2 WWW.100Y.CON WR_TxStart JR N 100Y.COM.TW (next page continued)

WWW.100Y.COM.TW **SERIAL EEPROM APPLICATION NOTE**

OLIVIAL ELI IVO				ALL ELOAMON NOTE
		COM.TW	WW.100Y.	COM.TW
WriteData	LD INC	R0,R15 R2	MM.M.100.	Data to be written to the EEPROM TxCount++
WTI	JR	WR_TxStart		
, WR_Data_1	OR CALL	P1,#01< <sda IIC_Clock_1Bit</sda 	WWW.i	Data "1" transfer
V.COM.TW	JR	WR_Count8bit		
, CommuniFail	AND NOP NOP	P1,#0FFh-(01< <scl)< td=""><td></td><td></td></scl)<>		
	OR JP	P1CONH,#01000000B GenlicStop	WW WI	SDA(P1.7) = Output Mode
TxStop	JP	GenlicStop		
IICbus_Start	NOP ; NOP ;		P1.7/P1.6 ← High (SDA, SCL)	
	NOP NOP			
	AND NOP	P1,#0FFh-(01< <sda)< td=""><td></td><td></td></sda)<>		
	NOP NOP			
	NOP NOP			
	AND RET	P1,#0FFh-(01< <scl)< td=""><td></td><td></td></scl)<>		
IIC_Clock_1Bit	OR NOP NOP	P1,#01< <scl;< td=""><td>M.100X.COM</td><td>Clock Generation.</td></scl;<>	M.100X.COM	Clock Generation.
	NOP			
	AND NOP	P1,#0FFh-(01< <scl)< td=""><td></td><td>M.TW WWW.IOOY.COM.T</td></scl)<>		M.TW WWW.IOOY.COM.T
	RET	D1 #0FFb (01 c-SDA)		勝 特 力 材 料 886-3-5753170
IICbus_Stop	AND NOP			■ 胜特力电子(深圳) 86-755-83298787
	NOP NOP	P1 #01		Http://www.100y.com.tw
	OR NOP NOP	P1,#01<<5CL		
	NOP NOP	P1 #01< <sda< td=""><td></td><td>; SDA ← High (Stop condition)</td></sda<>		; SDA ← High (Stop condition)
	NOP OR RET	P1,#01< <sda< td=""><td></td><td>; SDA ← High (Stop condition)</td></sda<>		; SDA ← High (Stop condition)
				W.100X.COM.TW WW.100X.COM.TW WWW.100X.COM.TW

WWW.100Y.COM.TW

WWW.100X.C

W.100Y.COM.TW

; This program demonstrates how the S524A40X21 serial EEPROM can be interfaced to the SAMSUNG S3C72F5 microcontroller. This software includes random address byte read and byte write operation. ; If you use the 5 MHz crystal oscillator, SCL frequency will be approximately 50 kHz Equation Table P0.0 SDA_PORT EQU SCL_PORT P0.1 EQU ReadAddr EQU 20H 勝 特 力 材 料 886-3-5753170 ReadData EQU 22H 胜特力电子(上海) 86-21-34970699 WriteAddr 30H EQU. WriteData EQU 32H 胜特力电子(深圳) 86-755-83298787 PMG1_BUF EQU 40H Http://www. 100y. com. tw Random Address Byte Read ; Start \rightarrow Slave Addr.(A0) \rightarrow Word Addr. \rightarrow Start \rightarrow #A1h \rightarrow Data IIC Interface start Read1Byte: CALL IICbus Start Y,#0H LD EA,#0A0h Slave Address (A0) LD ; 1Byte (8bit) RD_TxStart LD Z.#7 RD DataShift ADC EA,EA BTST C JP RD_Data_0 ; Data "1" transfer SDA_PORT **BITS** RD_Data_1 CALL IIC_Clock_1Bit JΡ RD_Count8bit ; Data "0" transfer SDA PORT RD Data 0 BITR WWW.100Y.CON IIC_Clock_1Bit CALL RD Count8bi DECS Z RD DataShift ; SDA Port Input Mode JP CALL SdaInMode WWW.100Y.COM.TW **BITS** SCL_PORT NOP NOP NOP (next page continued)

Http://www. 100y. com. tw

BTSF	SDA_PORT	; ACK Check
JR	CommuniFail	WP WOOY.CO TY
BITR	SCL PORT	
CALL	SdaOutMode	
CPSE	Y,#2H	; TxCount = Y
ID	NovtP1	· COM.

; TxCount = Y RxData CPSE\ WWW.100Y.COM.TW

JP JP

NextR1 **CPSE** Y,#1H

JΡ NextR2 JP

WWW.100Y.COM.TW EA,ReadAddr Y RD_TxStart LD Pointed Address to Read W.100Y.COM.TW WWW.100Y.COM.T

INCS

JΡ

ReStart WWW.I

RxData

W.100Y.COM.TW SDA HIGH WWW.100Y.COM.TW SCL HIGH SDA_PORT BITS WWW.100Y.COM.TW **BITS** SCL_PORT

NOP

NOP NOP

NOP NOP

BITR

W.100Y.COM.TW Start Condition WWW.100Y.COM.TW WWW.100Y.COM.TW SDA_PORT WWW.100Y.COM.TW

NOP

NOP NOP

NOP NOP

SCL PORT **BITR**

NOP

WW.100Y.COM.TW WWW.100Y.COM.TW WWW.100Y.COM.TW ; Slave Address for Reading (A1) ; Tx Count ++ ار Jave Addres ; Tx Count ++ WWW.100Y.COM.TW LD EA,#0A1h

; TxCount++

INCS

JP RD_TxStart

CALL SdalnMode

NOP

WWW.100Y.COM.TW LD EA,#00H

WWW.100Y.COM.TW ; 1Byte Count(8bit) LD Z,#7 WWW.100Y.C WWW.100Y.COM.TW

RotateLoop **BITS** SCL_PORT

NOP

NOP

NOP

SDA_PORT **BTSF**

JP SetCF

WWW.100Y.COM.TW OY.COM.TW DataRotate ; Data "0" **RCF** WW.100Y. JΡ

LLDOY.COM.TW

WWW.100Y.COM.

W.100Y.COM.TW :COM.TW WWW.100Y.COM.TW (next page continued) SetCF WWW.100Y.COM.TW WW.100Y.COM.TW

WWW.100X.

W 100Y.COM.TW

WWW.100Y.COM.TV WWW.100Y EA,EA **DataRotate ADC BITR** SCL_PORT NOP NOP WWW.100Y.COM.TW NOP DECS Z ; Save Read Data JΡ RotateLoop SdaOutMode LD WWW.100Y.C W.100Y.COM.TW **CALL** WWW.100Y.COM. **BITS** SDA_PORT WWW.100Y.COM.TW SCL_PORT NOP .100Y.COM.TW NOP **BITS** 勝 特 力 材 料 886-3-5753170 NOP NOP 胜特力电子(上海) 86-21-34970699 **BITR** SCL PORT IICbus_Stop 胜特力电子(深圳) 86-755-83298787 NOP Http://www. 100y. com. tw GenlicStop CALL **RET** ****** Byte Write Operation ; Start \rightarrow Slave Addr.(A0) \rightarrow Word addr. \rightarrow Data WWW.100Y.CO .100Y.COM.TW WWW.100Y.COM.TW ; Slave Address (A0) Write1Byte: CALL IICbus_Start WWW.100Y.COM.TW LD Y.#0H ; 1Byte (8bit) count EA,#Slave_WR WWW.100Y.COM.TW Z,#7 WR TxStart LD WWW.100Y.COM.TW WWW.100Y.COM:T EA,EA Data "1" transfer WR DataShift ADC WWW.100Y.COM.TW **BTST** C WI.MO: JP WR_Data_0 WR_Data_1 BITS SDA_PORT WWW.100Y.C WWW.100Y.COM.TW CALL IIC_Clock_1Bit **BITR** SDA_PORT JP WR_Count8bit MMM.1007 Data "0" transfer WR_Data_0 **BITR** SDA PORT CALL IIC_Clock_1Bit ; 1byte check WR Count8bit DECS Ζ WWW.100Y.COM.TW WWW.100X WR DataShift JP **CALL** SdalnMode SCL_PORT BITS WW.100Y.COM.TW (next page continued) N 100Y.COM.TW 100Y.COM.TW

SERIAL EEPROM APPLICATION NOTE

WWW.100Y.COM.T W.100Y.COM.TW WWW.100Y WWW.100Y.COM.TW NOP NOP NOP ; ACK Check SDA_PORT **BTSF** WWW.100Y WWW.100Y.COM. JΡ CommuniFail BITR SCL_PORT CALL SdaOutMode CPSE Y,#2H JΡ NextW1 JP **TxStop** NextW1 **CPSE** Y,#1H N.100Y.COM.TW JΡ NextW2 JΡ WriteData NextW2 LD ; Address to be written EA,WriteAddr **INCS** Υ JΡ WR_TxStart Data to be written WWW.100Y.COM.TW WriteData LD EA,WriteData INCS Y WW.100Y.COW.TW JP WR_TxStart JP GenlicStop **TxStop** WWW.100Y.CON.TW IICbus_Start SDASCL_OutMode CALL NOP WWW.100Y.COM.TW WWW.100Y.COM.TW NOP ; Start Condition NOP WWW.100Y.COM.TW NOP NOP SDA_PORT **BITR** WWW.100Y.COM. NOP NOP WWW.100Y.COM.TW NOP NOP WWW.100Y.COM.TW NOP **BITR** SCL_PORT 勝 特 力 材 料 886-3-5753170 RET SDA_PORT IICbus_Stop **BITR** 胜特力电子(上海) 86-21-34970699 NOP 胜特力电子(深圳) 86-755-83298787 NOP WW.100Y.COM.TW Http://www. 100y. com. tw SCL_PORT **BITS** WWW.100Y.COM.TW NOP NOP 100Y.COM.TW NOP NOP SDA_PORT NOP .100Y.COM.TW Stop Condition **BITS** WWW.100Y.COM.TW (next page continued) RET WW.100Y.COM.TW W 100Y.COM.TW

WWW.100Y.COM.TW 100Y.COM.TW APPLICATION NOTE SERIAL EEPROM

WWW.100Y WWW.100Y.COM.T SCL_PORT IIC_Clock_1Bit BITS NOP 勝 特 力 材 料 886-3-5753170 NOP 胜特力电子(上海) 86-21-34970699 NOP LOOY.COM.TW W.100Y.COM.TW 胜特力电子(深圳) 86-755-83298787 SCL_PORT **BITR** RET NY.COM.TW Http://www.100y.com.tw SdalnMode WWW.100 WWW.100Y.COM. EA,PMG1_BUF PUSH EAVWW.1007.COM WWW.100Y.COM.TW LD AND A,#1110B Y.COM.TW PMG1,EA LD WWW.100Y.COM.TW **SMB** ; SDA INPUT LD WWW.100Y.COM.TW WWW.100Y.COM.TW WWW.100Y **SMB** WWW.100Y.COM POP EΑ RET .100Y.COM.TW SdaOutMode **PUSH** EΑ WWW.1003 **SMB** 0 WWW.100Y.COM.TW . "πυυυ1Β PMG1_BUF,EA 15 LD 100Y.COM.TW WWW.100Y.COM.TW OR LD WWW.100Y.COM.TW SDA OUTPUT **SMB** WWW.100Y.COM.TW LD PMG1.EA WWW. **SMB** POP EΑ RET SCL_PORT CommuniFail **BITR** NOP NOP CALL SdaOutMode JP GenlicStop NWW.100Y.COM.TW WWW.100Y.COM.TW SDASCL OutMode ; N-ch open drain (P0.0) **BITS EMB** WWW.100Y.COM.TW SMB 15 ; SCL,SDA OUTPUT ; Pull-up enable LD EA,#0000001B WWW.100Y.COM.TW LD PNE1,EA EA,#0000011B LD پیدری SDA OU⊺ ; Pull-up enable LD PMG1,EA LD PUMOD1,EA WWW.100Y.COM **SMB** LD PMG1 BUF.EA **BITS** SDA PORT SCL_PORT NOP WWW.100Y.COM.TW BITS



RET

WWW.100Y.COM.TW

WWW.100Y.

N 100Y.COM.TW

WWW.100X.COM.

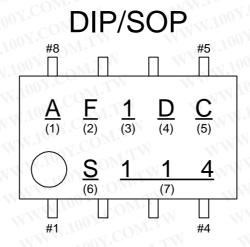
8-11

TU 100Y.COM.TW



Marking Information

Data Sheet



- (1) Operating Voltage
 - A = 1.8 V to 5.5 V
 - L = 2.0 V to 5.5 V
 - C = 2.5 V to 5.5 V
- (2) EEPROM Density
 - 1 = 1K-bit
 - 2 = 2K-bit
 - 4 = 4K-bit
 - 8 = 8K-bit
 - 5 = 16K-bit 9 = 32K-bit
 - B = 64K-bit
 - D = 128K-bit
 - F = 256K-bit
 - H = 256K-DitH = 512K-bit

- (3) Write Protection
 - 0 = Hardware and software
 - 1 = Hardware Only
- (4) Package Type
 - D = DIP type
 - S = SOP type
 - R = TSSOP type
- (5) Temperature Range
 - $C = -25^{\circ} C$ to $70^{\circ} C$
 - $I = -40^{\circ} \text{ C to } 85^{\circ} \text{ C}$
- (6) Work Week Code
- (7) Assembly Site Code

TSSOF





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Ordering Information

Data Sheet

(6)

- WWW.100Y.COM.TW (1) Series Name 24: I²C interface
 - (2) Operation Voltage C: 2.5 V - 5.5 V L: 2.0 V - 5.5 V A: 1.8 V - 5.5 V
 - (3) Samsung's Internal Management Data
 - (4) ROM Size 1 = 1K-bit2 = 2K-bit4 = 4K-bit8 = 8K-bit5 = 16K-bit9 = 32K-bitB = 64K-bitD = 128K-bitF = 256K-bitH = 512K-bit

- (5) Write Protection 0 = Hardware and software 1 = Hardware only
- (6) Package Type D = DIPR = TSSOPS = SOP
- (7) Temperature Range $C = -25^{\circ} C$ to $70^{\circ} C$ $I = -40^{\circ} C \text{ to } 85^{\circ} C$
- (8) Package Type B = TubeT = Tape & Reel
- (9) Customer Type 0 = None

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