DATA SHEET

S524A Series (I^2C-Bus) Serial EEPROM Revision 1

SAMSUNG ELECTRONICS

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Serial EEPROM

DATA SHEET

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S524A Series (I^2C Bus) Serial EEPROM
Data Sheet, Revision 1
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Serial EEPROM Selection Guide

S524A40X10/40X20/40X40

S524A40X11/40X21/40X41/60X81/60X51

S524AB0X91/B0XB1

S524AD0XD1/D0XF1

S524AE0XH1

Packaging Information

Application Note

Marking Information

Ordering Information

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Serial EEPROM Selection Guide

Data Sheet

SERIAL EEPROM SELECTION GUIDE

Product	Density (Organization)	Page Buffer	Write Time (Max)	Write Protect	Endurance	Operating Voltage	Package
S524A40X11	1K-bit (128 × 8)	16 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A40X10	1K-bit (128 × 8)	16 bytes	5 ms	H/W, S/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A40X21	2K-bit (256 × 8)	16 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A40X20	2K-bit (256 × 8)	16 bytes	5 ms	H/W, S/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A40X41	4K-bit (512 × 8)	16 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A40X40	4K-bit (512 × 8)	16 bytes	5 ms	H/W, S/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A60X81	8K-bit (1024 × 8)	16 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524A60X51	16K-bit (2048 × 8)	16 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524AB0X91	32K-bit (4096 × 8)	32 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524AB0XB1	64K-bit (8192 × 8)	32 bytes	5 ms	H/W	1M	1.8V–5.5V	8DIP/SOP/TSSOP
S524AD0XD1	128K-bit (16384 × 8)	64 bytes	5 ms	H/W	500K	1.8V–5.5V	8DIP/TSSOP
S524AD0XF1	256K-bit (32768 × 8)	64 bytes	5 ms	H/W	500K	1.8V–5.5V	8DIP/TSSOP

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S524A40X10/40X20/40X40

1K/2K/4K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524A40X10/40X20/40X40 serial EEPROM has a 1,024/2,048/4,096-bit (128/256/512-byte) capacity, supporting the standard I²C™-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). Important features are a hardware-based write protection circuit for the entire memory area and software-based write protection logic for the lower 128 bytes. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. The software-based method is one-time programmable and permanent. Using one-page write mode, you can load up to 16 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524A40X10/40X20/40X40 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 1K/2K/4K-bit (128/256/512-byte) storage area
- 16-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- Software-based write protection for the lower 128-byte EEPROM
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

Operating Characteristics

- Operating voltage
  - 1.8 V to 5.5 V
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 200 µA at 5.5 V
  - Maximum stand-by current: < 5 µA at 5.5 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 100 kHz at standard mode
  - 400 kHz at fast mode
- Electrostatic discharge (ESD)
  - 5,000 V (HBM)
  - 500 V (MM)

Packages

- 8-pin DIP, SOP, and TSSOP

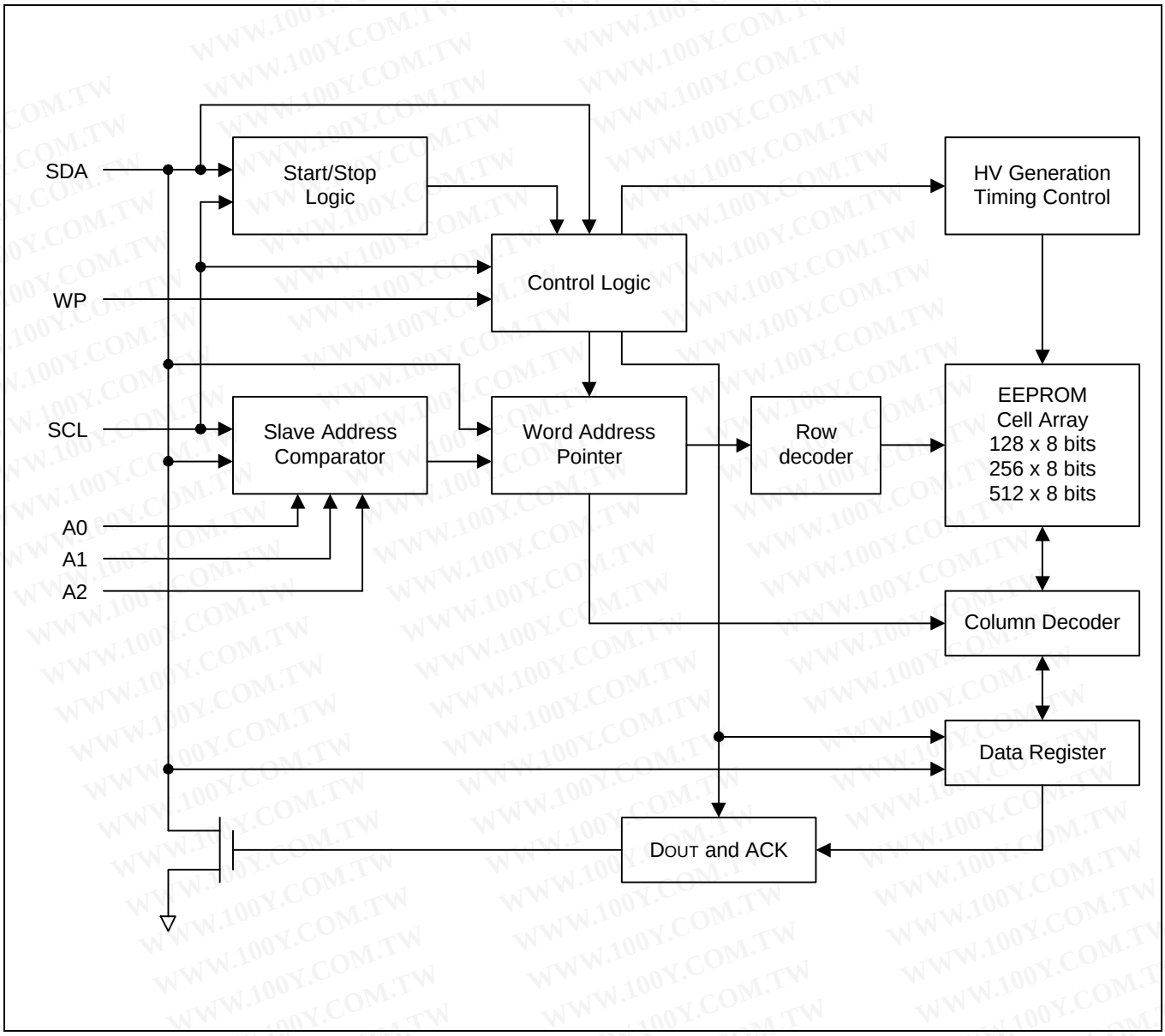
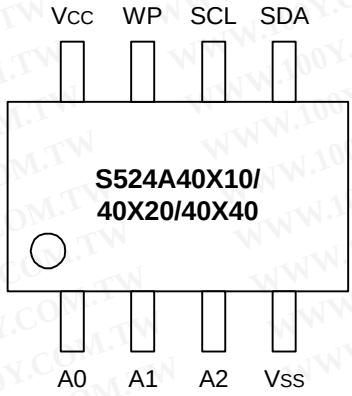


Figure 2-1. S524A40X10/40X20/40X40 Block Diagram



NOTE: The S524A40X10/40X20/40X40 is available in 8-pin DIP, SOP, and TSSOP package.

Figure 2-2. Pin Assignment Diagram

Table 2-1. S524A40X10/40X20/40X40 Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS}.	1
V_{SS}	–	Ground pin.	–
SDA	I/O	Bi-directional data pin for the I^2C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V_{CC}. Typical values for this pull-up resistor are 4.7 kΩ (100 kHz) and 1 kΩ (400 kHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC}, the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS}, the write function is enabled. This pin is internally pulled down to V_{SS}.	1
V_{CC}	–	Single power supply.	–

NOTE: See the following page for diagrams of pin circuit types 1, 2, and 3.

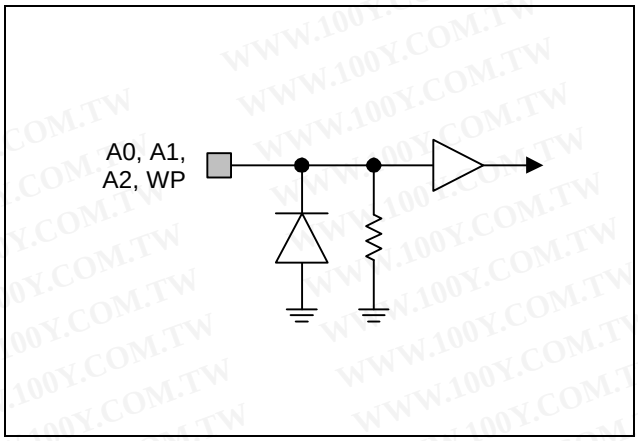


Figure 2-3. Pin Circuit Type 1

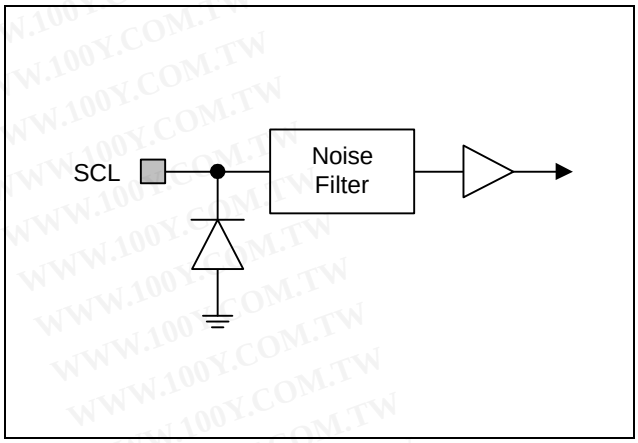


Figure 2-4. Pin Circuit Type 2

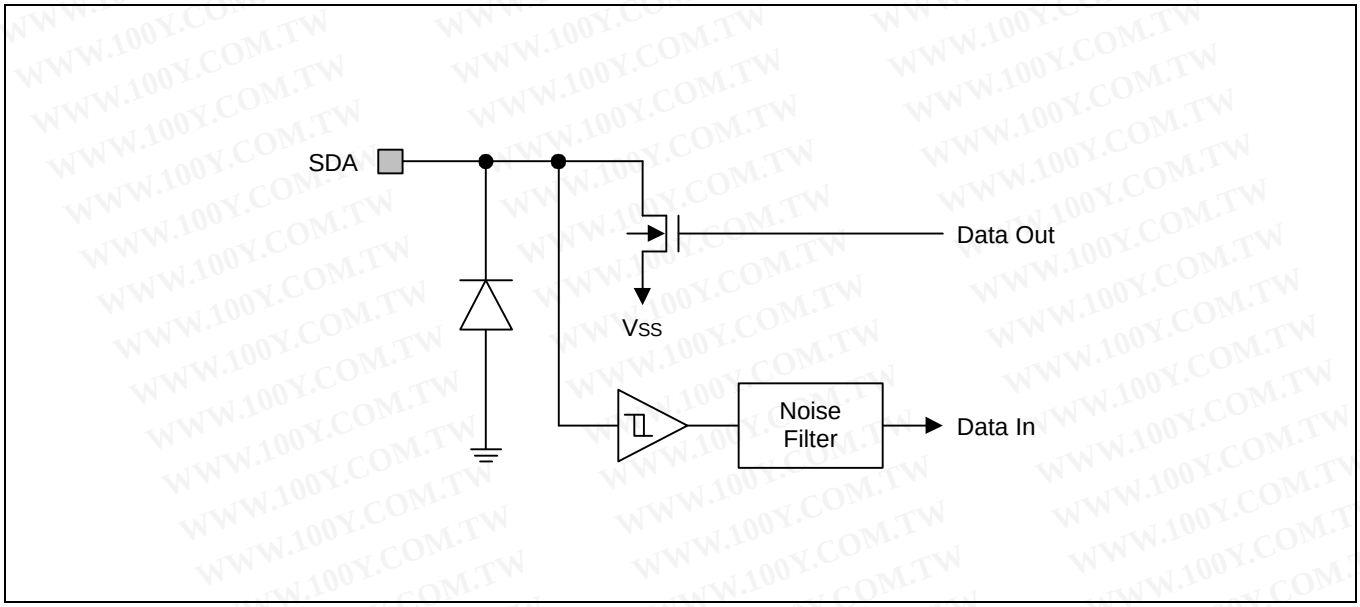


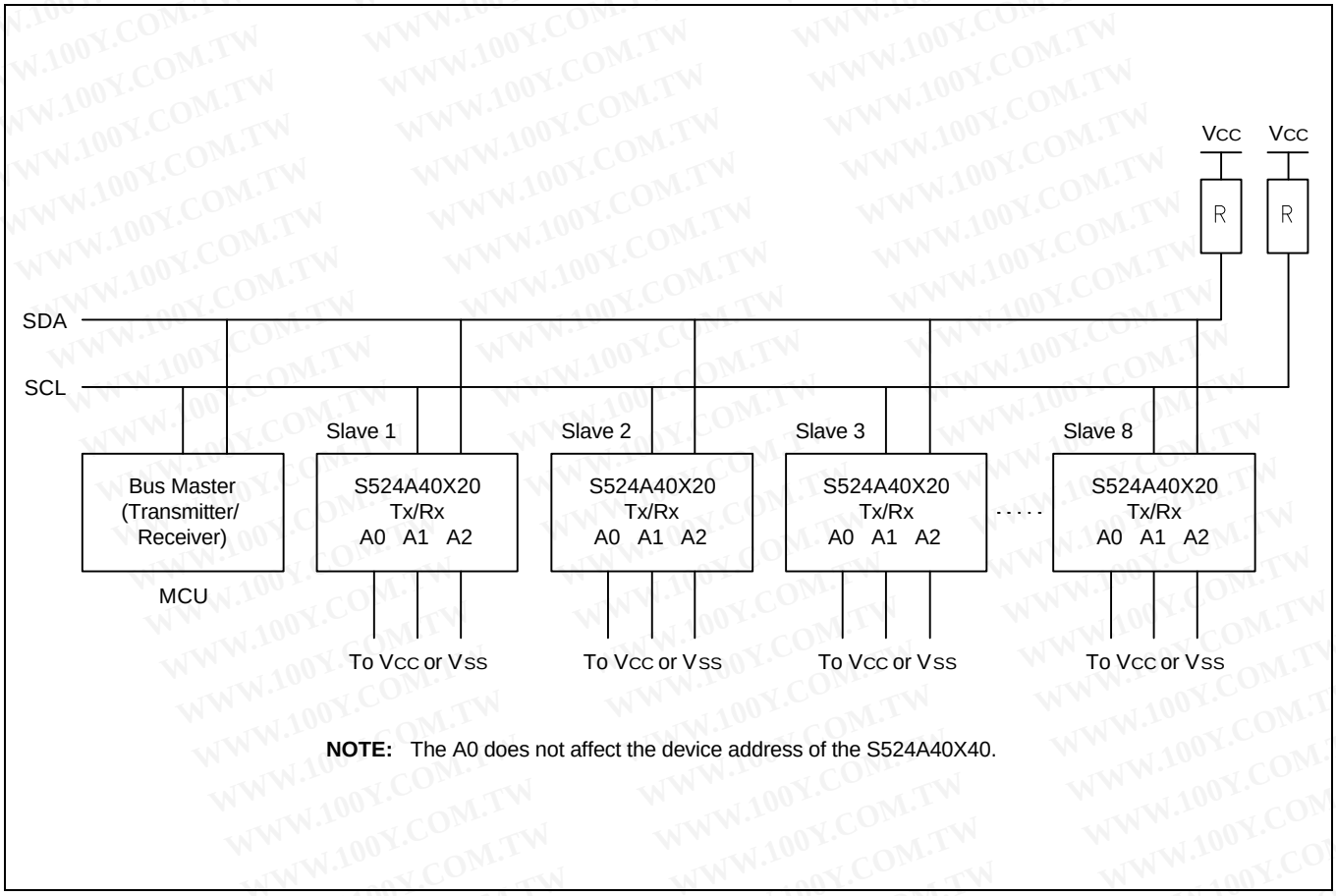
Figure 2-5. Pin Circuit Type 3

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524A40X10/40X20/40X40 supports the I²C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as the “transmitter” and any device that gets data from the bus is the “receiver.” The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0,A1 and A2 input pins, up to eight S524A40X10/40X20 (four for S524A40X40) devices can be connected to the same I²C-bus as slaves (see Figure 2-6). Both the master and slaves can operate as transmitter or receiver, but the master device determines which bus operating mode would be active.



NOTE: The A0 does not affect the device address of the S524A40X40.

Figure 2-6. Typical Configuration (16 Kbits of Memory on the I²C-Bus)

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

— A new data transfer can be initiated only when the bus is currently not busy.

— MSB is always transferred first in transmitting data.

— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- Start condition: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition (see Figure 2-7).

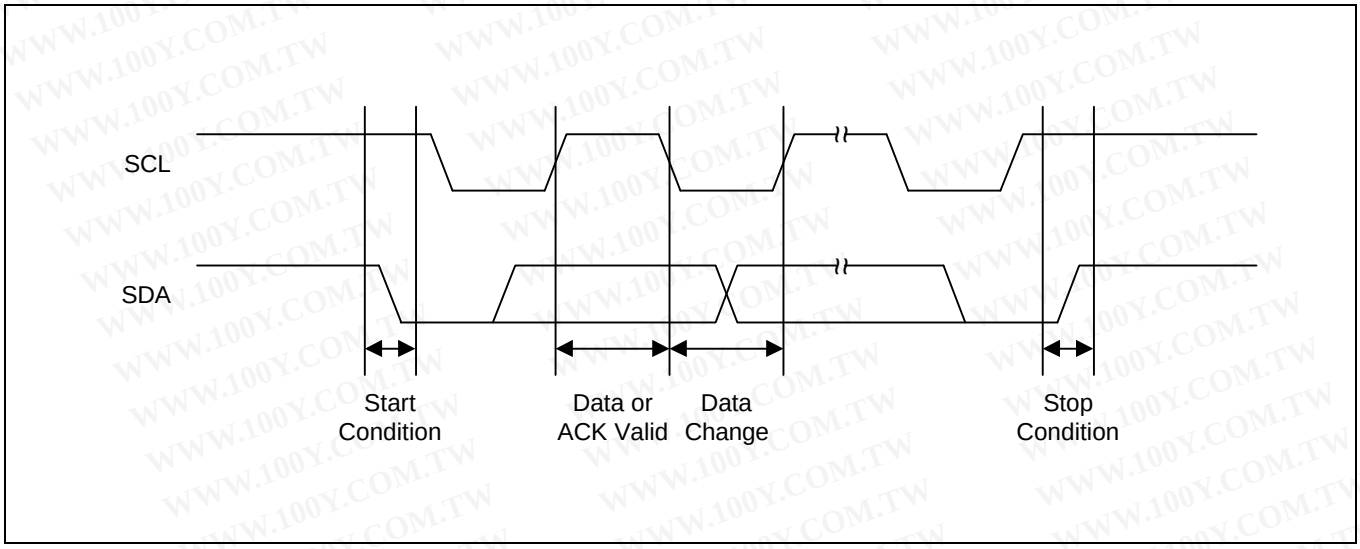


Figure 2-7. Data Transmission Sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.
- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 2-8). But the slave does not send an ACK if an internal write cycle is still in progress.

  In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

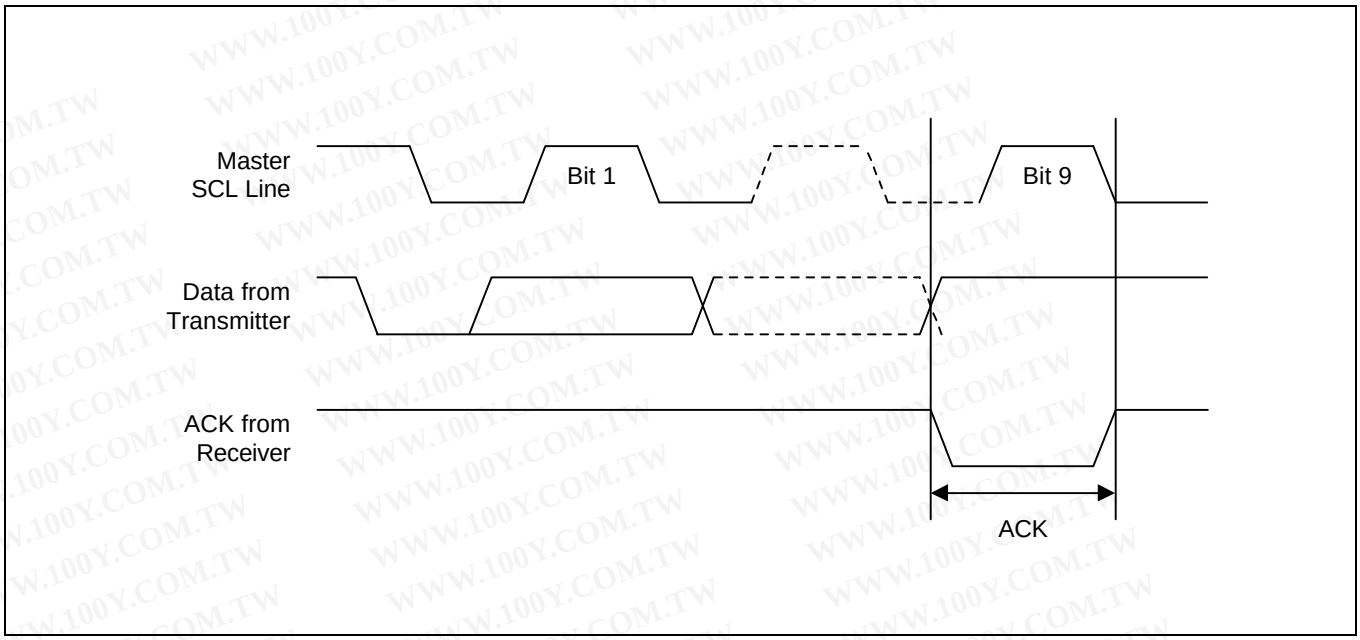


Figure 2-8. Acknowledge Response From Receiver

- Slave Address: After the master initiates a Start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the “device identifier”. The identifier for the S524A40X10/40X20/40X40 is “1010B”. The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1 and A2 pins. Using this addressing scheme, you can cascade up to eight S524A40X10/40X20 or four S524A40X40 on the bus (see Table 2-2 below). The b1 for S524A40X40 is used by the master to select which of the blocks of internal memory (1 block = 256 words) are to be accessed. The bit is in effect the most significant bit of the word address.
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is “1”, a read operation is executed. If it is “0”, a write operation is executed.

Table 2-2. Slave Device Addressing

Function	Device Identifier				Device Address			R/W Bit
	b7	b6	b5	b4	b3	b2	b1(note)	b0
Read	1	0	1	0	A2	A1	A0	1
Write	1	0	1	0	A2	A1	A0	0
Write-protect	0	1	1	0	A2	A1	A0	0

NOTE: The b1 for S524A40X40 corresponds to the MSB of the memory array address word.

BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the S524A40X10/40X20/40X40 slave device (see Figure 2-9).

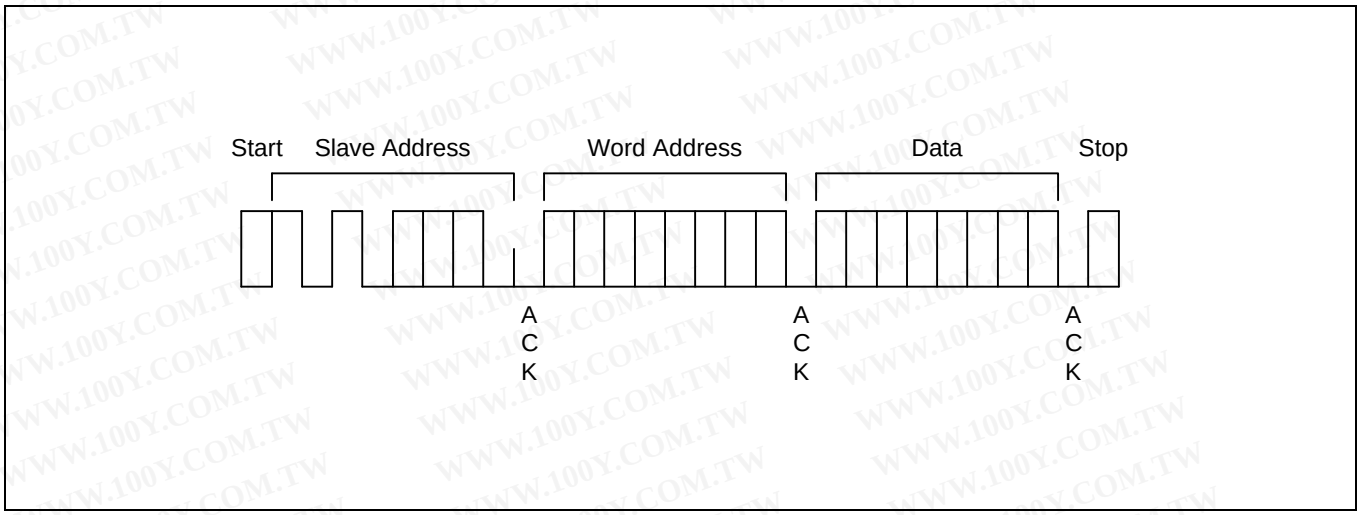


Figure 2-9. Byte Write Operation

Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to “0” onto the bus. Then the addressed S524A40X10/40X20/40X40 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the S524A40X10/40X20/40X40.

When the S524A40X10/40X20/40X40 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the S524A40X10/40X20/40X40 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the S524A40X10/40X20/40X40 begins the internal write cycle.

While the internal write cycle is in progress, all S524A40X10/40X20/40X40 inputs are disabled and the S524A40X10/40X20/40X40 does not respond to additional requests from the master.

PAGE WRITE OPERATION

The S524A40X10/40X20/40X40 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The S524A40X10/40X20/40X40 responds with an ACK each time it receives a complete byte of data (see Figure 2-10).

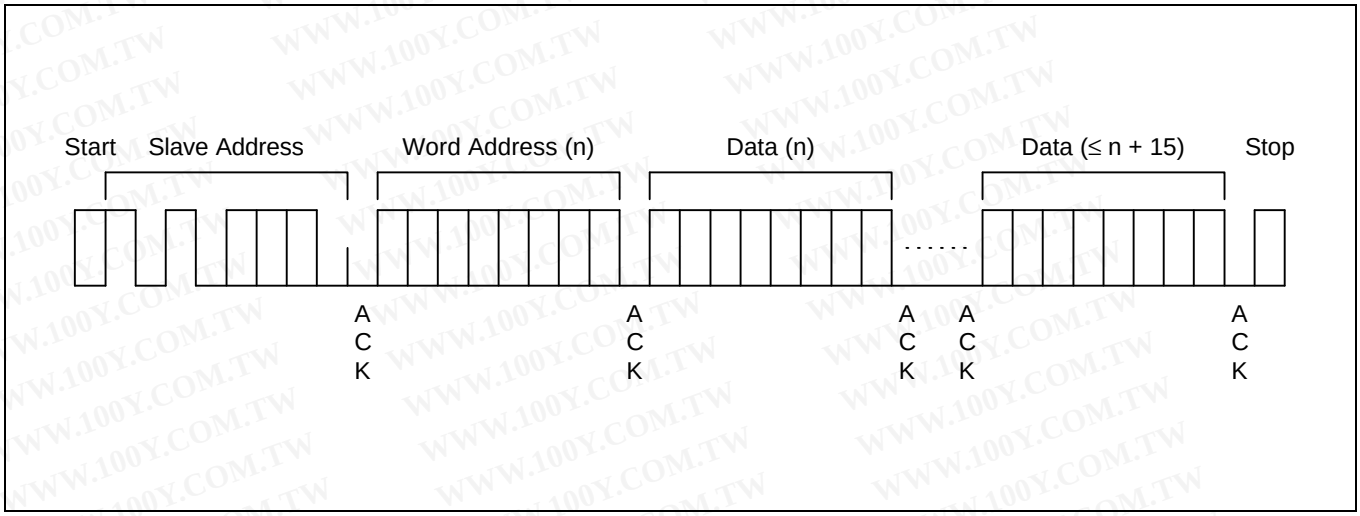


Figure 2-10. Page Write Operation

The S524A40X10/40X20/40X40 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.

If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the S524A40X10/40X20/40X40 word address pointer value “rolls over” and the previously received data is overwritten. If the master transmits less than 16 bytes and generates a stop condition, the S524A40X10/40X20/40X40 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524A40X10/40X20/40X40 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524A40X10/40X20/40X40 remains busy with the write operation, no ACK is returned. When the S524A40X10/40X20/40X40 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 2-11).

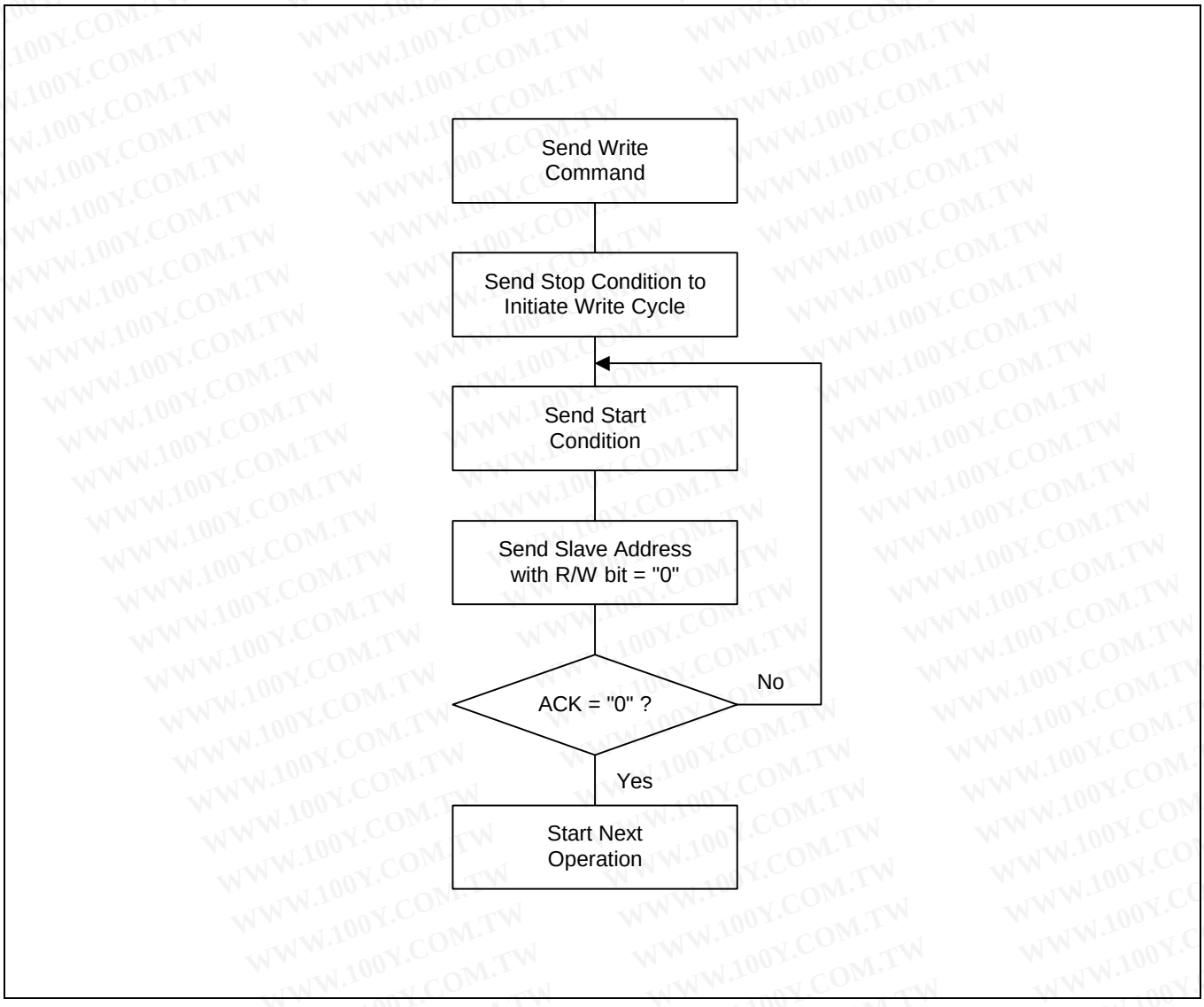


Figure 2-11. Master Polling for an ACK Signal from a Slave Device

SOFTWARE-BASED WRITE PROTECTION

You can write-protect the lower 128 bytes of the EEPROM, locations 00H–7FH, in one operation. To do this, you simply write a value to a one-time, write-only register. Once you have applied this write protection, any write attempt to access the lower 128-byte area is ignored. In other words, the write protection is permanent. The effect of such a failed attempt is processed in the same way as an invalid I^2C-bus protocol.

To enable write protection, you must execute a write operation to the write protection register. To access the write protection register, you use the device address “0110”. The word address and data in this write operation can be any value and the timing and wave form characteristics are identical to a normal byte write operation (see Figure 2-12).

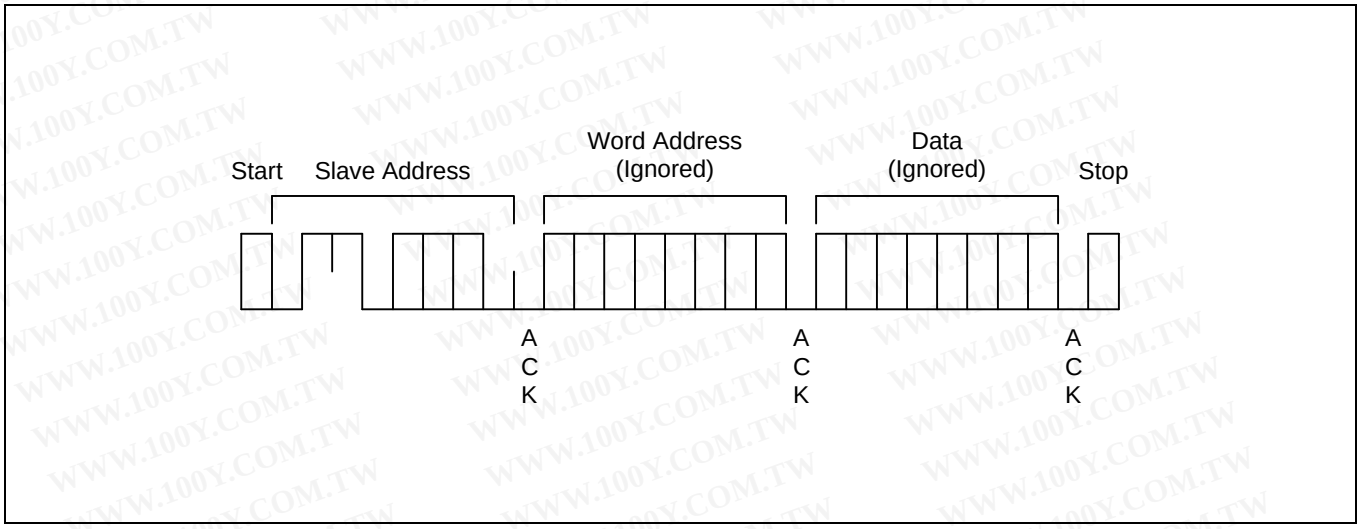


Figure 2-12. Write Protection Operation

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524A40X10/40X20/40X40. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to the memory is ignored.
The S524A40X10/40X20/40X40 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated. By connecting the WP pin to V_{SS}, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address “n”, the next read operation would access data at address “n+1”.

When the S524A40X10/40X20/40X40 receives a slave address with the R/W bit set to “1”, it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the S524A40X10/40X20/40X40 effectively stops the transmission (see Figure 2-13).

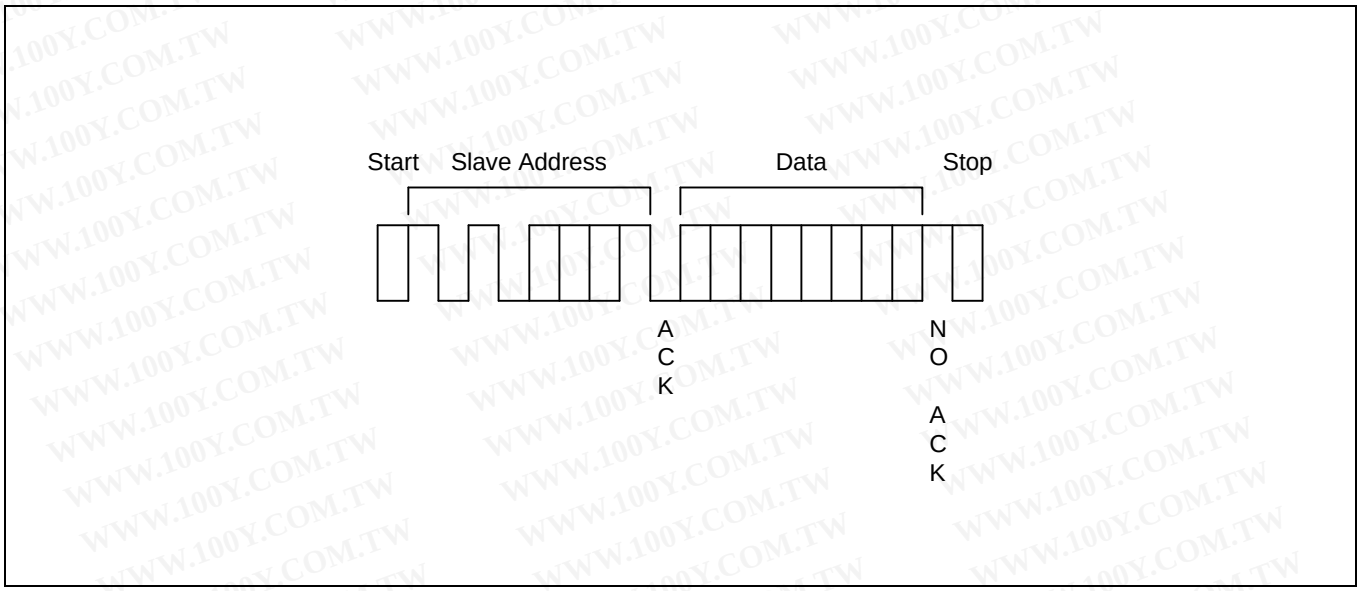


Figure 2-13. Current Address Byte Read Operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. This operation is performed in the following steps:

1. The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the S524A40X10/40X20/40X40 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to “1”.
3. The S524A40X10/40X20/40X40 then sends an ACK and the 8-bit data stored at the desired address.
4. At this point, the master does not acknowledge the transmission, but generates a stop condition instead.
5. In response, the S524A40X10/40X20/40X40 stops transmitting data and reverts to its stand-by mode (see Figure 2-14).

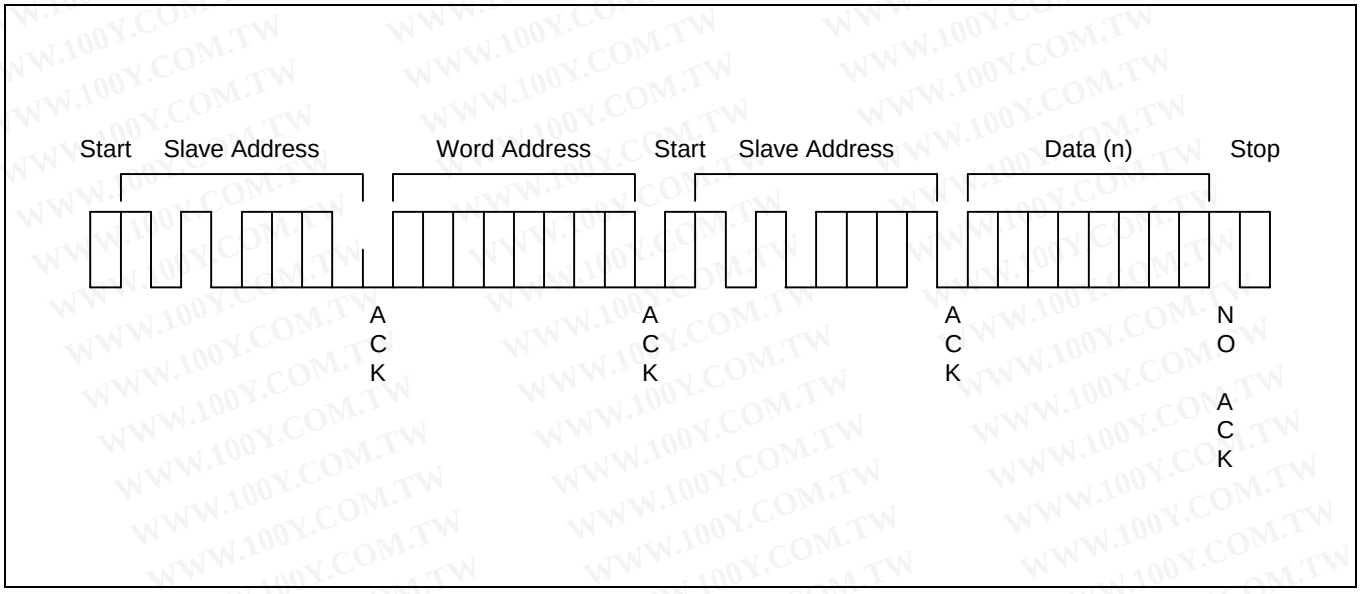


Figure 2-14. Random Address Byte Read Operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time, however, the master responds with an ACK, indicating that it requires additional data.
The S524A40X10/40X20/40X40 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

Using this method, data is output sequentially with the data from address “n” followed by the data from “n+1”. The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer “rolls over” and the S524A40X10/40X20/40X40 continues to transmit data for each ACK it receives from the master (see Figure 2-15).

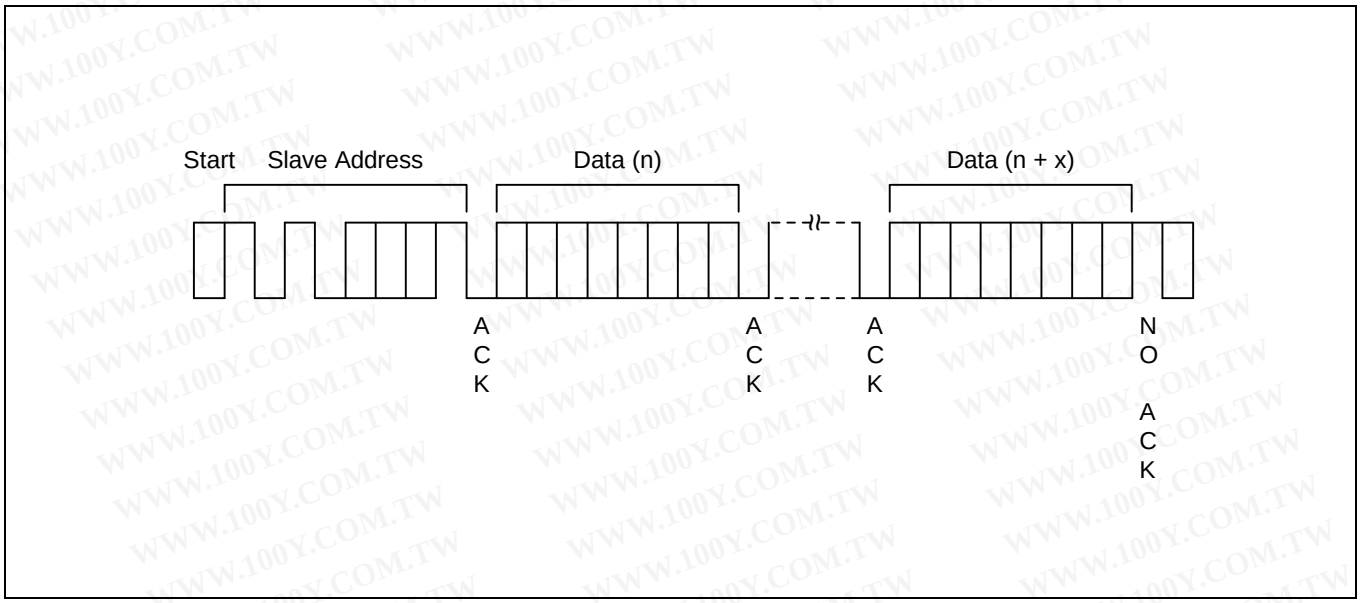


Figure 2-15. Sequential Read Operation

ELECTRICAL DATA

Table 2-3. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to + 7.0	V
Output voltage	V_O	–	– 0.3 to + 7.0	V
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	HBM	5000	V
		MM	500	

Table 2-4. D.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage		V_{IL}	SCL, SDA, A0, A1, A2	–	–	0.3 V_{CC}	V
Input high voltage		V_{IH}		0.7 V_{CC}	–	–	V
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Output leakage current		I_{LO}	V_O = 0 to V_{CC}	–	–	10	µA
Output low voltage		V_{OL}	I_{OL} = 0.15 mA, V_{CC} = 1.8 V	–	–	0.2	V
			I_{OL} = 2.1 mA, V_{CC} = 2.5 V	–	–	0.4	
Supply current	Write	I_{CC1}	V_{CC} = 5.5 V, 400 kHz	–	–	3	mA
		I_{CC2}	V_{CC} = 1.8 V, 100 kHz	–	–	1	
	Read	I_{CC3}	V_{CC} = 5.5 V, 400 kHz	–	–	0.2	
		I_{CC4}	V_{CC} = 1.8 V, 100 kHz	–	–	60	µA
Stand-by current		I_{CC5}	V_{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	–	–	5	µA
		I_{CC6}	V_{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	–	–	1	

Table 2-4. D.C. Electrical Characteristics (Continued)

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	25°C, 1MHz, V_{CC} = 5 V, V_{IN} = 0 V, A0, A1, A2, SCL and WP pin	–	–	10	pF
Input/output capacitance	$C_{I/O}$	25°C, 1MHz, V_{CC} = 5 V, $V_{I/O}$ = 0 V, SDA pin	–	–	10	

Table 2-5. A.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	V_{CC} = 1.8 to 5.5 V (Standard Mode)		V_{CC} = 2.5 to 5.5 V (Fast Mode)		Unit
			Min	Max	Min	Max	
External clock frequency	F_{CLK}	–	0	100	0	400	kHz
Clock high time	t_{HIGH}	–	4	–	0.6	–	µs
Clock low time	t_{LOW}	–	4.7	–	1.3	–	
Rising time	t_R	SDA, SCL	–	1	–	0.3	
Falling time	t_F	SDA, SCL	–	0.3	–	0.3	
Start condition hold time	$t_{HD:STA}$	–	4	–	0.6	–	
Start condition setup time	$t_{SU:STA}$	–	4.7	–	0.6	–	
Data input hold time	$t_{HD:DAT}$	–	0	–	0	–	
Data input setup time	$t_{SU:DAT}$	–	0.25	–	0.1	–	
Stop condition setup time	$t_{SU:STO}$	–	4	–	0.6	–	
Bus free time	t_{BUF}	Before new transmission	4.7	–	1.3	–	
Data output valid from clock low (note)	t_{AA}	–	0.3	3.5	–	0.9	
Noise spike width	t_{SP}	–	–	100	–	50	ns
Write cycle time	t_{WR}	–	–	5	–	5	ms

NOTES:

1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
2. When acting as a transmitter, the S524A40X10/40X20/40X40 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

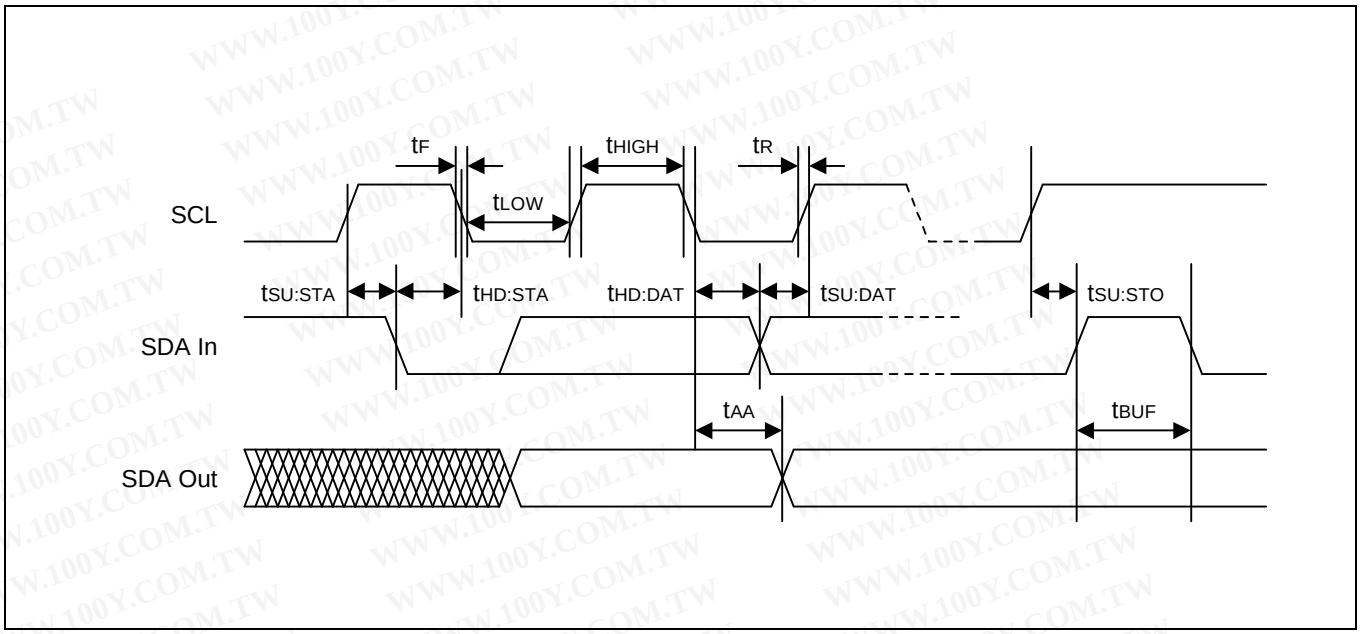


Figure 2-16. Timing Diagram for Bus Operations

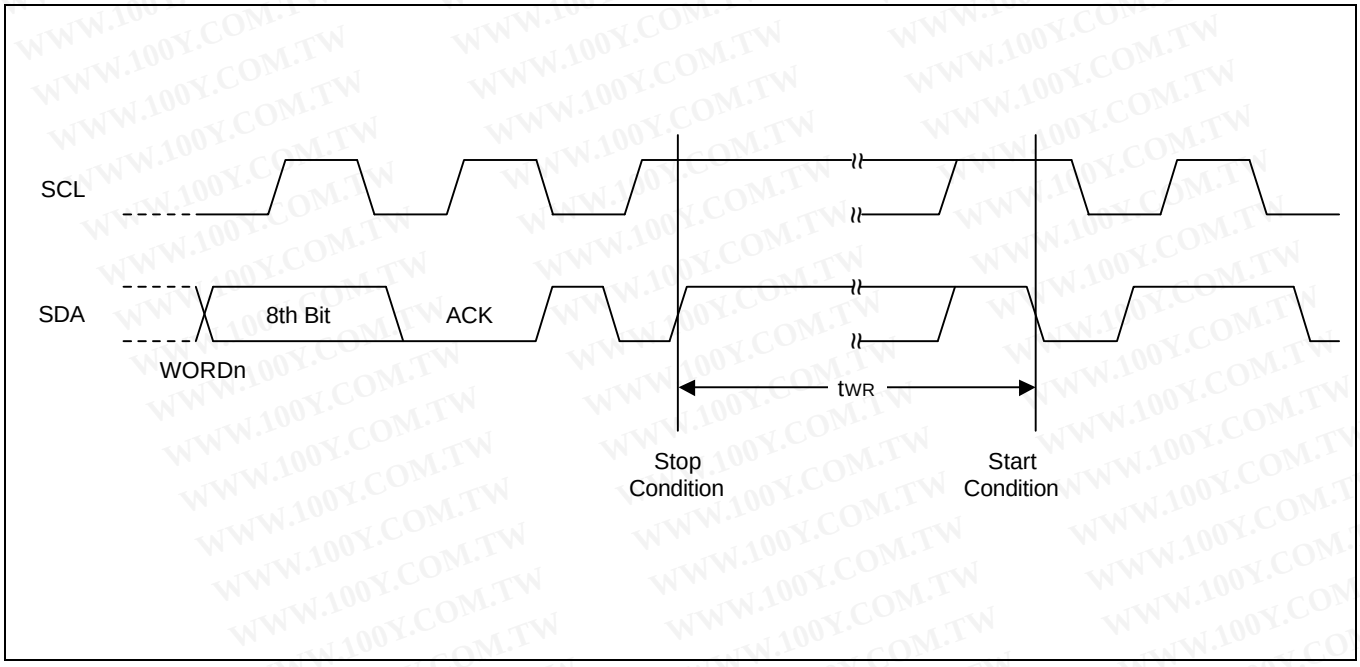


Figure 2-17. Write Cycle Timing Diagram

SAMSUNG ELECTRONICS

S524A40X11/40X21/ 40X41/60X81/60X51

1K/2K/4K/8K/16K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524A40X11/40X21/40X41/60X81/60X51 serial EEPROM has a 1,024/2,048/4,096/8,192/16,384-bit capacity, supporting the standard I²C™-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 16 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524A40X11/40X21/40X41/60X81/60X51 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 1K/2K/4K/8K/16K-bit (128/256/512/1,024/2,048-byte) storage area
- 16-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

Operating Characteristics

- Operating voltage
  - 1.8 V to 5.5 V
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 200 µA at 5.5 V
  - Maximum stand-by current: < 5 µA at 5.5 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 100 kHz at standard mode
  - 400 kHz at fast mode
- Electrostatic discharge (ESD)
  - 5,000 V (HBM)
  - 500 V (MM)

Packages

- 8-pin DIP, SOP, and TSSOP

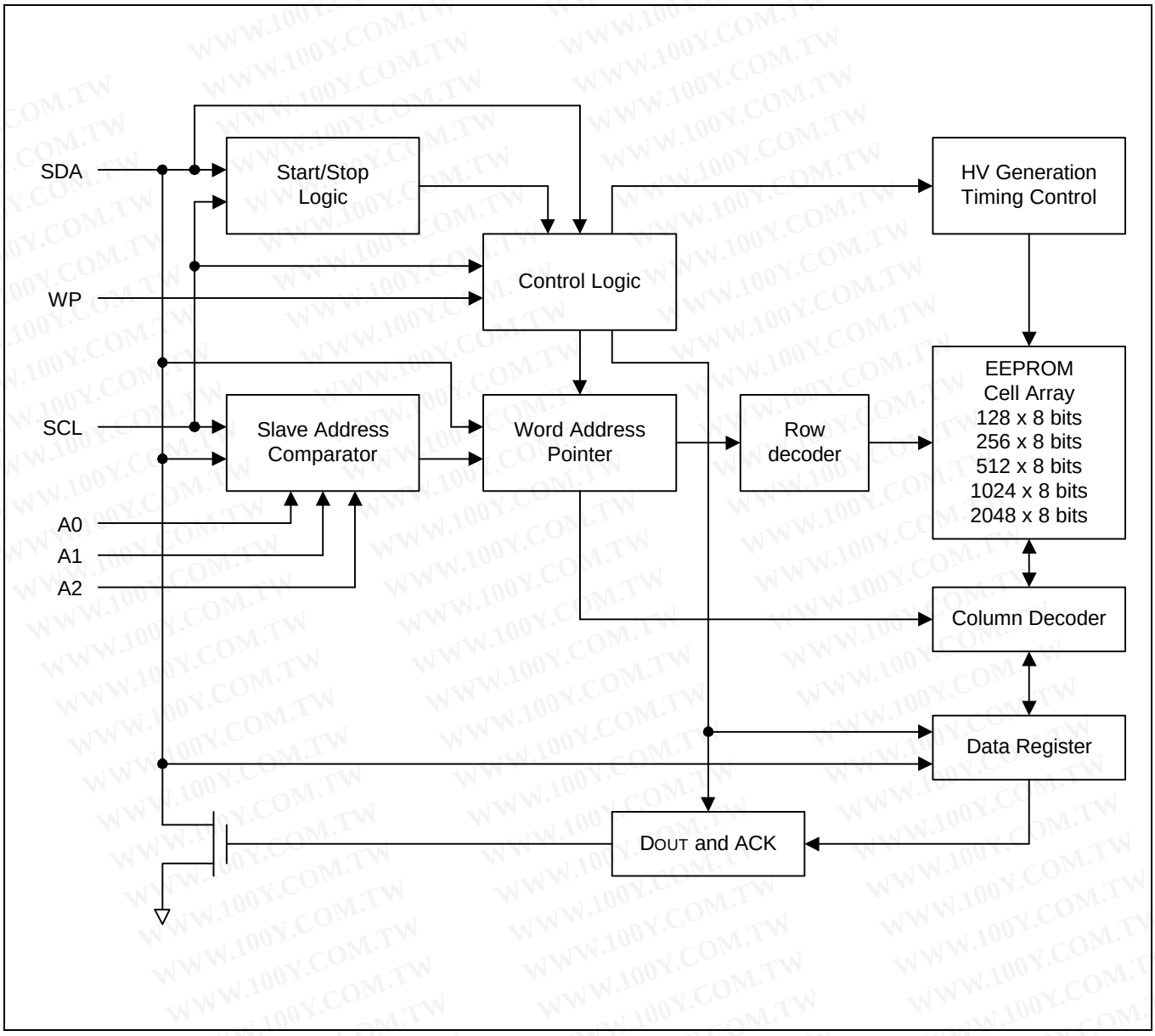
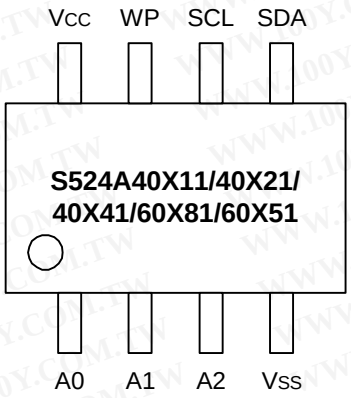


Figure 3-1. S524A40X11/40X21/40X41/60X81/60X51 Block Diagram



NOTE: The S524A40X11/40X21/40X41/60X81/60X51 is available in 8-pin DIP, SOP, and TSSOP package.

Figure 3-2. Pin Assignment Diagram

Table 3-1. S524A40X11/40X21/40X41/60X81/60X51 Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS}.	1
V_{SS}	–	Ground pin.	–
SDA	I/O	Bi-directional data pin for the I^2C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V_{CC}. Typical values for this pull-up resistor are 4.7 kΩ (100 kHz) and 1 kΩ (400 kHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC}, the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS}, the write function is enabled. This pin is internally pulled down to V_{SS}.	1
V_{CC}	–	Single power supply.	–

NOTE: See the following page for diagrams of pin circuit types 1, 2, and 3.

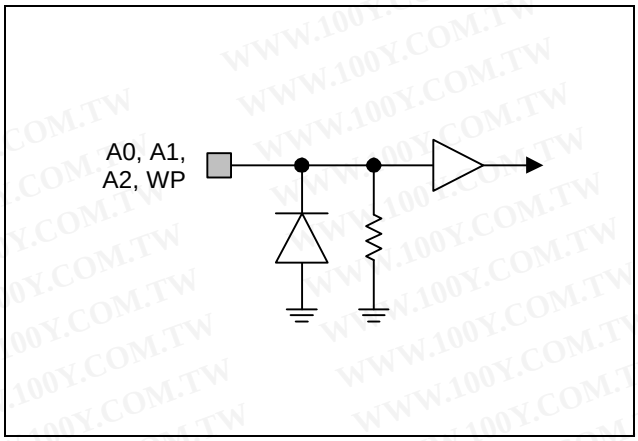


Figure 3-3. Pin Circuit Type 1

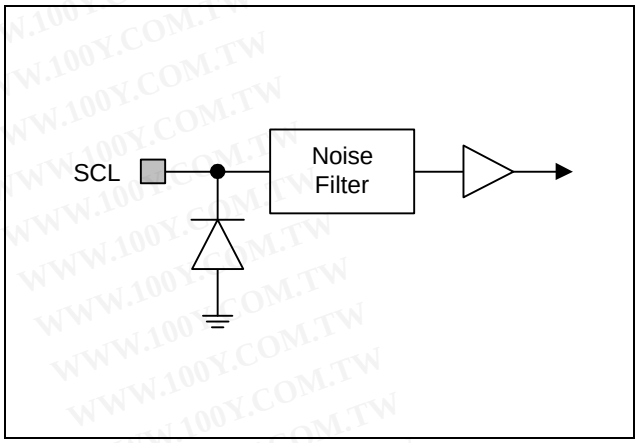


Figure 3-4. Pin Circuit Type 2

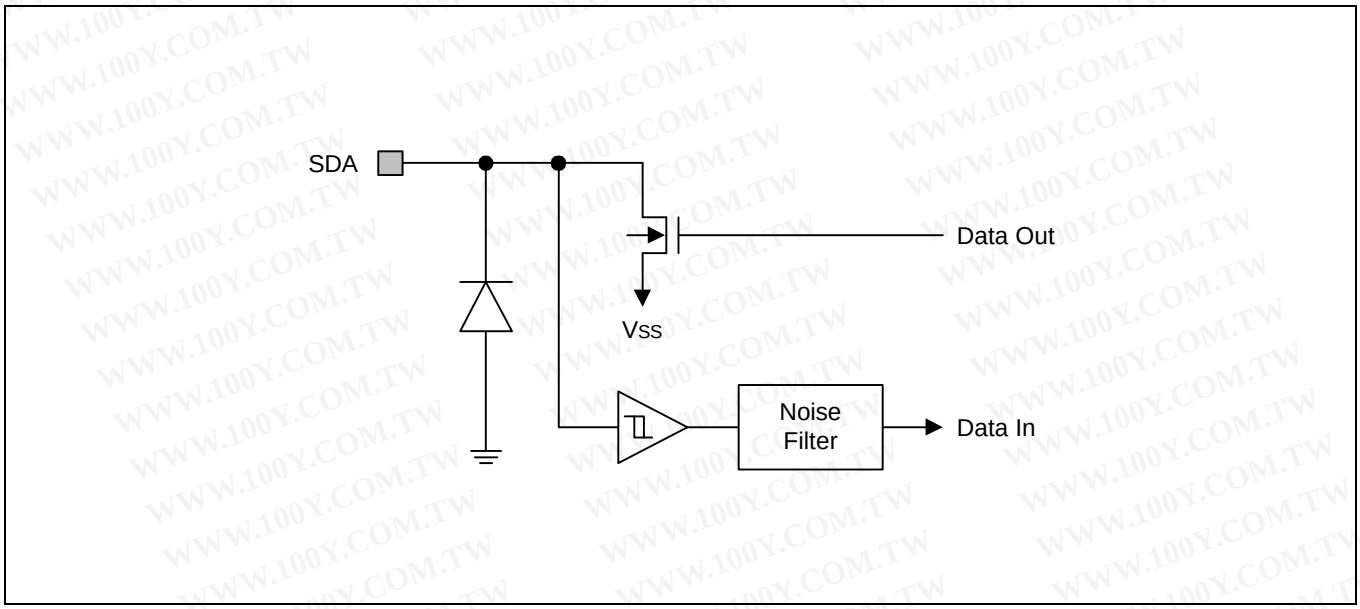


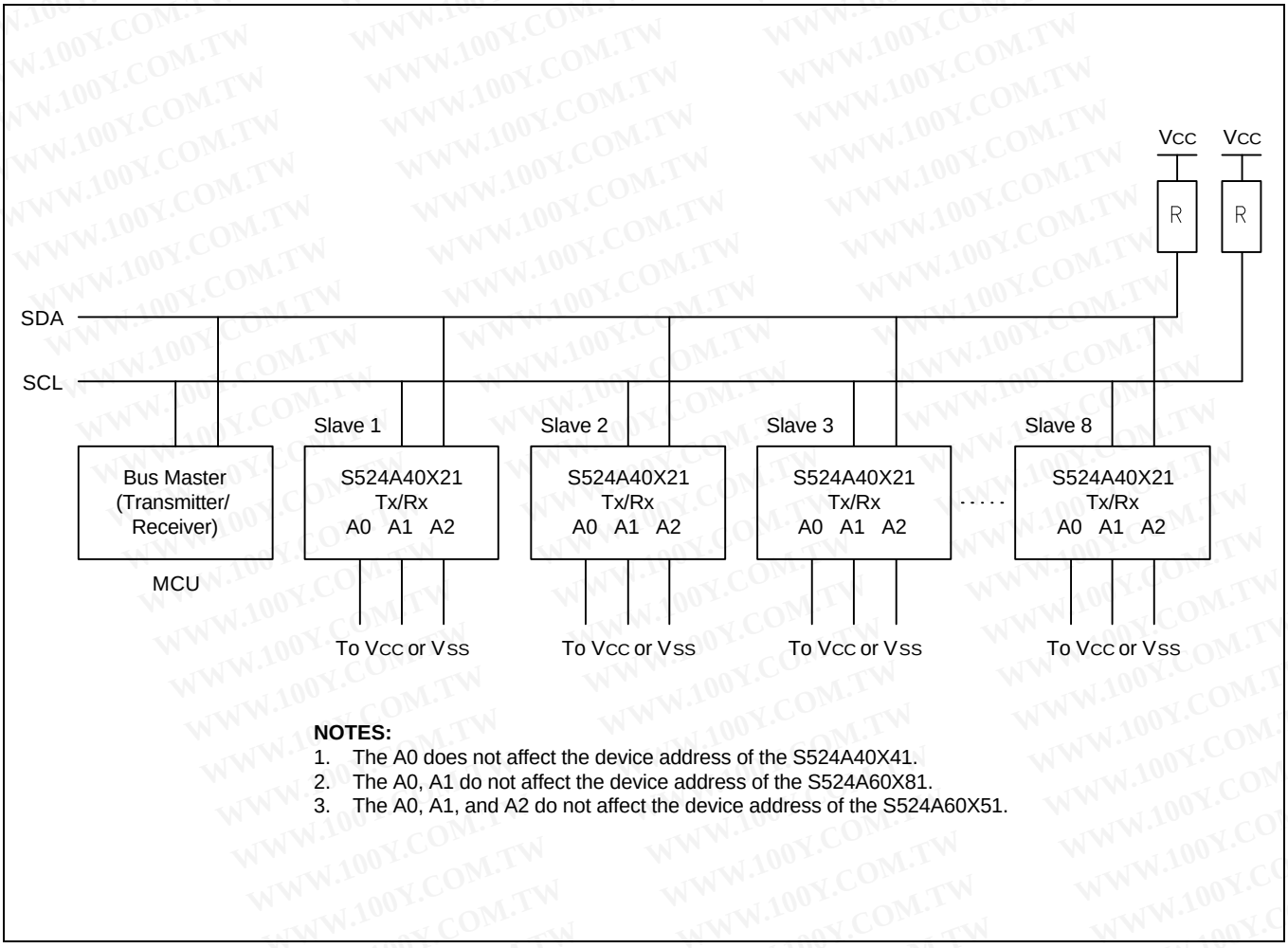
Figure 3-5. Pin Circuit Type 3

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524A40X11/40X21/40X41/60X81/60X51 supports the I²C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as the “transmitter” and any device that gets data from the bus is the “receiver.” The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight S524A40X11/40X21 (four S524A40X41, two for S524A60X81, one for S524A60X51) devices can be connected to the same I²C-bus as slaves (see Figure 3-6). Both the master and slaves can operate as transmitter or receiver, but the master device determines which bus operating mode would be active.



NOTES:
1. The A0 does not affect the device address of the S524A40X41.
2. The A0, A1 do not affect the device address of the S524A60X81.
3. The A0, A1, and A2 do not affect the device address of the S524A60X51.

Figure 3-6. Typical Configuration (16 Kbits of Memory on the I²C-Bus)

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

— A new data transfer can be initiated only when the bus is currently not busy.

— MSB is always transferred first in transmitting data.

— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- Start condition: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition (see Figure 3-7).

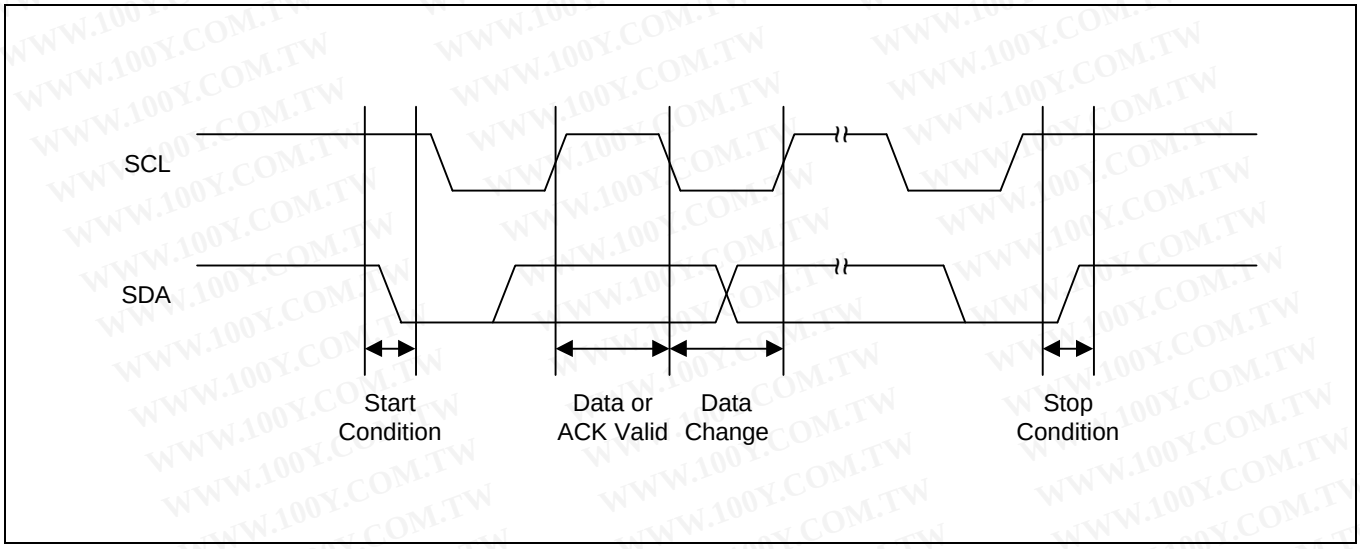


Figure 3-7. Data Transmission Sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.
- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 3-8). But the slave does not send an ACK if an internal write cycle is still in progress.

  In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

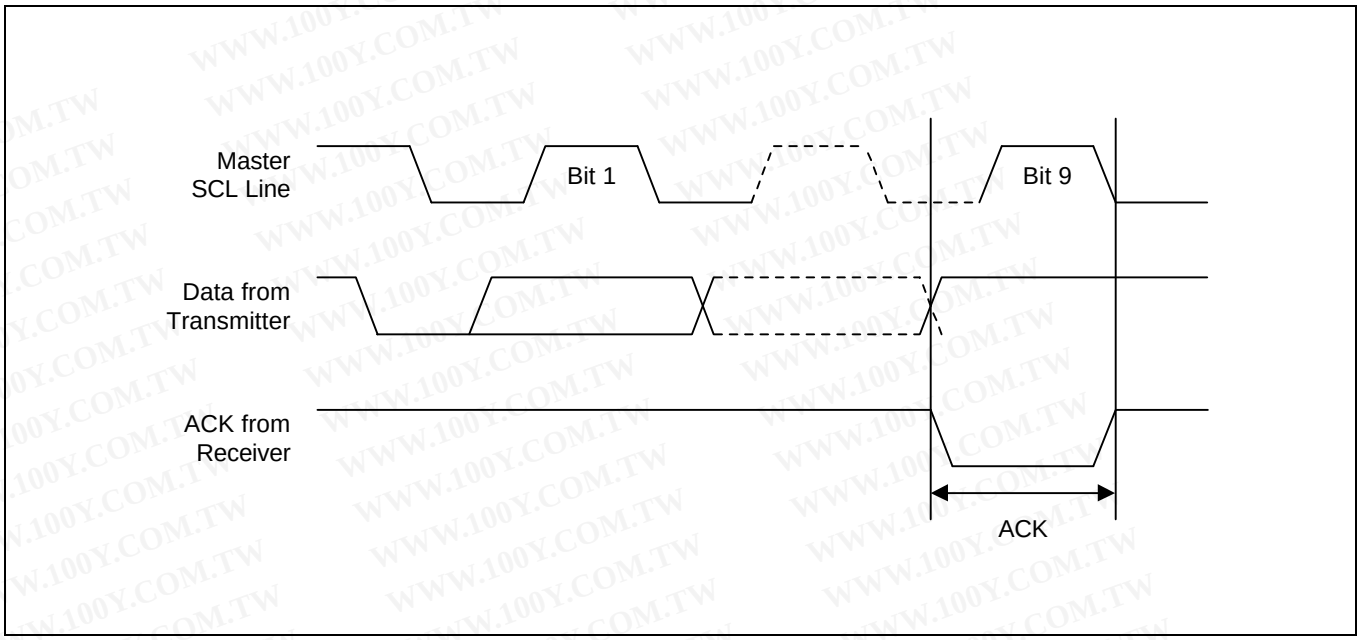


Figure 3-8. Acknowledge Response From Receiver

- Slave Address: After the master initiates a Start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the “device identifier”. The identifier for the S524A40X11/40X21/40X41/60X81/60X51 is “1010B”. The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1 and A2 pins. Using this addressing scheme, you can cascade up to eight S524A40X11/40X21 or four S524A40X41 or two S524A60X81 or one S524A60X51 on the bus (see Table 3-2 below). The b1 for S524A40X41 or the b1, b2 for S524A60X81 or the b1, b2, b3 for S524A60X51 are used by the master to select which of the blocks of internal memory (1 block = 256 words) are to be accessed. The bits are in effect the most significant bits of the word address.
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is “1”, a read operation is executed. If it is “0”, a write operation is executed.

Table 3-2. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	b7	b6	b5	b4	b3	b2	b1	b0
S524A40X11/40X21	1	0	1	0	A2	A1	A0	R/W
S524A40X41	1	0	1	0	A2	A1	B0	R/W
S524A60X81	1	0	1	0	A2	B1	B0	R/W
S524A60X51	1	0	1	0	B2	B1	B0	R/W

NOTE: The B2, B1, B0 correspond to the MSB of the memory array address word.

BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the S524A40X11/40X21/40X41/60X81/60X51 slave device (see Figure 3-9).

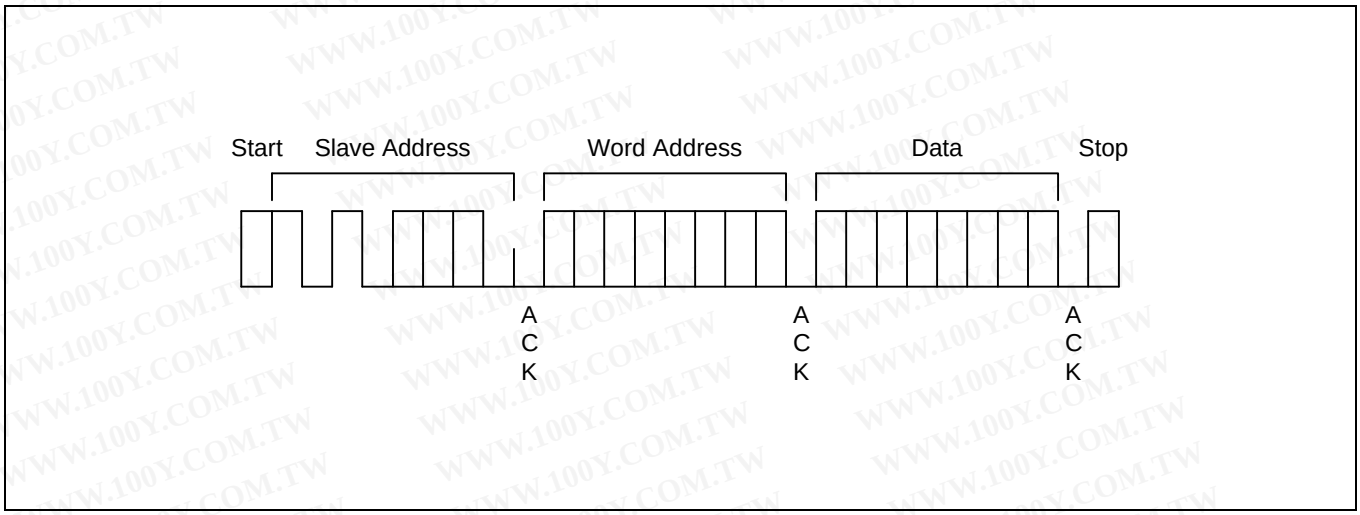


Figure 3-9. Byte Write Operation

Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to “0” onto the bus. Then the addressed S524A40X11/40X21/40X41/60X81/60X51 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the S524A40X11/40X21/40X41/60X81/60X51.

When the S524A40X11/40X21/40X41/60X81/60X51 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the S524A40X11/40X21/40X41/60X81/60X51 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the S524A40X11/40X21/40X41/60X81/60X51 begins the internal write cycle.

While the internal write cycle is in progress, all S524A40X11/40X21/40X41/60X81/60X51 inputs are disabled and the S524A40X11/40X21/40X41/60X81/60X51 does not respond to additional requests from the master.

PAGE WRITE OPERATION

The S524A40X11/40X21/40X41/60X81/60X51 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The S524A40X11/40X21/40X41/60X81/60X51 responds with an ACK each time it receives a complete byte of data (see Figure 3-10).

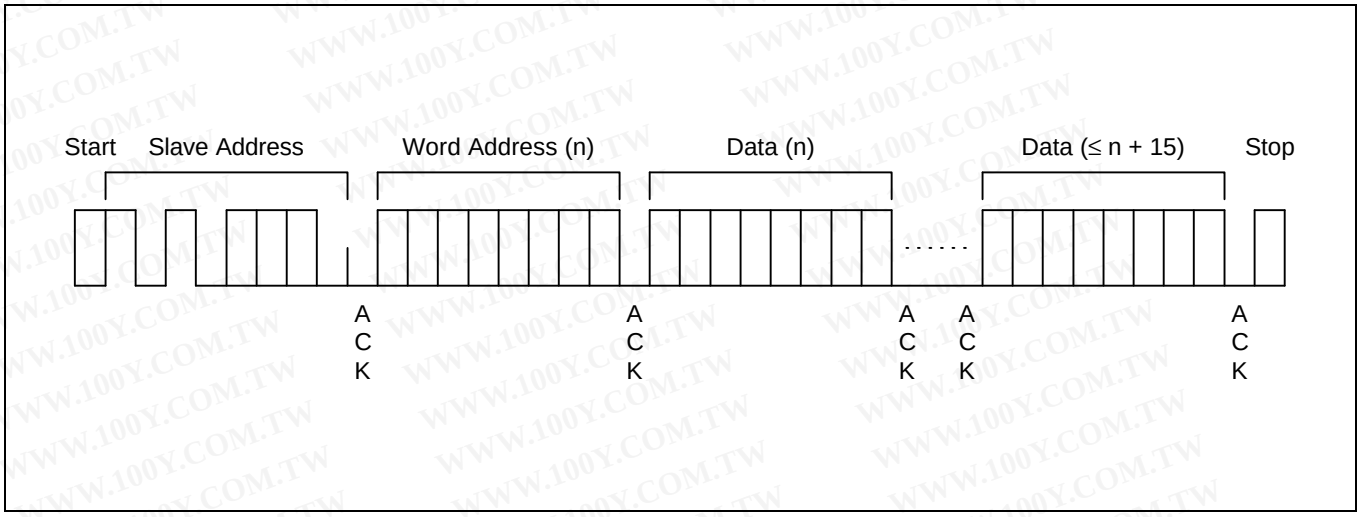


Figure 3-10. Page Write Operation

The S524A40X11/40X21/40X41/60X81/60X51 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.

If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the S524A40X11/40X21/40X41/60X81/60X51 word address pointer value “rolls over” and the previously received data is overwritten. If the master transmits less than 16 bytes and generates a stop condition, the S524A40X11/40X21/40X41/60X81/60X51 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524A40X11/40X21/40X41/60X81/60X51 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524A40X11/40X21/40X41/60X81/60X51 remains busy with the write operation, no ACK is returned. When the S524A40X11/40X21/40X41/60X81/60X51 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 3-11).

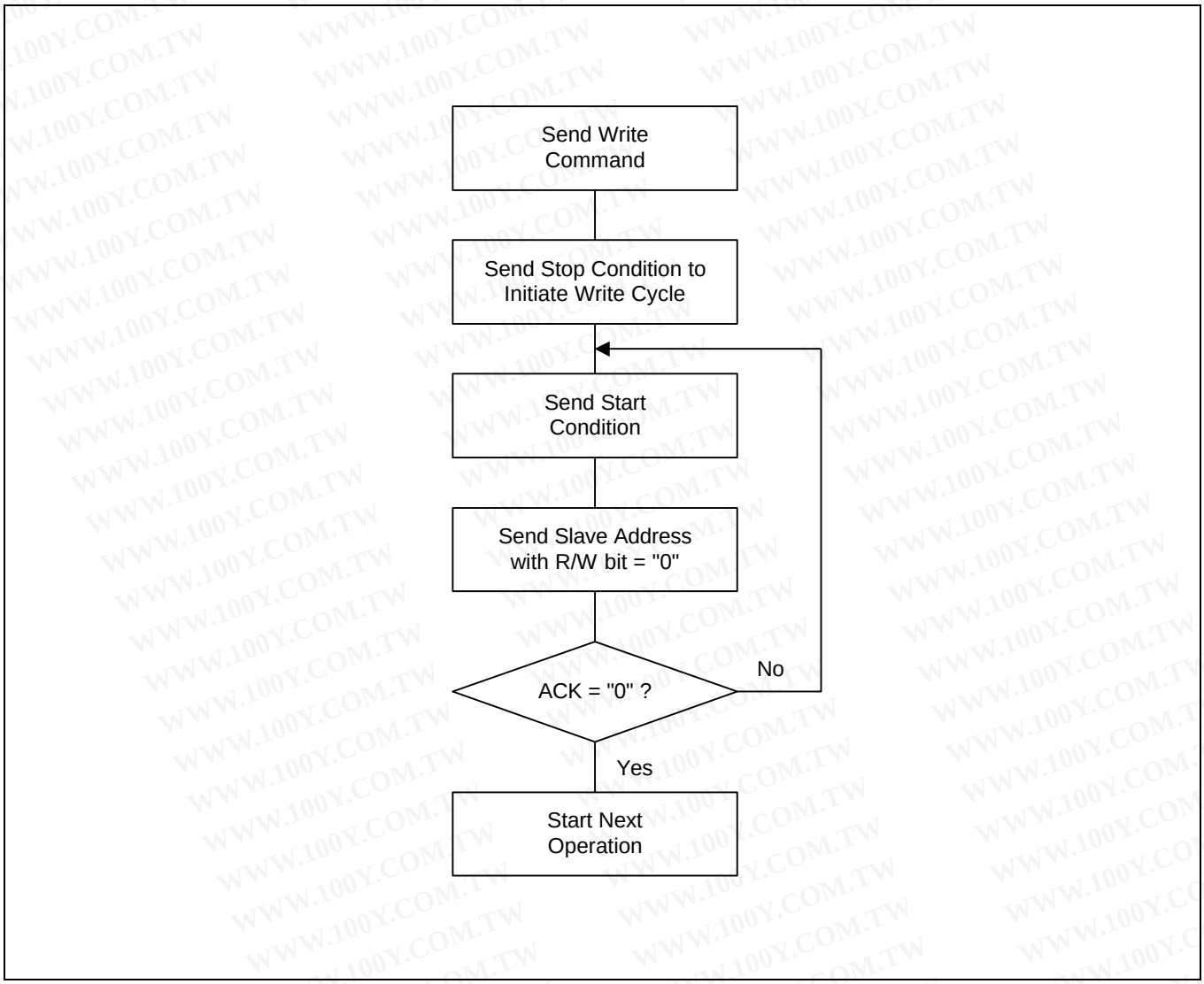


Figure 3-11. Master Polling for an ACK Signal from a Slave Device

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524A40X11/40X21/40X41/60X81/60X51. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to the memory is ignored.
The S524A40X11/40X21/40X41/60X81/60X51 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated. By connecting the WP pin to V_{SS}, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address “n”, the next read operation would access data at address “n+1”.

When the S524A40X11/40X21/40X41/60X81/60X51 receives a slave address with the R/W bit set to “1”, it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the S524A40X11/40X21/40X41/60X81/60X51 effectively stops the transmission (see Figure 3-12).

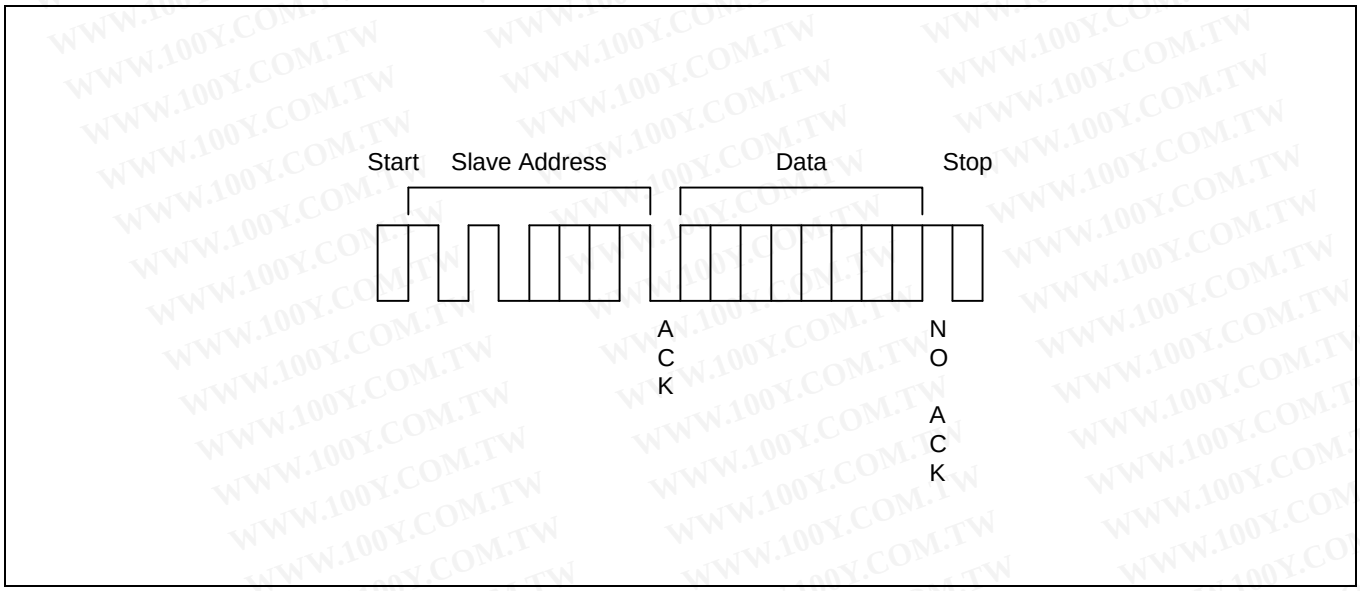


Figure 3-12. Current Address Byte Read Operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. This operation is performed in the following steps:

1. The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the S524A40X11/40X21/40X41/60X81/60X51 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to “1”.
3. The S524A40X11/40X21/40X41/60X81/60X51 then sends an ACK and the 8-bit data stored at the desired address.
4. At this point, the master does not acknowledge the transmission, but generates a stop condition instead.
5. In response, the S524A40X11/40X21/40X41/60X81/60X51 stops transmitting data and reverts to its stand-by mode (see Figure 3-13).

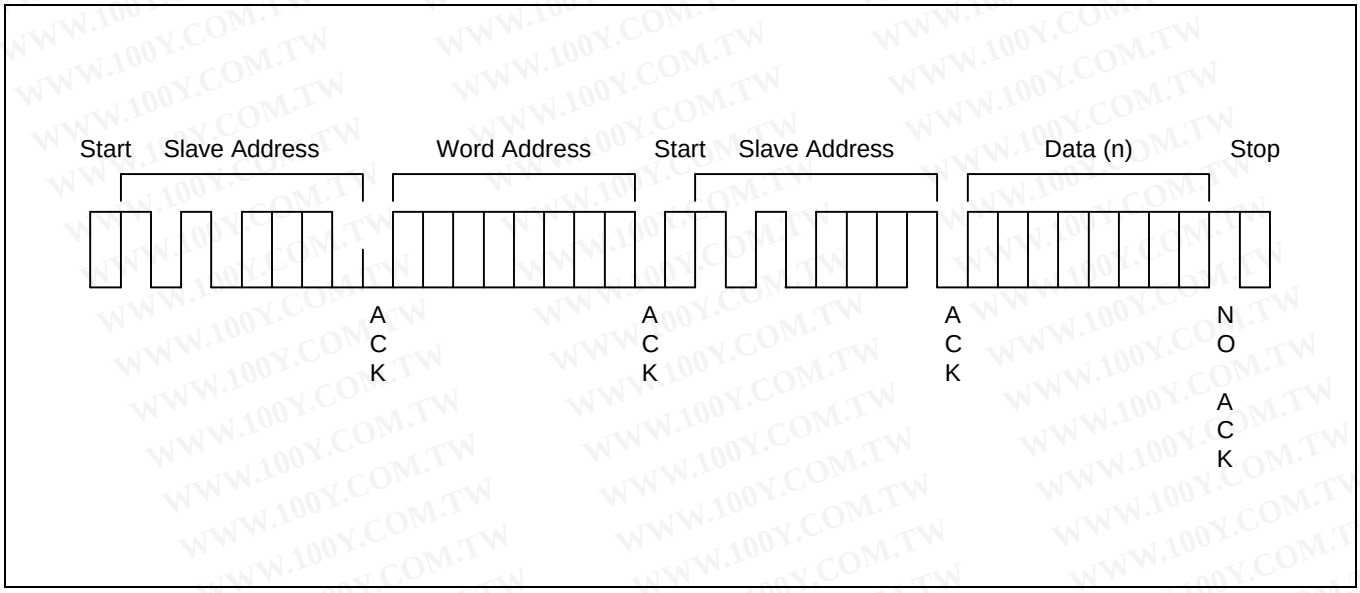


Figure 3-13. Random Address Byte Read Operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time, however, the master responds with an ACK, indicating that it requires additional data.
The S524A40X11/40X21/40X41/60X81/60X51 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

Using this method, data is output sequentially with the data from address “n” followed by the data from “n+1”. The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer “rolls over” and the S524A40X11/40X21/40X41/60X81/60X51 continues to transmit data for each ACK it receives from the master (see Figure 3-14).

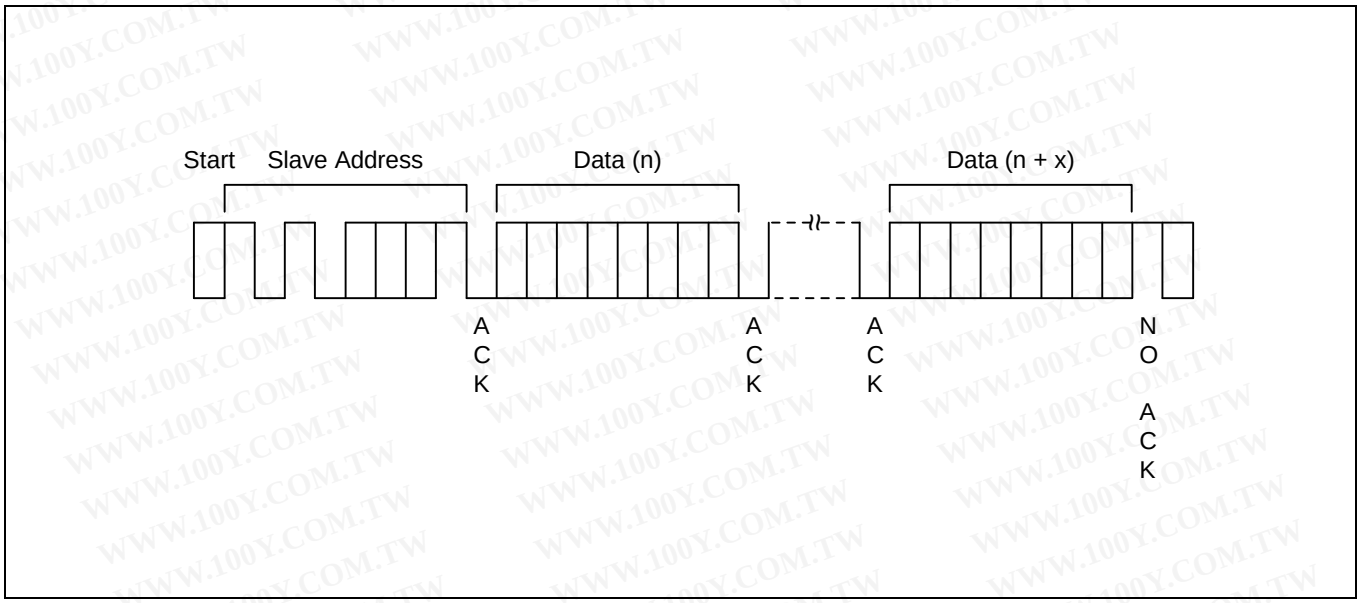


Figure 3-14. Sequential Read Operation

ELECTRICAL DATA

Table 3-3. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to + 7.0	V
Output voltage	V_O	–	– 0.3 to + 7.0	V
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	HBM	5000	V
		MM	500	

Table 3-4. D.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage		V_{IL}	SCL, SDA, A0, A1, A2	–	–	0.3 V_{CC}	V
Input high voltage		V_{IH}		0.7 V_{CC}	–	–	V
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Output leakage current		I_{LO}	V_O = 0 to V_{CC}	–	–	10	µA
Output low voltage		V_{OL}	I_{OL} = 0.15 mA, V_{CC} = 1.8 V	–	–	0.2	V
			I_{OL} = 2.1 mA, V_{CC} = 2.5 V	–	–	0.4	
Supply current	Write	I_{CC1}	V_{CC} = 5.5 V, 400 kHz	–	–	3	mA
		I_{CC2}	V_{CC} = 1.8 V, 100 kHz	–	–	1	
	Read	I_{CC3}	V_{CC} = 5.5 V, 400 kHz	–	–	0.2	
		I_{CC4}	V_{CC} = 1.8 V, 100 kHz	–	–	60	µA
Stand-by current		I_{CC5}	V_{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	–	–	5	µA
		I_{CC6}	V_{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	–	–	1	

Table 3-4. D.C. Electrical Characteristics (Continued)

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	25 °C, 1MHz, V_{CC} = 5 V, V_{IN} = 0 V, A0, A1, A2, SCL and WP pin	–	–	10	pF
Input/output capacitance	$C_{I/O}$	25 °C, 1MHz, V_{CC} = 5 V, $V_{I/O}$ = 0 V, SDA pin	–	–	10	

Table 3-5. A.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	V_{CC} = 1.8 to 5.5 V (Standard Mode)		V_{CC} = 2.5 to 5.5 V (Fast Mode)		Unit
			Min	Max	Min	Max	
External clock frequency	F_{CLK}	–	0	100	0	400	kHz
Clock high time	t_{HIGH}	–	4	–	0.6	–	µs
Clock low time	t_{LOW}	–	4.7	–	1.3	–	
Rising time	t_R	SDA, SCL	–	1	–	0.3	
Falling time	t_F	SDA, SCL	–	0.3	–	0.3	
Start condition hold time	$t_{HD:STA}$	–	4	–	0.6	–	
Start condition setup time	$t_{SU:STA}$	–	4.7	–	0.6	–	
Data input hold time	$t_{HD:DAT}$	–	0	–	0	–	
Data input setup time	$t_{SU:DAT}$	–	0.25	–	0.1	–	
Stop condition setup time	$t_{SU:STO}$	–	4	–	0.6	–	
Bus free time	t_{BUF}	Before new transmission	4.7	–	1.3	–	
Data output valid from clock low (note)	t_{AA}	–	0.3	3.5	–	0.9	
Noise spike width	t_{SP}	–	–	100	–	50	ns
Write cycle time	t_{WR}	–	–	5	–	5	ms

NOTES:

1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
2. When acting as a transmitter, the S524A40X11/40X21/40X41/60X81/60X51 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

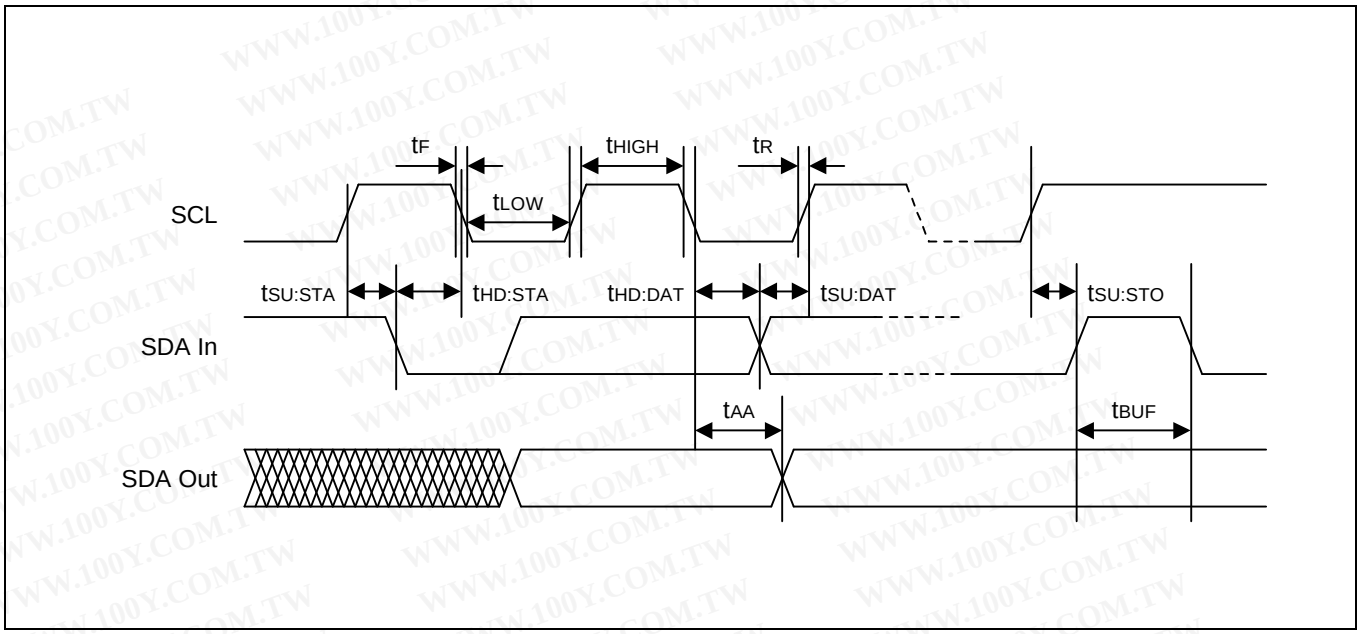


Figure 3-15. Timing Diagram for Bus Operations

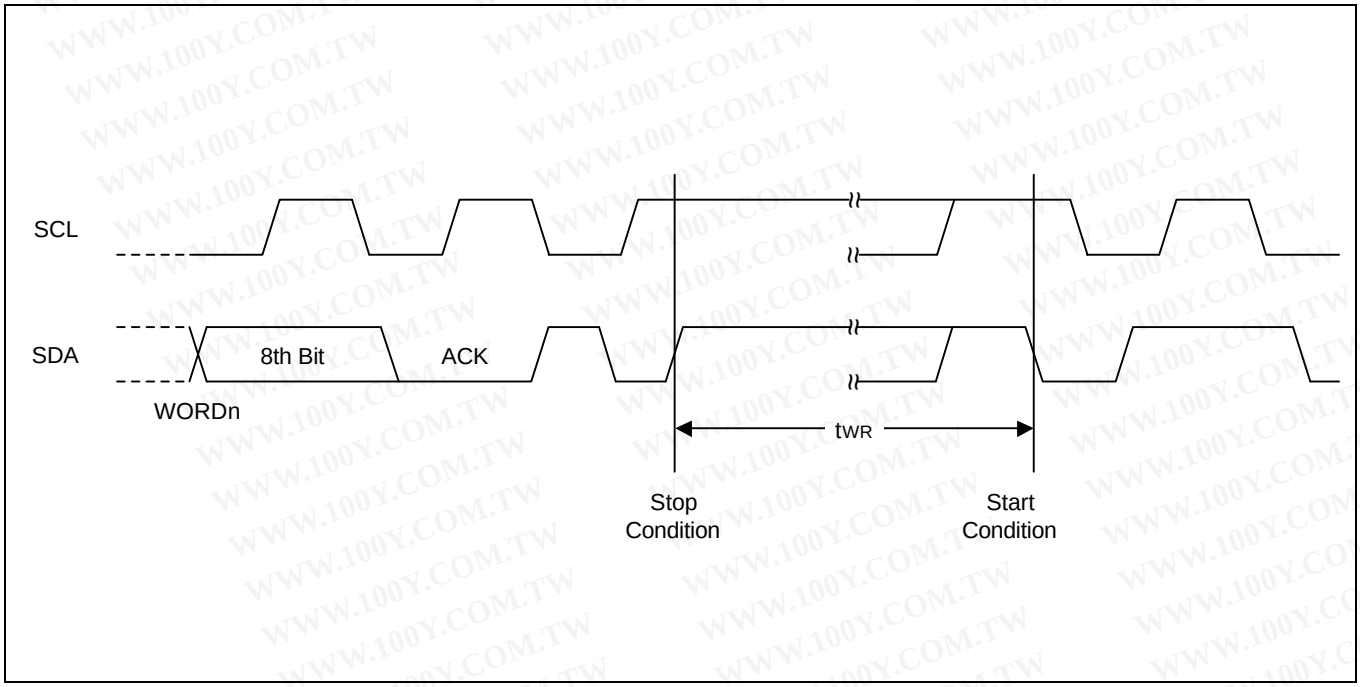


Figure 3-16. Write Cycle Timing Diagram

SAMSUNG ELECTRONICS

S524AB0X91/B0XB1

32K/64K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524AB0X91/B0XB1 serial EEPROM has a 32K/64K-bit (4,096/8,192 bytes) capacity, supporting the standard I²C™-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 32 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524AB0X91/B0XB1 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 32K/64K-bit (4,096/8,192 bytes) storage area
- 32-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

Operating Characteristics

- Operating voltage
  - 1.8 V to 5.5 V
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 400 µA at 5.5 V
  - Maximum stand-by current: < 5 µA at 5.5 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 100 kHz at standard mode
  - 400 kHz at fast mode
- Electrostatic discharge (ESD)
  - 5,000 V (HBM)
  - 500 V (MM)

Packages

- 8-pin DIP, SOP, and TSSOP

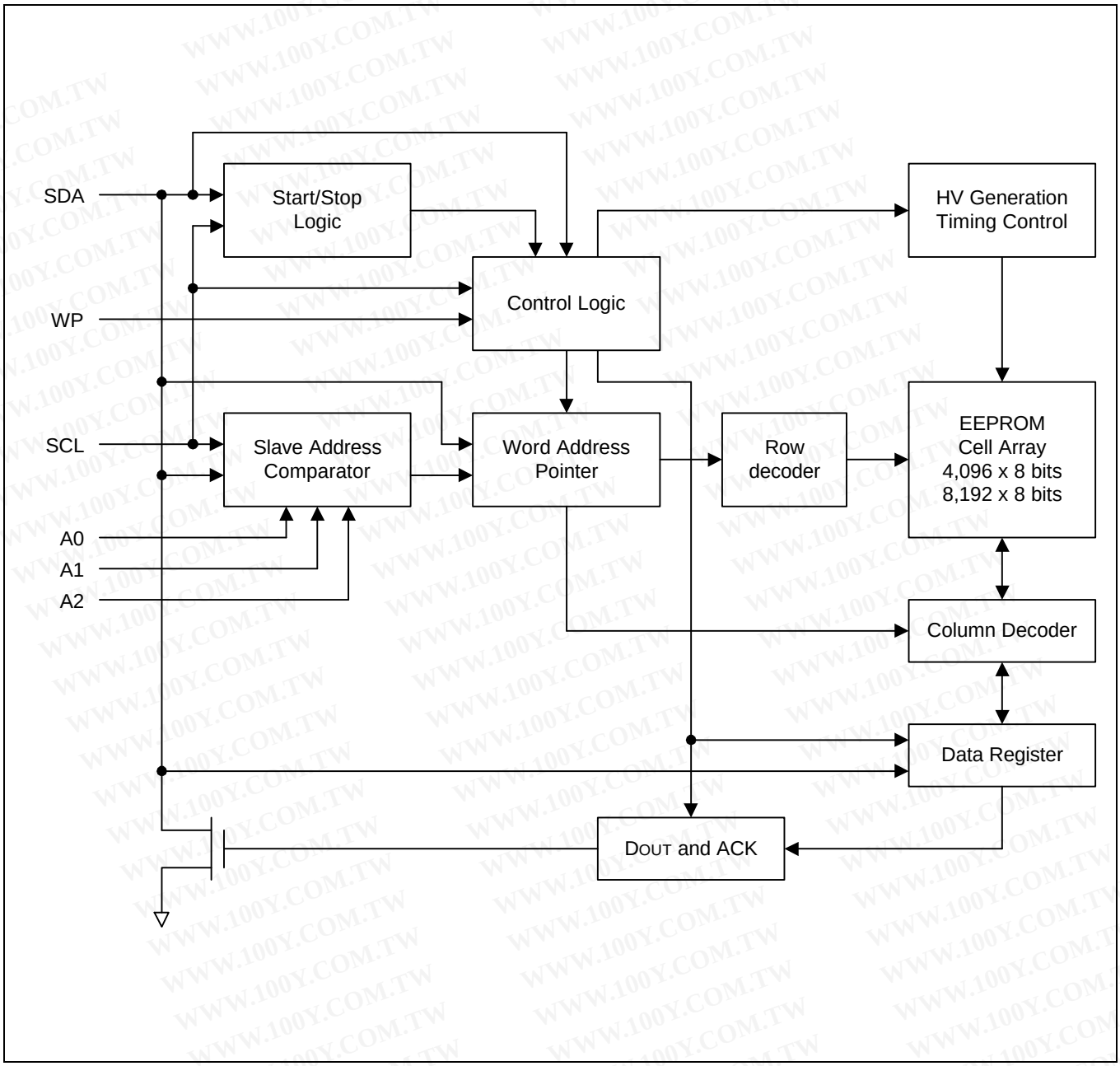
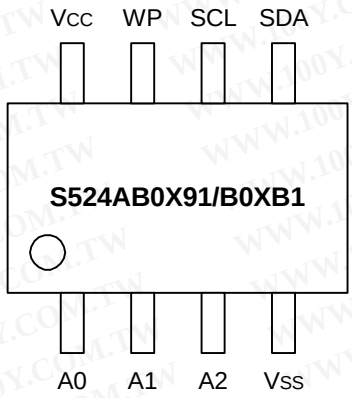


Figure 4-1. S524AB0X91/B0XB1 Block Diagram



NOTE: The S524AB0X91/B0XB1 is available in 8-pin DIP, SOP, and TSSOP package.

Figure 4-2. Pin Assignment Diagram

Table 4-1. S524AB0X91/B0XB1 Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS}.	1
V_{SS}	–	Ground pin.	–
SDA	I/O	Bi-directional data pin for the I^2C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V_{DD}. Typical values for this pull-up resistor are 4.7 KΩ (100 KHz) and 1 KΩ (400 KHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC}, the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS}, the write function is enabled. This pin is internally pulled down to V_{SS}.	1
V_{CC}	–	Single power supply.	–

NOTE: See the following page for diagrams of pin circuit types 1, 2, and 3.

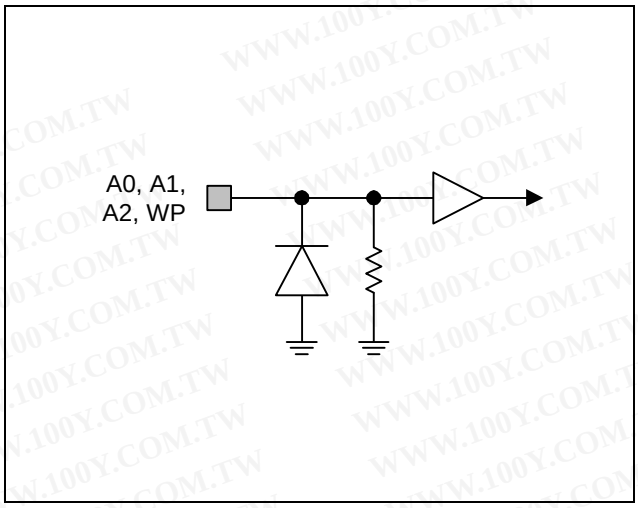


Figure 4-3. Pin Circuit Type 1

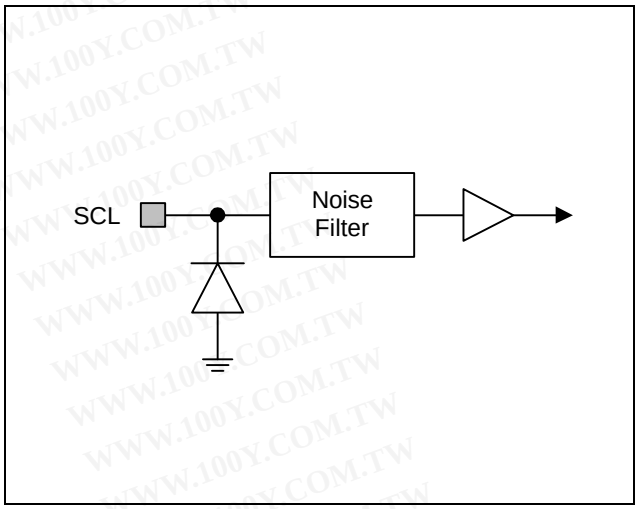


Figure 4-4. Pin Circuit Type 2

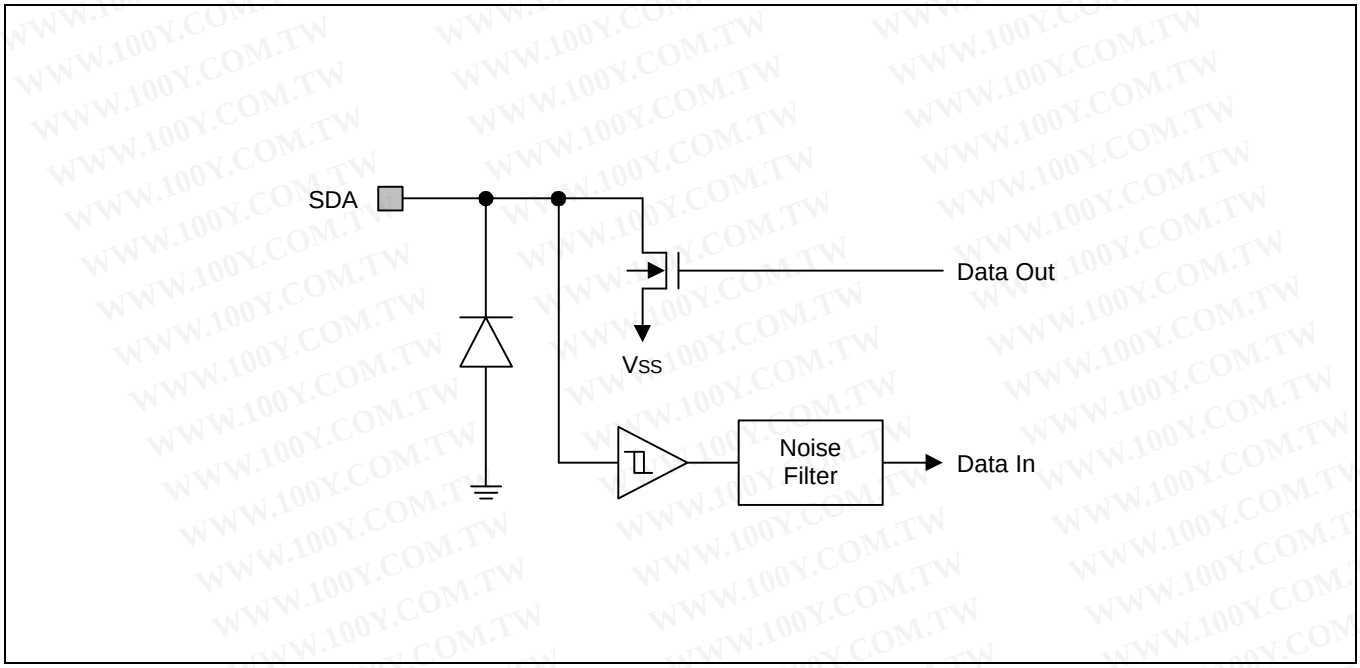


Figure 4-5. Pin Circuit Type 3

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524AB0X91/B0XB1 supports the I²C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as a “transmitter” and any device that gets data from the bus is a “receiver.” The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight S524AB0X91/B0XB1 devices can be connected to the same I²C-bus as slaves (see Figure 4-6). Both the master and slaves can operate as a transmitter or a receiver, but the master device determines which bus operating mode would be active.

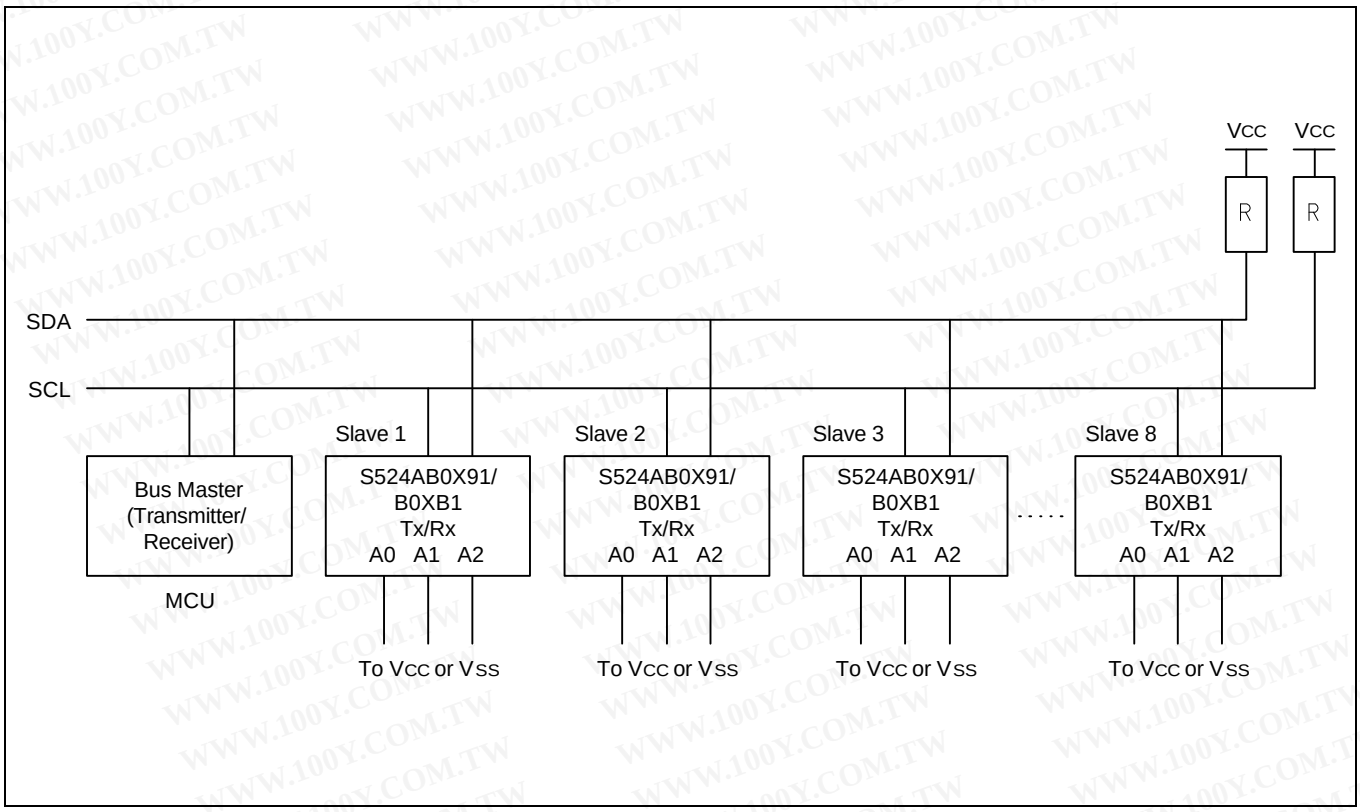


Figure 4-6. Typical Configuration

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

— A new data transfer can be initiated only when the bus is currently not busy.

— MSB is always transferred first in transmitting data.

— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain in High level when the bus is not active.
- Start condition: A start condition is initiated by a High-to-Low transition of the SDA line while SCL remains in High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains in High level. All bus operations must be completed by a stop condition (see Figure 4-7).

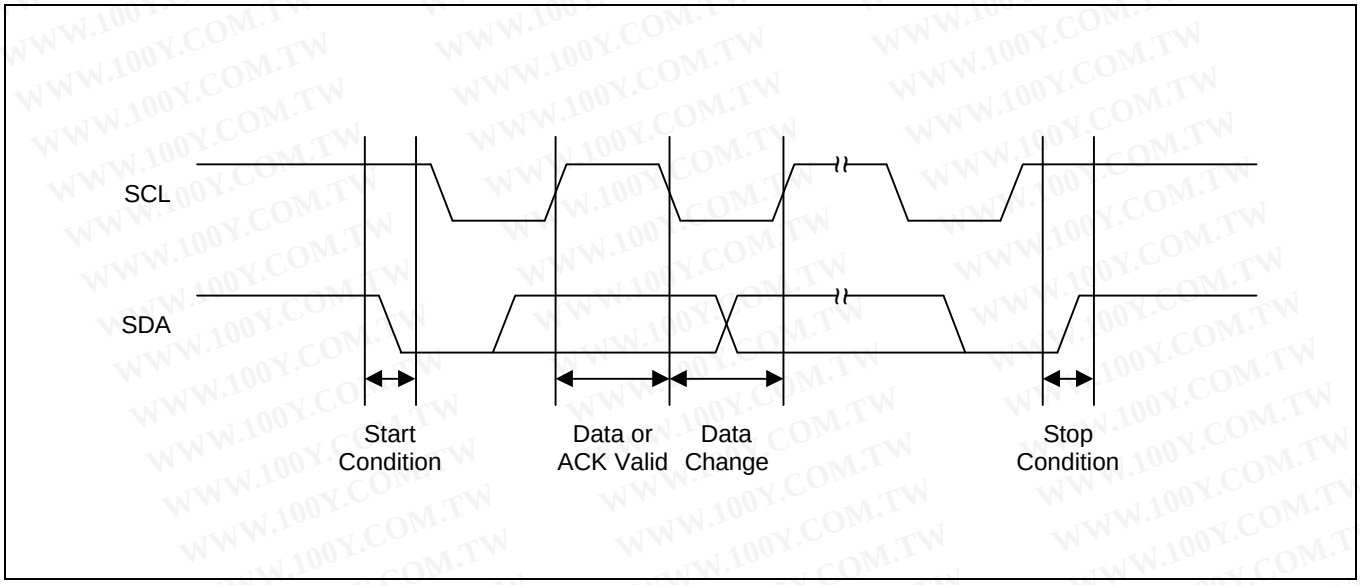


Figure 4-7. Data Transmission Sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.
- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it has successfully received the eight bits of data (see Figure 4-8). But the slave does not send an ACK if an internal write cycle is still in progress.

  In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected but no stop condition, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

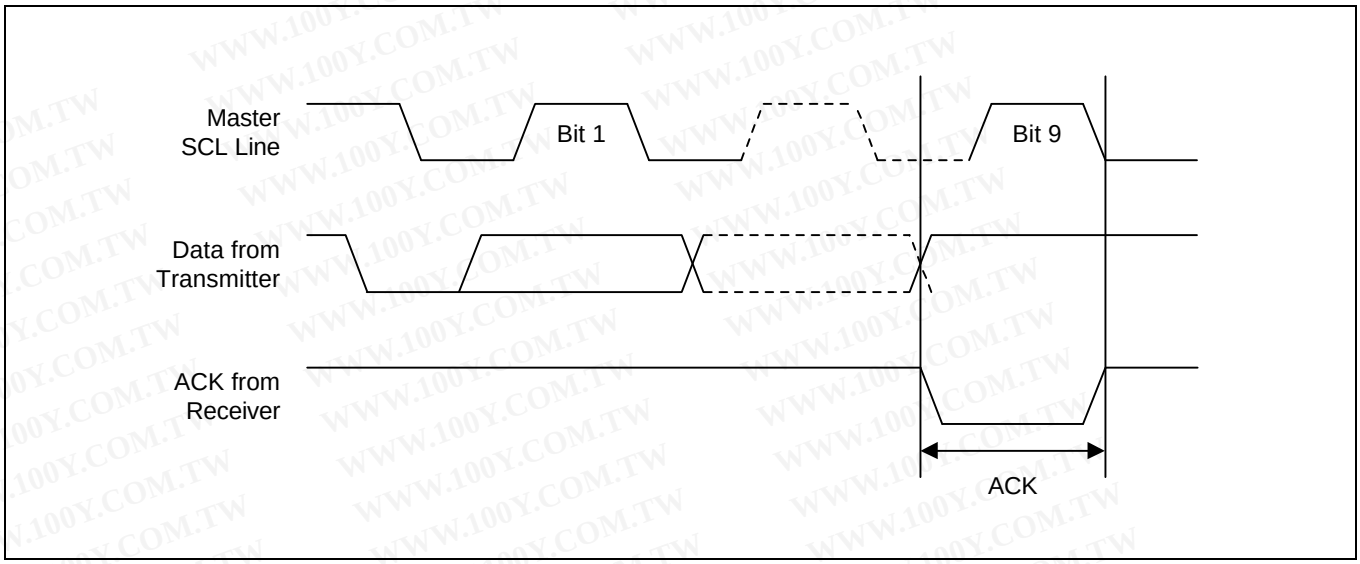
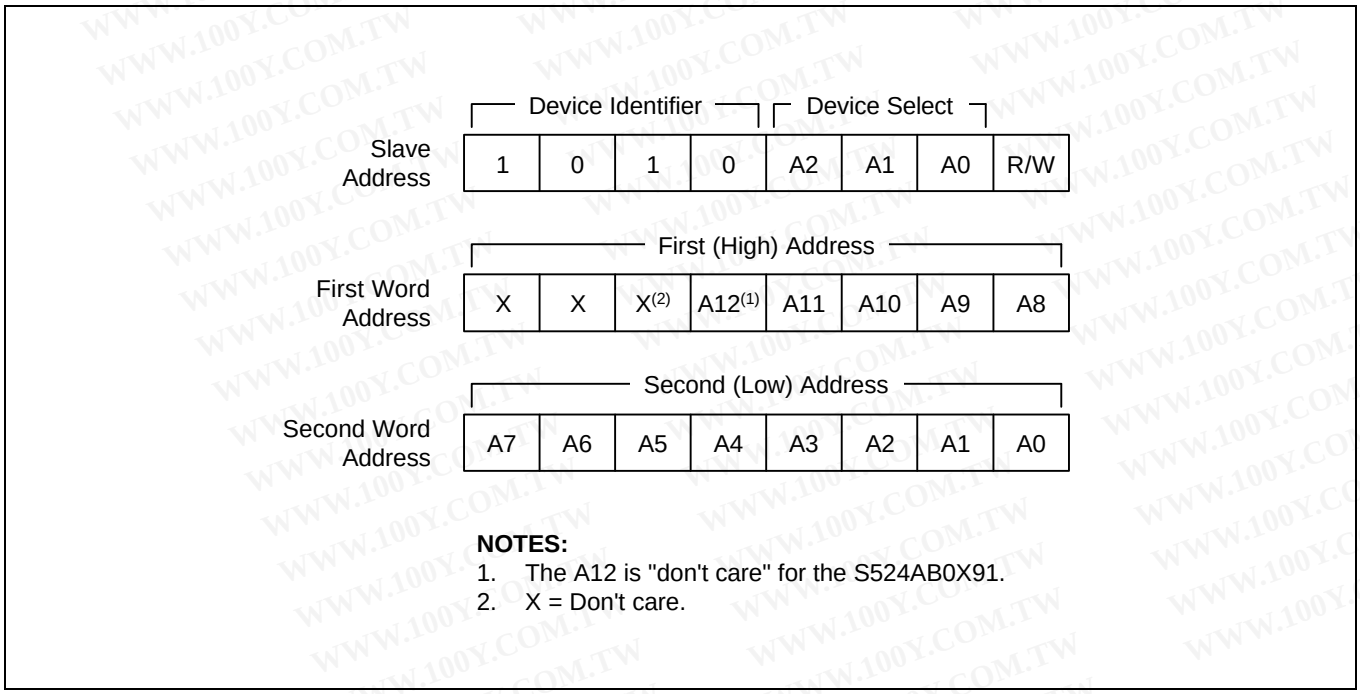


Figure 4-8. Acknowledge Response From Receiver

- Slave Address: After the master initiates a start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the “device identifier.” The identifier for the S524AB0X91/B0XB1 is “1010B”. The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1, and A2 pins. Using this addressing scheme, you can cascade up to eight S524AB0X91/B0XB1s on the bus (see Figure 4-9 below).
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is “1”, a read operation is executed. If it is “0”, a write operation is executed.



NOTES:
1. The A12 is "don't care" for the S524AB0X91.
2. X = Don't care.

Figure 4-9. Device Address

BYTE WRITE OPERATION

A write operation requires 2-byte word addresses, the first (high) word address and the second (low) word address. In a byte write operation, the master transmits the slave address, the first word address, the second word address, and one data byte to the S524AB0X91/B0XB1 slave device (see Figure 4-10).

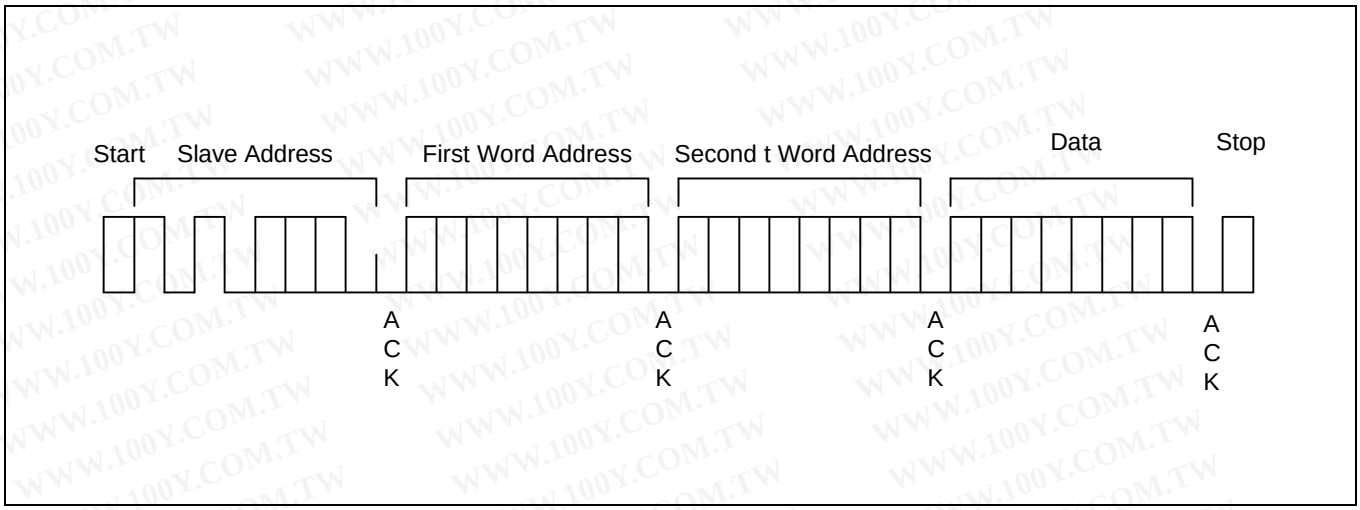


Figure 4-10. Byte Write Operation

Following a start condition, the master puts the device identifier (4 bits), the device address (3 bits), and an R/W bit set to “0” onto the bus. Upon the receipt of the slave address, the S524AB0X91/B0XB1 responds with an ACK. And the master transmits the first word address, the second word address, and one byte data to be written into the addressed memory location.

The master terminates the transfer by generating a stop condition, at which time the S524AB0X91/B0XB1 begins the internal write cycle. While the internal write cycle is in progress, all S524AB0X91/B0XB1 inputs are disabled and the S524AB0X91/B0XB1 does not respond to any additional request from the master.

PAGE WRITE OPERATION

The S524AB0X91/B0XB1 can also perform 32-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 31 additional bytes. The S524AB0X91/B0XB1 responds with an ACK each time it receives a complete byte of data (see Figure 4-11).

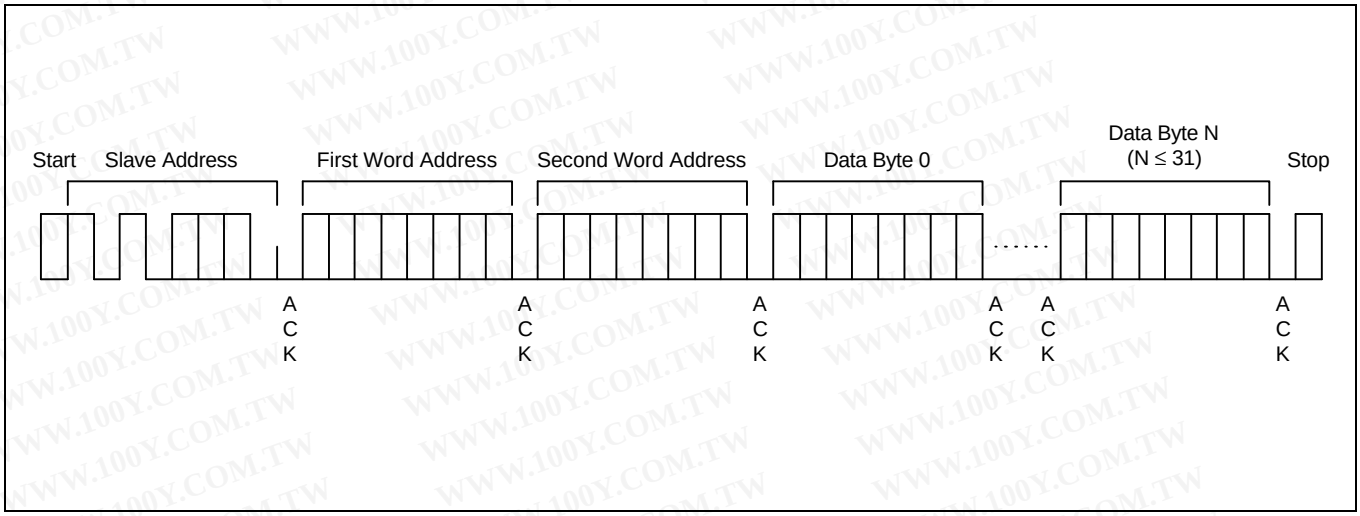


Figure 4-11. Page Write Operation

The S524AB0X91/B0XB1 automatically increments the word address pointer each time it receives a complete data byte. When one byte is received, the internal word address pointer increments to the next address so that the next data byte can be received.

If the master transmits more than 32 bytes before it generates a stop condition to end the page write operation, the S524AB0X91/B0XB1 word address pointer value “rolls over” and the previously received data is overwritten. If the master transmits less than 32 bytes and generates a stop condition, the S524AB0X91/B0XB1 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there would be no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524AB0X91/B0XB1 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device to determine whether the write cycle is completed.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524AB0X91/B0XB1 remains busy with the write operation, no ACK is returned. When the S524AB0X91/B0XB1 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 4-12).

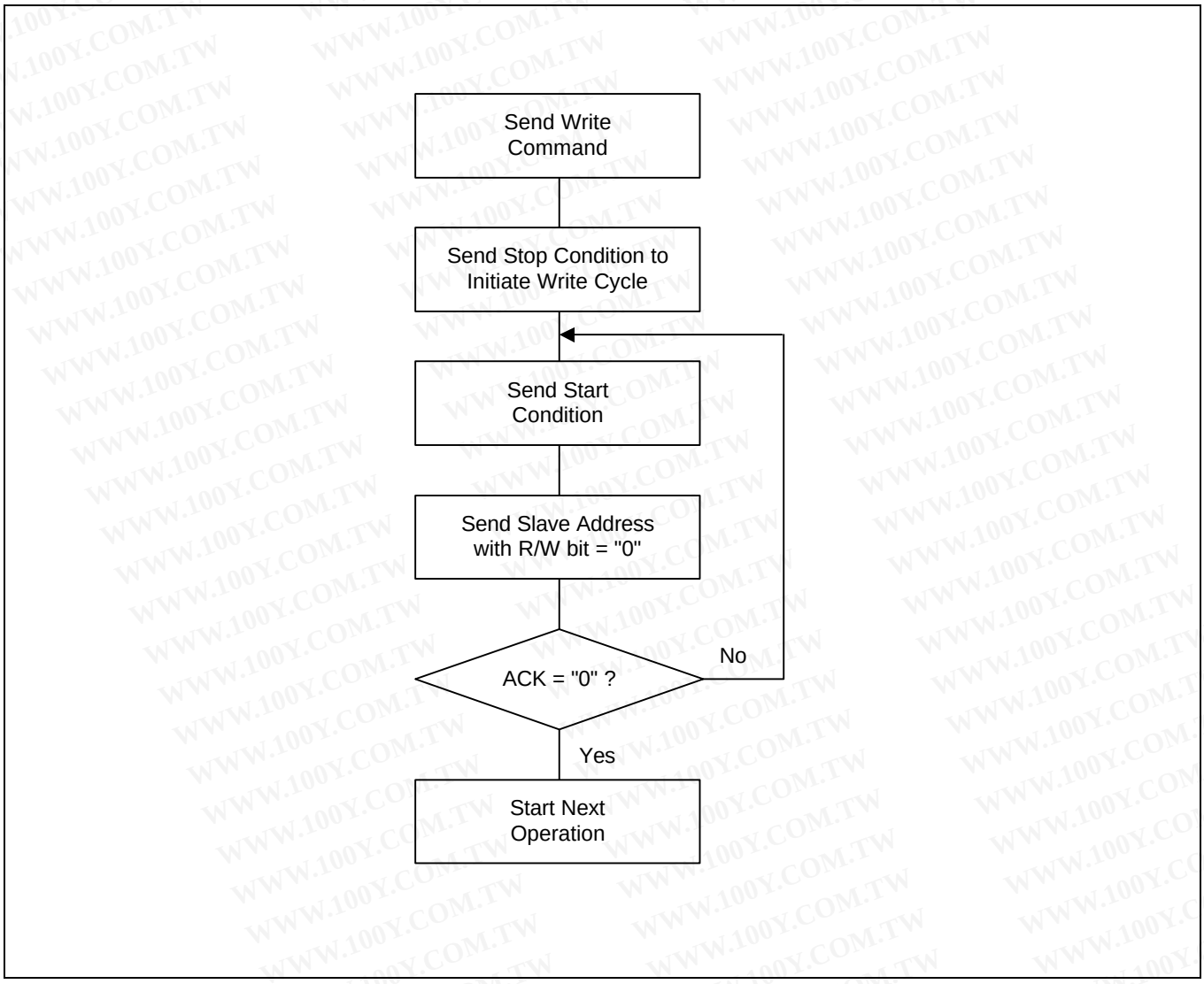


Figure 4-12. Master Polling for an ACK Signal from a Slave Device

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524AB0X91/B0XB1. This write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to it is ignored. The S524AB0X91/B0XB1 will acknowledge slave and word addresses, but it will not generate an acknowledge after receiving the first byte of data. In this situation, the write cycle will not be started when a stop condition is generated. By connecting the WP pin to V_{SS}, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to protect data from being overwritten. Whenever the write function is disabled, a slave address and word addresses are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address “n”, the next read operation would be to access data at address “n+1”.

When the S524AB0X91/B0XB1 receives a slave address with the R/W bit set to “1”, it issues an ACK and sends the eight bits of data. In a current address byte read operation, the master does not acknowledge the data, and it generates a stop condition, forcing the S524AB0X91/B0XB1 to stop the transmission (see Figure 4-13).

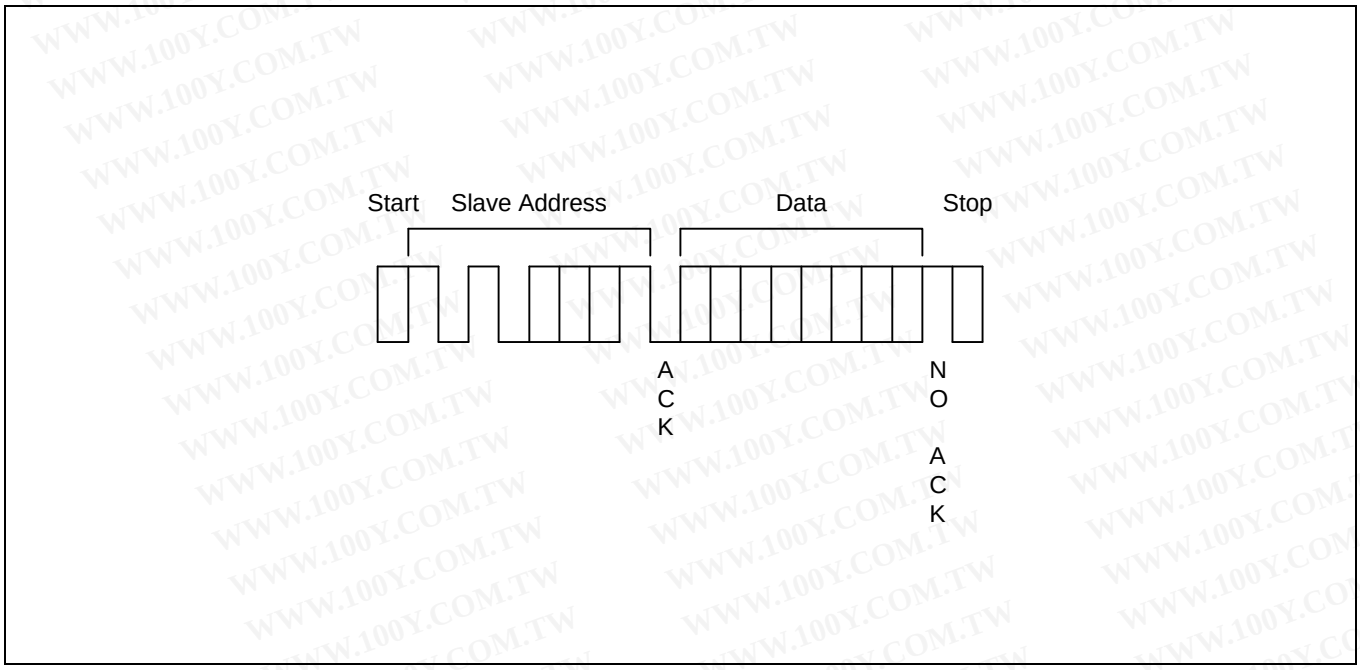


Figure 4-13. Current Address Byte Read Operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. This operation is performed in the following steps:

1. The master first issues a start condition, the slave address, and the word address (the first and the second addresses) to be read. (This step sets the internal word address pointer of the S524AB0X91/B0XB1 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to “1”.
3. The S524AB0X91/B0XB1 then sends an ACK and the 8-bit data stored at the pointed address.
4. At this point, the master does not acknowledge the transmission, generating a stop condition.
5. The S524AB0X91/B0XB1 stops transmitting data and reverts to stand-by mode (see Figure 4-14).

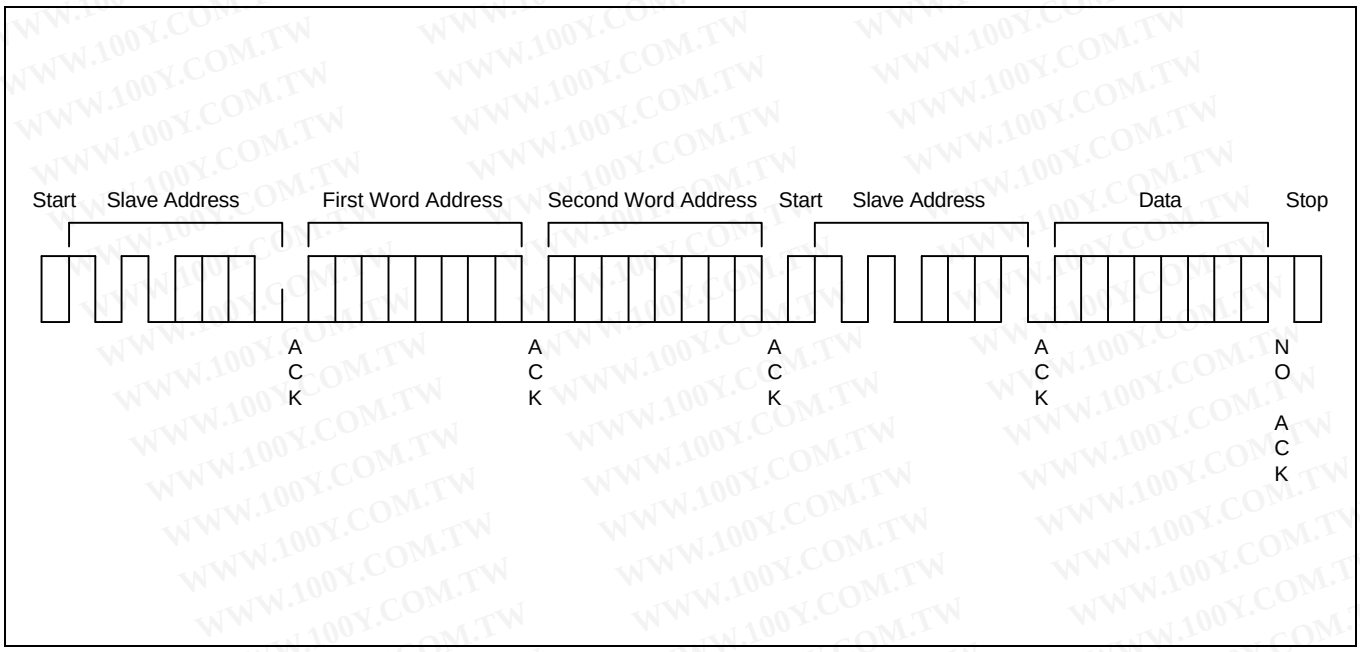


Figure 4-14. Random Address Byte Read Operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: current address sequential read operation, and random address sequential read operation. The first data is sent in either of the two ways, current address byte read operation or random address byte read operation described earlier. If the master responds with an ACK, the S524AB0X91/B0XB1 continues transmitting data. If the master does not issue an ACK, generating a stop condition, the slave stops transmission, ending the sequential read operation.

Using this method, data is output sequentially from address “n” followed by address “n+1”. The word address pointer for read operations increments to all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer “rolls over” and the S524AB0X91/B0XB1 continues to transmit data for each ACK it receives from the master (see Figure 4-15).

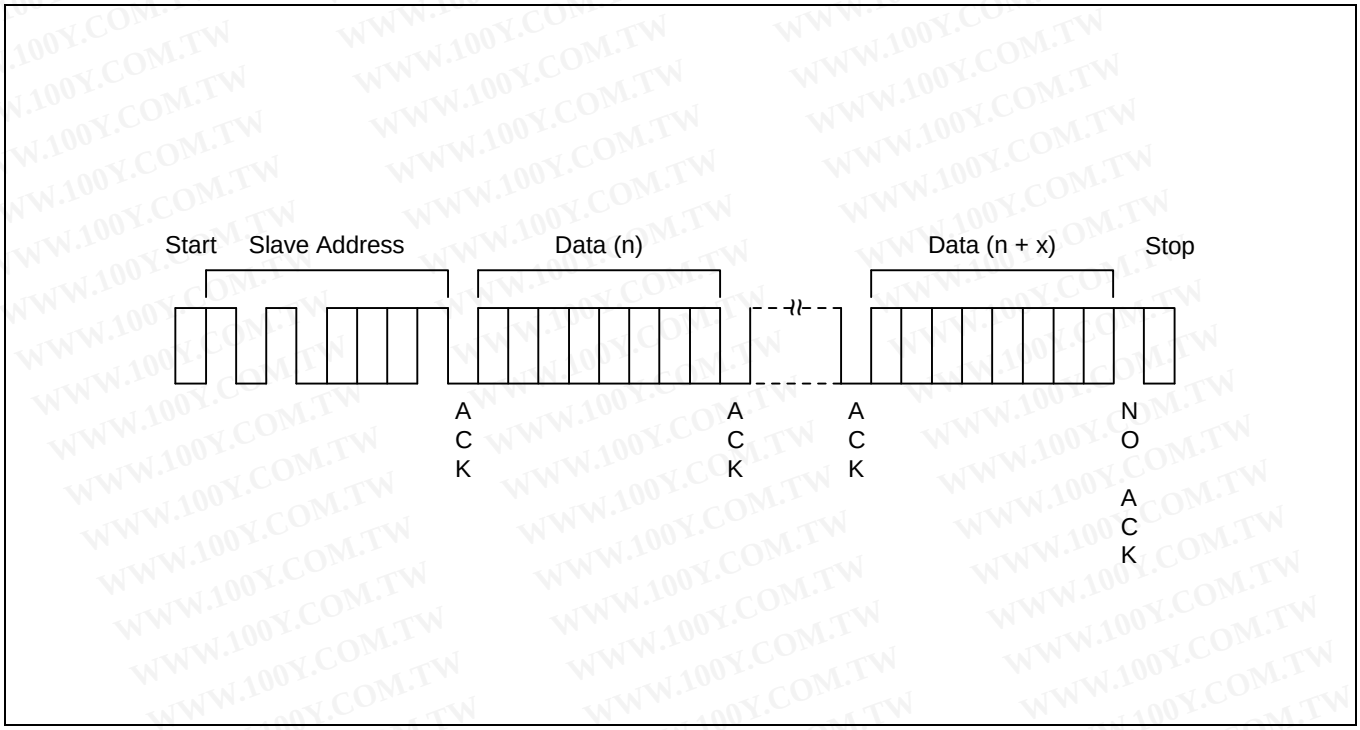


Figure 4-15. Sequential Read Operation

ELECTRICAL DATA

Table 4-2. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to + 7.0	V
Output voltage	V_O	–	– 0.3 to + 7.0	V
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	HBM	5000	V
		MM	500	

Table 4-3. D.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (Commercial), – 40°C to + 85°C (Industrial), V_{CC} = 1.8 V to 5.5 V)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage		V_{IL}	SCL, SDA, A0, A1, A2	–	–	0.3 V_{CC}	V
Input high voltage		V_{IH}		0.7 V_{CC}	–	–	V
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Output leakage current		I_{LO}	V_O = 0 to V_{CC}	–	–	10	µA
Output low voltage		V_{OL}	I_{OL} = 0.15 mA, V_{CC} = 1.8 V	–	–	0.2	V
			I_{OL} = 2.1 mA, V_{CC} = 2.5 V	–	–	0.4	
Supply current	Write	I_{CC1}	V_{CC} = 5.5 V, 400 kHz	–	–	3	mA
		I_{CC2}	V_{CC} = 1.8 V, 100 kHz	–	–	1	
	Read	I_{CC3}	V_{CC} = 5.5 V, 400 kHz	–	–	0.4	
		I_{CC4}	V_{CC} = 1.8 V, 100 kHz	–	–	60	µA
Stand-by current		I_{CC5}	V_{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	–	–	5	µA
		I_{CC6}	V_{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	–	–	1	

Table 4-3. D.C. Electrical Characteristics (Continued)

(T_A = – 25°C to + 70°C (Commercial), – 40°C to + 85°C (Industrial), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	25°C, 1MHz, V_{CC} = 5 V, V_{IN} = 0 V, A0, A1, A2, SCL and WP pin	–	–	10	pF
Input/Output capacitance	$C_{I/O}$	25°C, 1MHz, V_{CC} = 5 V, $V_{I/O}$ = 0 V, SDA pin	–	–	10	

Table 4-4. A.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (Commercial), – 40°C to + 85°C (Industrial), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	V_{CC} = 1.8 to 5.5 V (Standard Mode)		V_{CC} = 2.5 to 5.5 V (Fast Mode)		Unit
			Min	Max	Min	Max	
External clock frequency	F_{clk}	–	0	100 (1)	0	400 (1)	kHz
Clock High time	t_{HIGH}	–	4	–	0.6	–	µs
Clock Low time	t_{LOW}	–	4.7	–	1.3	–	µs
Rising time	t_R	SDA, SCL	–	1	–	0.3	µs
Falling time	t_F	SDA, SCL	–	0.3	–	0.3	µs
Start condition hold time	$t_{HD:STA}$	–	4	–	0.6	–	µs
Start condition setup time	$t_{SU:STA}$	–	4.7	–	0.6	–	µs
Data input hold time	$t_{HD:DAT}$	–	0	–	0	–	µs
Data input setup time	$t_{SU:DAT}$	–	0.25	–	0.1	–	µs
Stop condition setup time	$t_{SU:STO}$	–	4	–	0.6	–	µs
Bus free time	t_{BUF}	Before new transmission	4.7	–	1.3	–	µs
Data output valid from clock low (2)	t_{AA}	–	0.3	3.5	–	0.9	µs
Noise spike width	t_{SP}	–	–	100	–	50	ns
Write cycle time	t_{WR}	–	–	5	–	5	ms

NOTES:

1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
2. When acting as a transmitter, the S524AB0X91/B0XB1 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

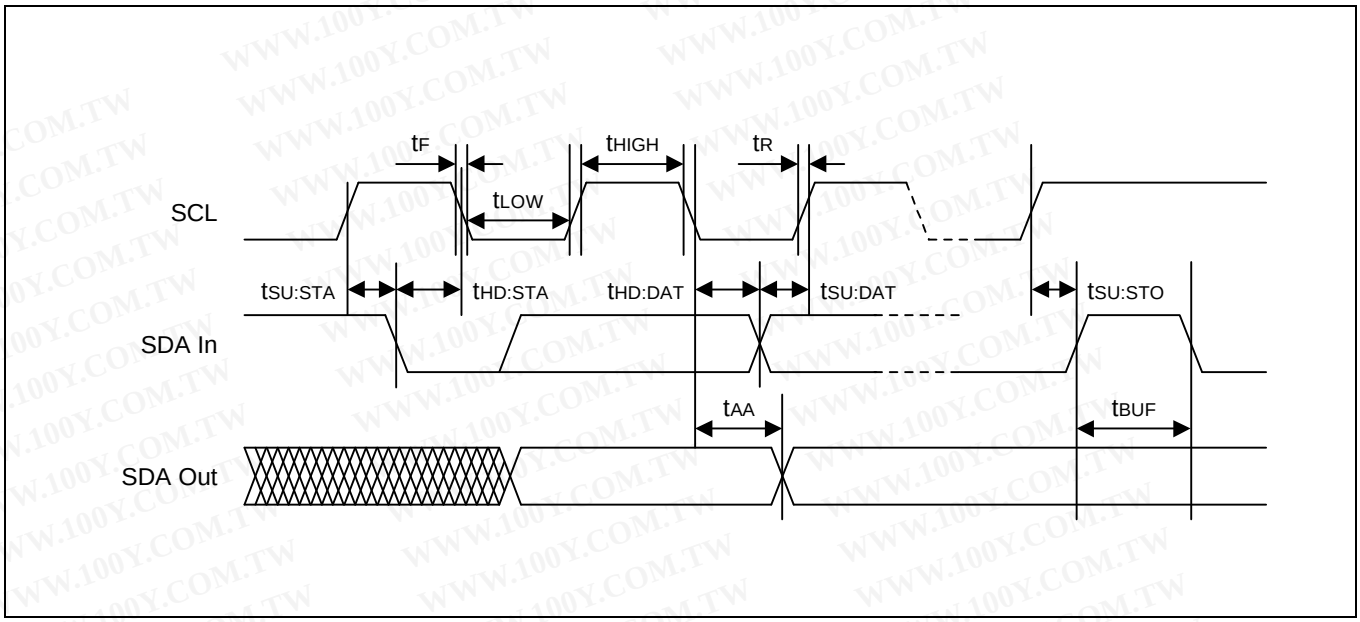


Figure 4-16. Timing Diagram for Bus Operations

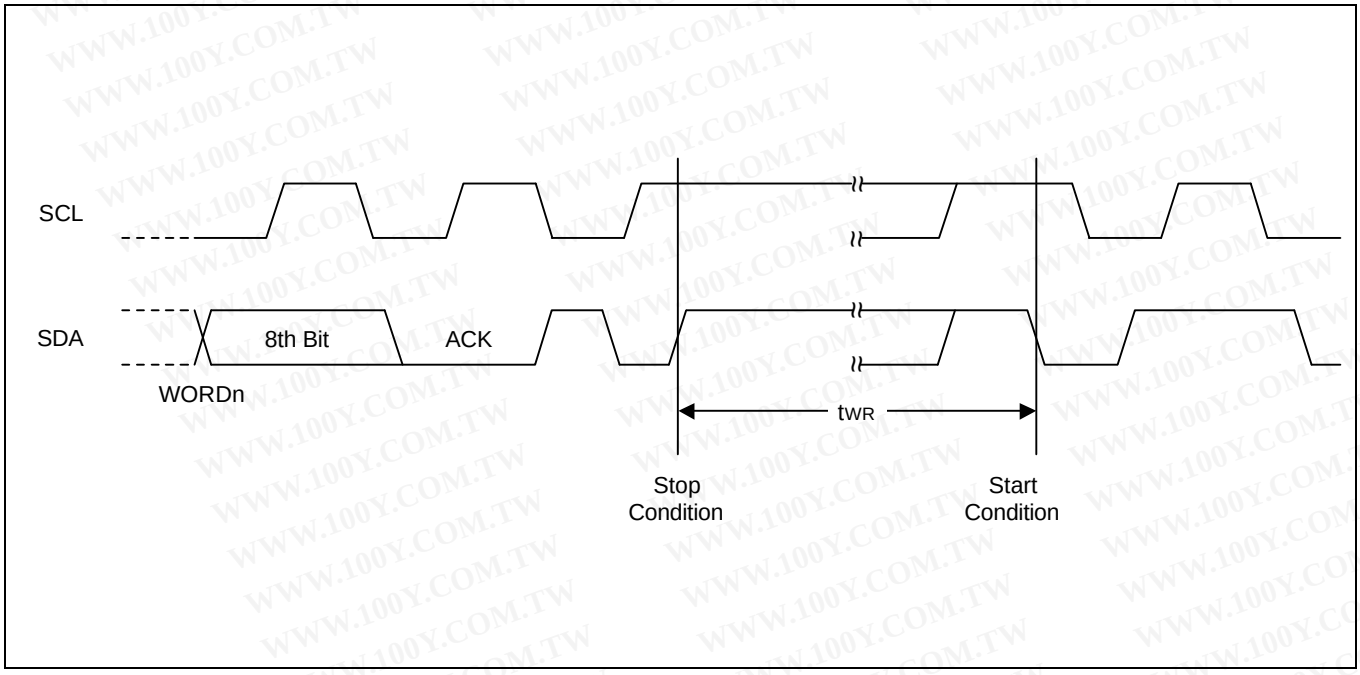


Figure 4-17. Write Cycle Timing Diagram

SAMSUNG ELECTRONICS

S524AD0XD1/D0XF1

128K/256K-bit Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The S524AD0XD1/D0XF1 serial EEPROM has a 128K/256K-bit (16,384/32,768 bytes) capacity, supporting the standard I²C™-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 64 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524AD0XD1/D0XF1 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 128K/256K-bit (16,384/32,768 bytes) storage area
- 64-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 500,000 erase/write cycles
- 50 years data retention

Operating Characteristics

- Operating voltage
  - 1.8 V to 5.5 V
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 400 µA at 5.5 V
  - Maximum stand-by current: < 5 µA at 5.5 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 400 kHz at standard mode
  - 1 MHz at fast mode
- Electrostatic discharge (ESD)
  - 5,000 V (HBM)
  - 500 V (MM)

Packages

- 8-pin DIP, and TSSOP

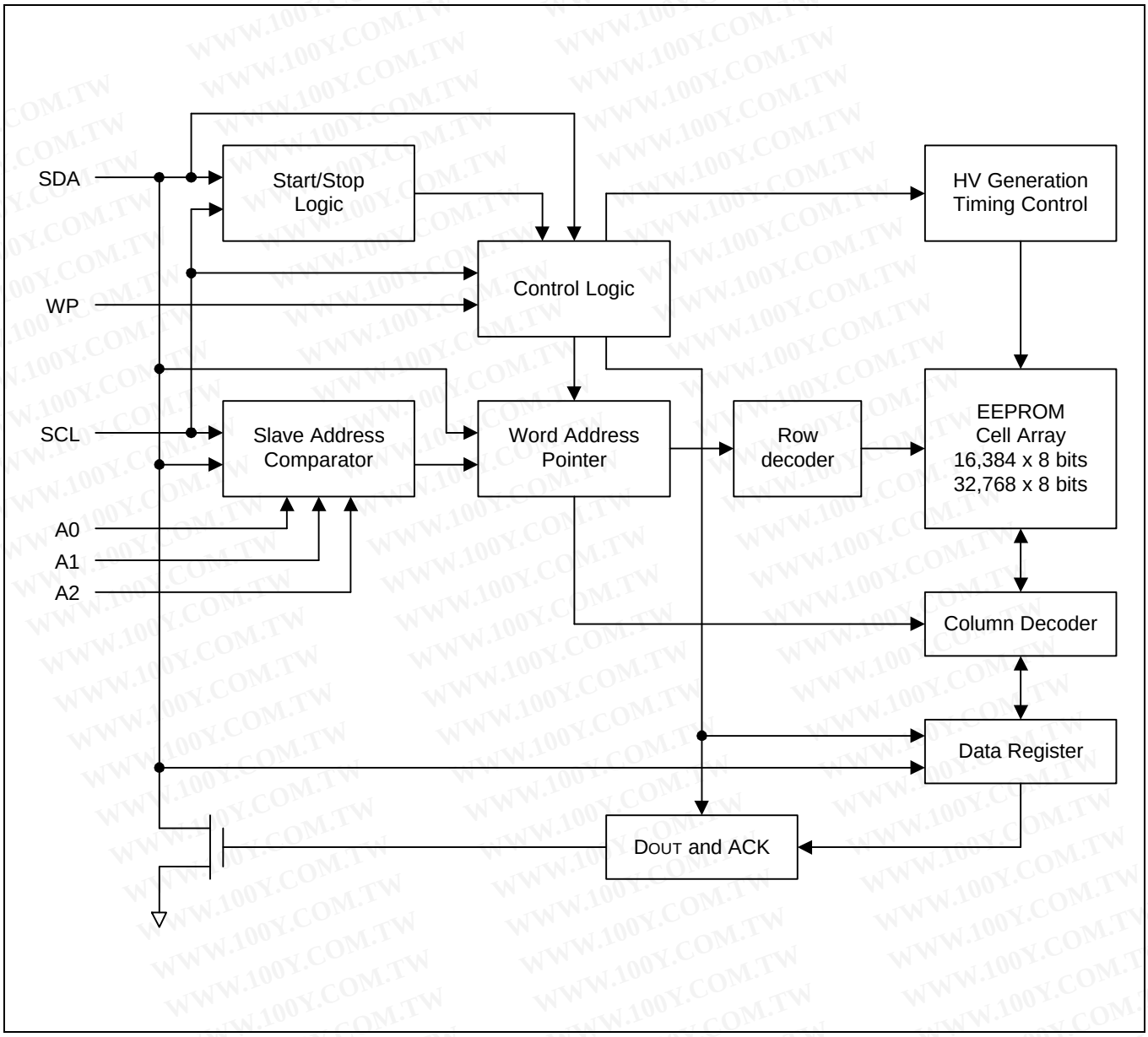
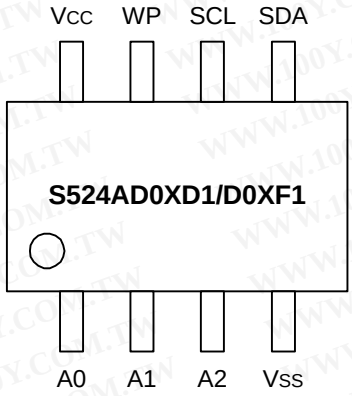


Figure 5-1. S524AD0XD1/D0XF1 Block Diagram



NOTE: The S524AD0XD1/D0XF1 is available in 8-pin DIP, and TSSOP package.

Figure 5-2. Pin Assignment Diagram

Table 5-1. S524AD0XD1/D0XF1 Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS}.	1
V_{SS}	–	Ground pin.	–
SDA	I/O	Bi-directional data pin for the I^2C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to V_{DD}. Typical values for this pull-up resistor are 4.7 KΩ (100 KHz) and 1 KΩ (400 KHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to V_{CC}, the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS}, the write function is enabled. This pin is internally pulled down to V_{SS}.	1
V_{CC}	–	Single power supply.	–

NOTE: See the following page for diagrams of pin circuit types 1, 2, and 3.

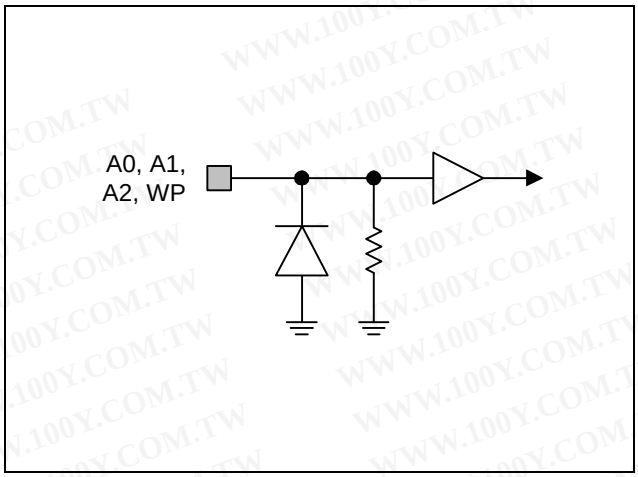


Figure 5-3. Pin Circuit Type 1

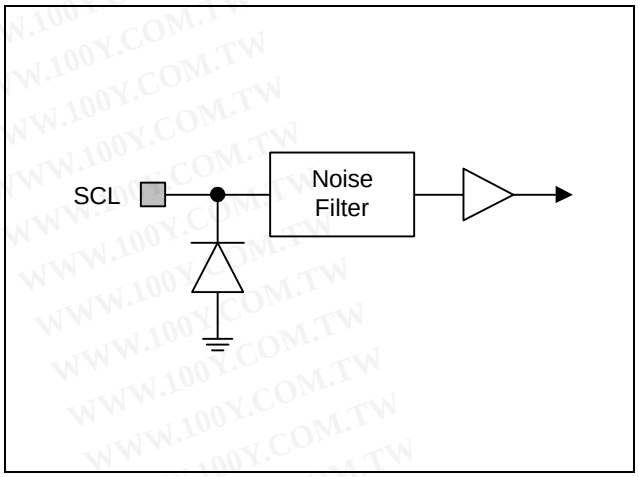


Figure 5-4. Pin Circuit Type 2

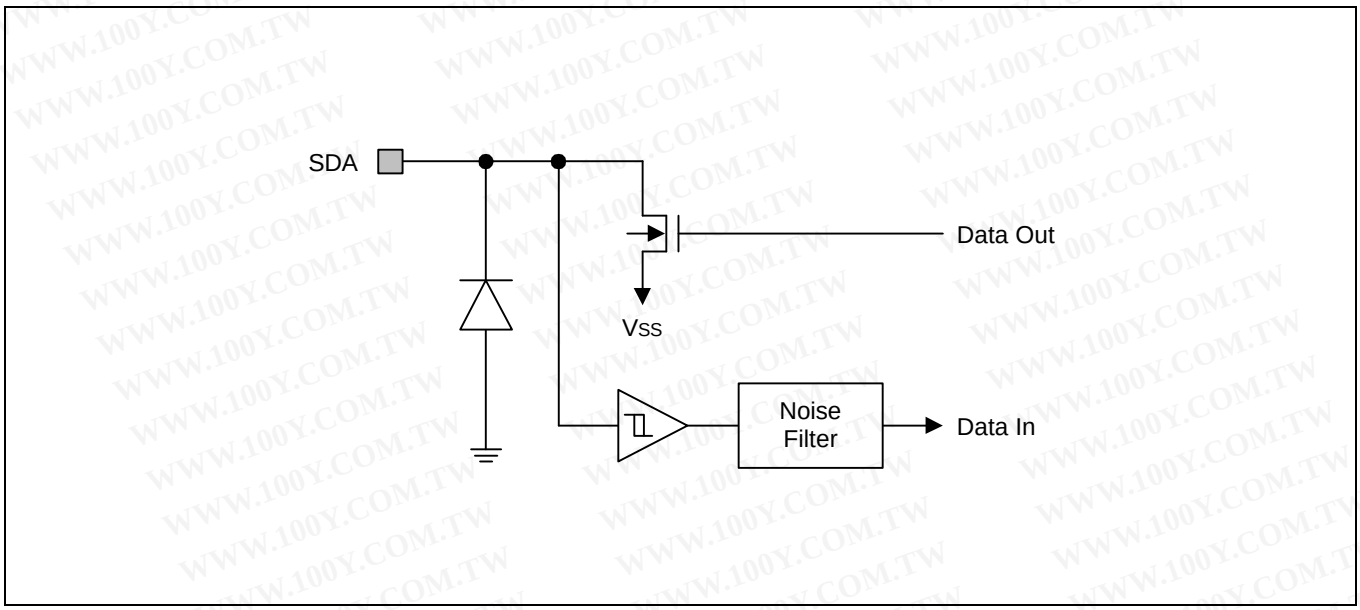


Figure 5-5. Pin Circuit Type 3

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The S524AD0XD1/D0XF1 supports the I²C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as a “transmitter” and any device that gets data from the bus is a “receiver.” The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight S524AD0XD1/D0XF1 devices can be connected to the same I²C-bus as slaves (see Figure 5-6). Both the master and slaves can operate as a transmitter or a receiver, but the master device determines which bus operating mode would be active.

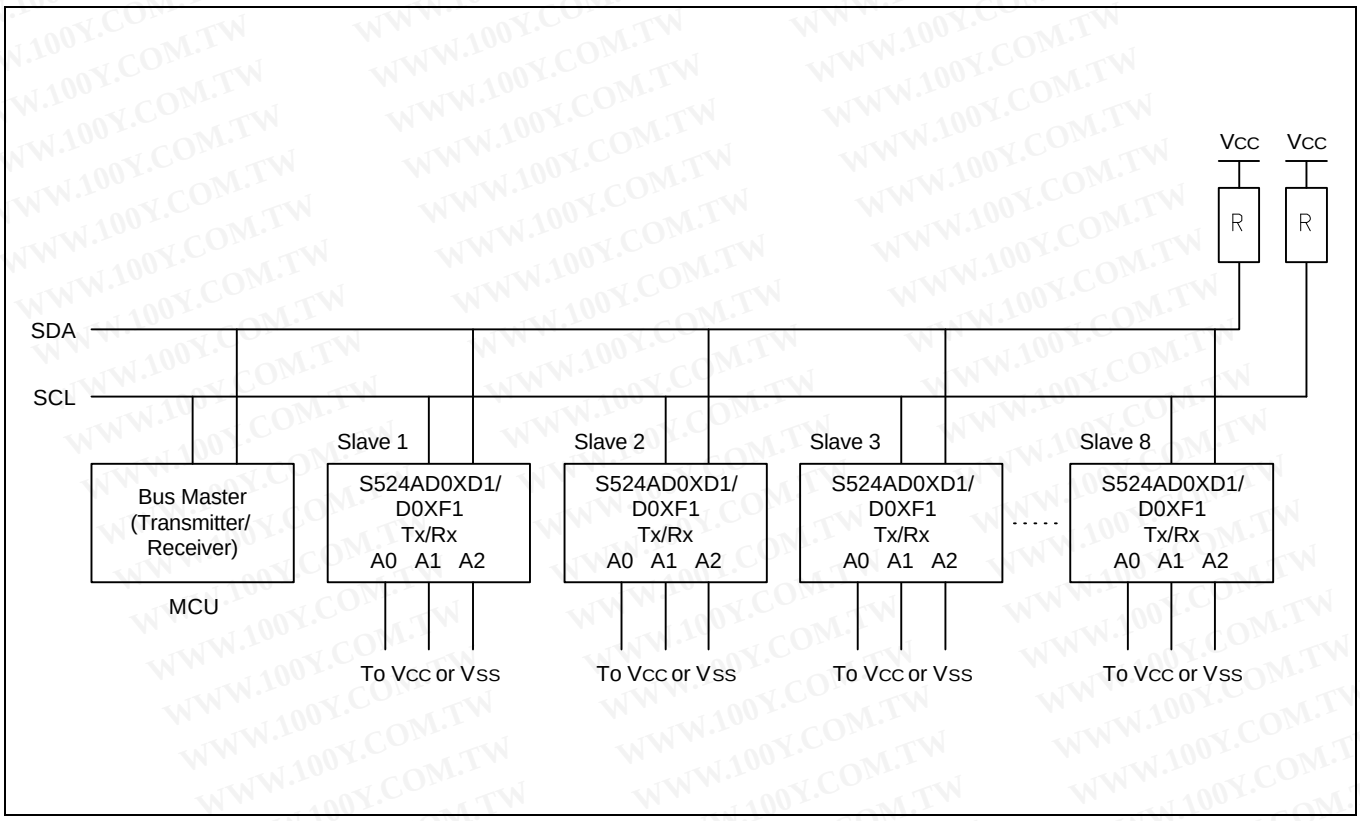


Figure 5-6. Typical Configuration

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

— A new data transfer can be initiated only when the bus is currently not busy.

— MSB is always transferred first in transmitting data.

— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain in High level when the bus is not active.
- Start condition: A start condition is initiated by a High-to-Low transition of the SDA line while SCL remains in High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains in High level. All bus operations must be completed by a stop condition (see Figure 5-7).

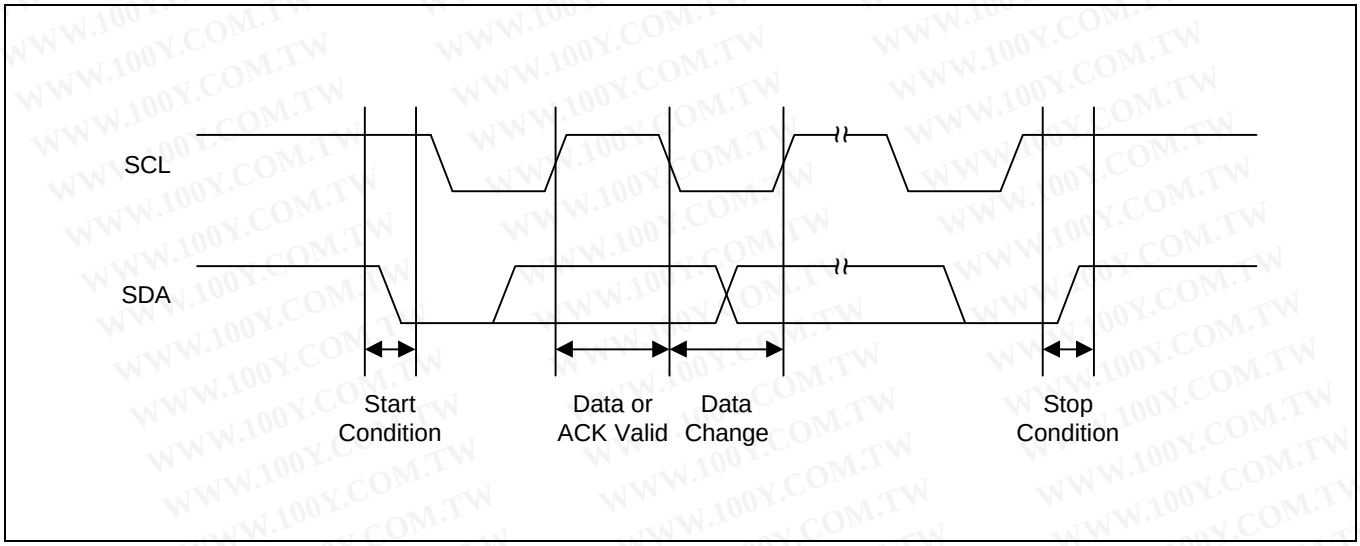


Figure 5-7. Data Transmission Sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.
- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it has successfully received the eight bits of data (see Figure 5-8). But the slave does not send an ACK if an internal write cycle is still in progress.

  In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected but no stop condition, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

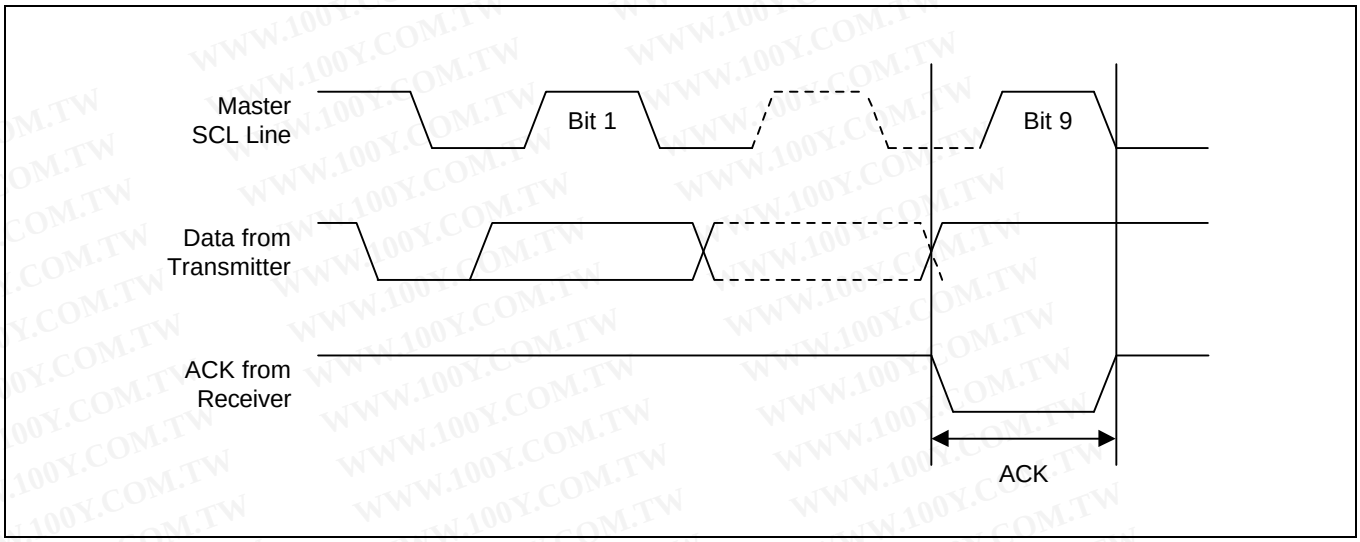
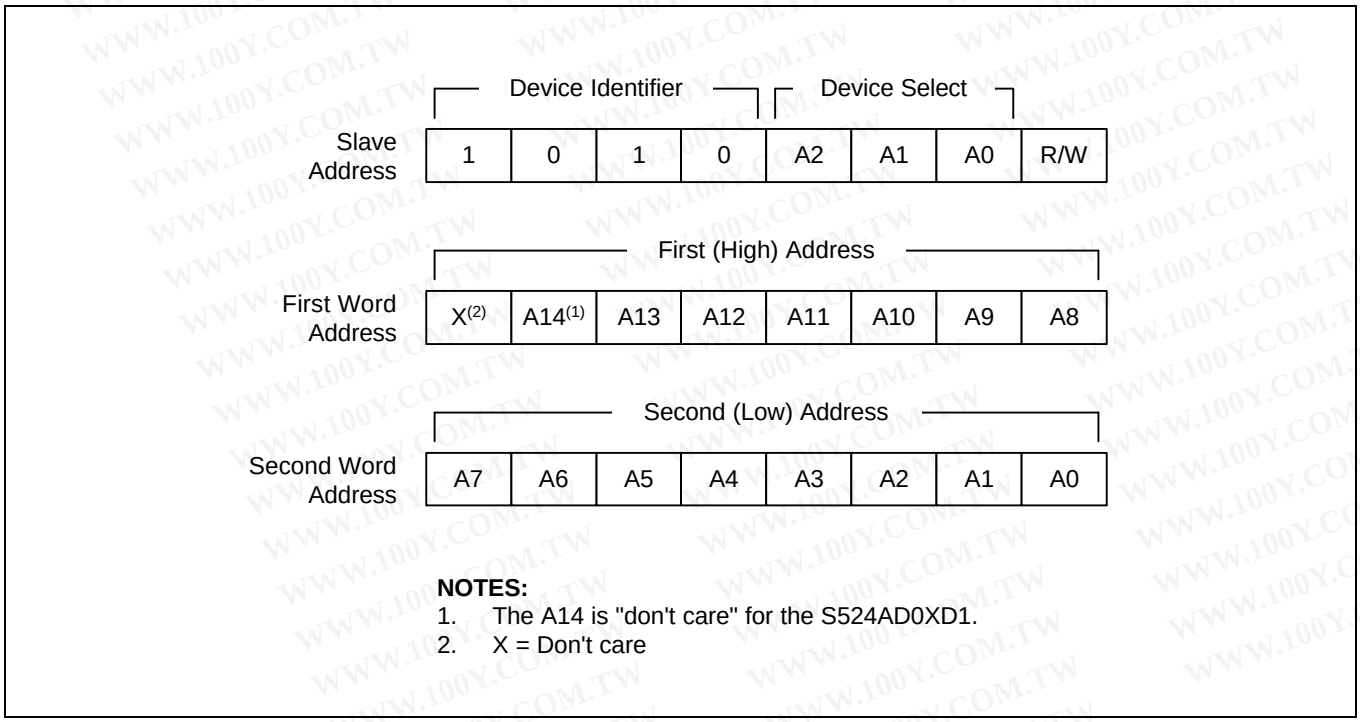


Figure 5-8. Acknowledge Response from Receiver

- Slave Address: After the master initiates a start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the “device identifier.” The identifier for the S524AD0XD1/D0XF1 is “1010B”. The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1, and A2 pins. Using this addressing scheme, you can cascade up to eight S524AD0XD1/D0XF1s on the bus (see Figure 5-9 below).
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is “1”, a read operation is executed. If it is “0”, a write operation is executed.



NOTES:
1. The A14 is "don't care" for the S524AD0XD1.
2. X = Don't care

Figure 5-9. Device Address

BYTE WRITE OPERATION

A write operation requires 2-byte word addresses, the first (high) word address and the second (low) word address. In a byte write operation, the master transmits the slave address, the first word address, the second word address, and one data byte to the S524AD0XD1/D0XF1 slave device (see Figure 5-10).

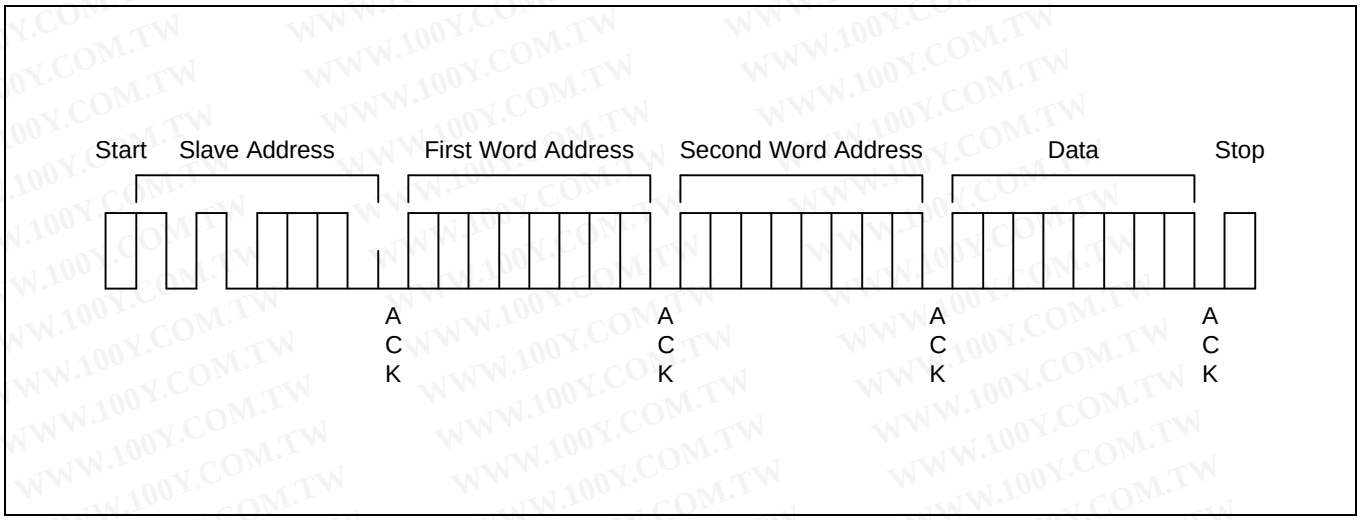


Figure 5-10. Byte Write Operation

Following a start condition, the master puts the device identifier (4 bits), the device address (3 bits), and an R/W bit set to “0” onto the bus. Upon the receipt of the slave address, the S524AD0XD1/D0XF1 responds with an ACK. And the master transmits the first word address, the second word address, and one byte data to be written into the addressed memory location.

The master terminates the transfer by generating a stop condition, at which time the S524AD0XD1/D0XF1 begins the internal write cycle. While the internal write cycle is in progress, all S524AD0XD1/D0XF1 inputs are disabled and the S524AD0XD1/D0XF1 does not respond to any additional request from the master.

PAGE WRITE OPERATION

The S524AD0XD1/D0XF1 can also perform 64-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 63 additional bytes. The S524AD0XD1/D0XF1 responds with an ACK each time it receives a complete byte of data (see Figure 5-11).

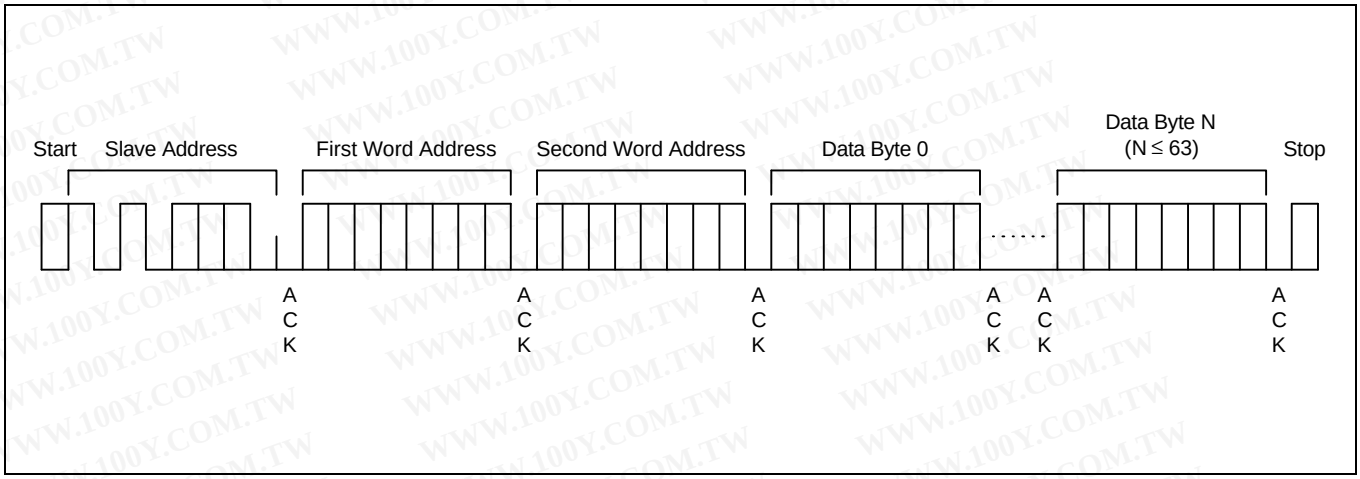


Figure 5-11. Page Write Operation

The S524AD0XD1/D0XF1 automatically increments the word address pointer each time it receives a complete data byte. When one byte is received, the internal word address pointer increments to the next address so that the next data byte can be received.

If the master transmits more than 64 bytes before it generates a stop condition to end the page write operation, the S524AD0XD1/D0XF1 word address pointer value “rolls over” and the previously received data is overwritten. If the master transmits less than 64 bytes and generates a stop condition, the S524AD0XD1/D0XF1 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there would be no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the S524AD0XD1/D0XF1 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device to determine whether the write cycle is completed.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the S524AD0XD1/D0XF1 remains busy with the write operation, no ACK is returned. When the S524AD0XD1/D0XF1 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 5-12).

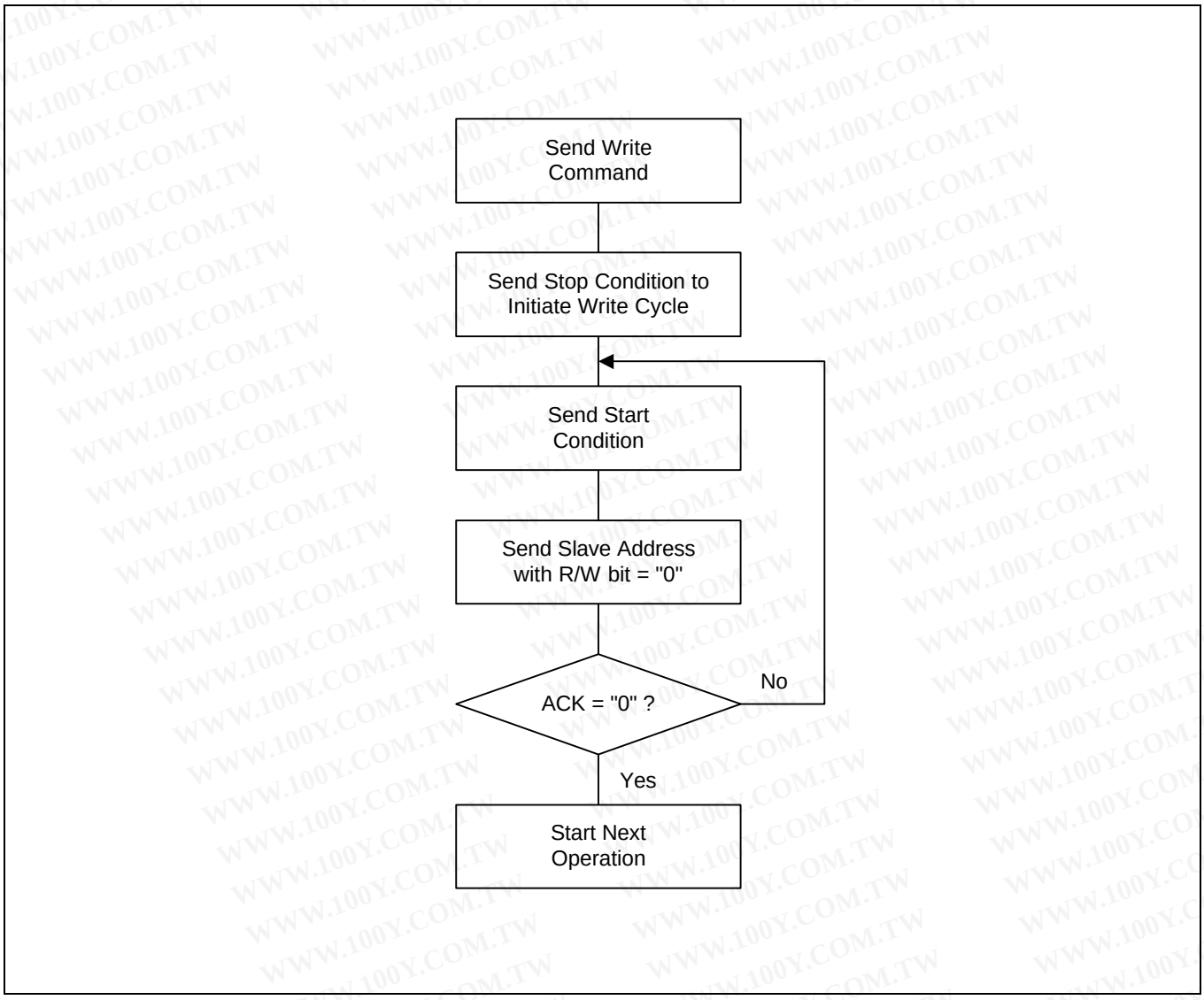


Figure 5-12. Master Polling for an ACK Signal from a Slave Device

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the S524AD0XD1/D0XF1. This write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to it is ignored. The S524AD0XD1/D0XF1 will acknowledge slave address, word address, and data bytes. But the write cycle will not be started when a stop condition is generated. By connecting the WP pin to V_{SS}, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to protect data from being overwritten.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address “n”, the next read operation would be to access data at address “n+1”.

When the S524AD0XD1/D0XF1 receives a slave address with the R/W bit set to “1”, it issues an ACK and sends the eight bits of data. In a current address byte read operation, the master does not acknowledge the data, and it generates a stop condition, forcing the S524AD0XD1/D0XF1 to stop the transmission (see Figure 5-13).

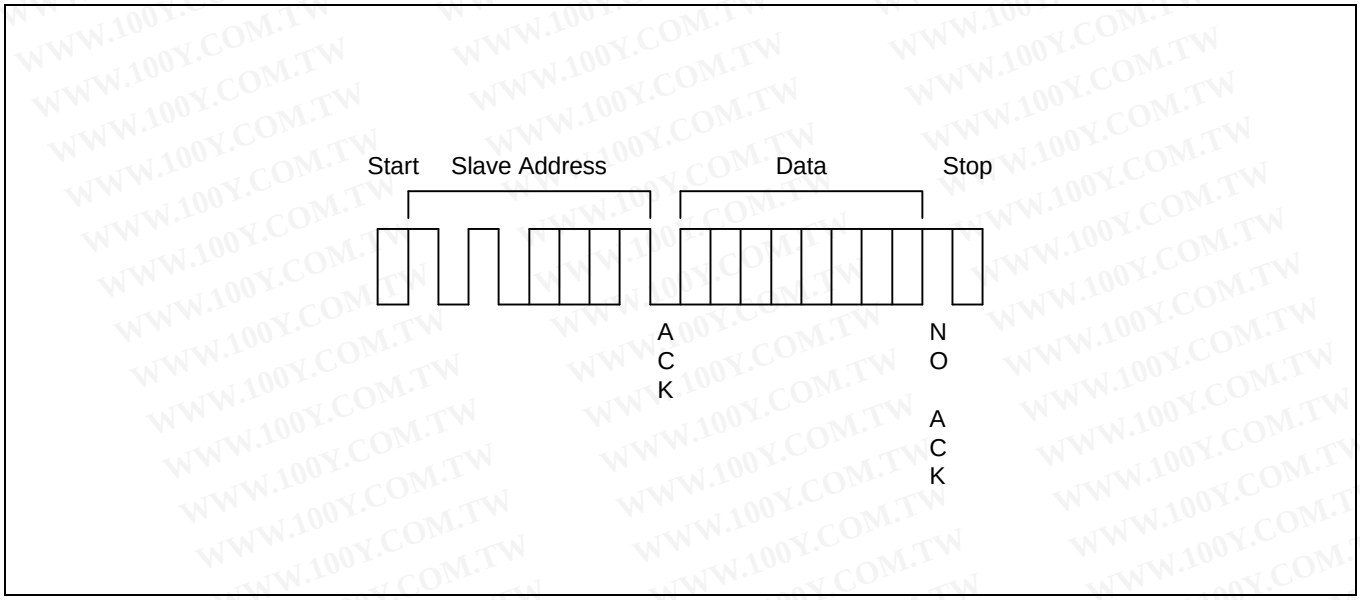


Figure 5-13. Current Address Byte Read Operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. This operation is performed in the following steps:

1. The master first issues a start condition, the slave address, and the word address (the first and the second addresses) to be read. (This step sets the internal word address pointer of the S524AD0XD1/D0XF1 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to “1”.
3. The S524AD0XD1/D0XF1 then sends an ACK and the 8-bit data stored at the pointed address.
4. At this point, the master does not acknowledge the transmission, generating a stop condition.
5. The S524AD0XD1/D0XF1 stops transmitting data and reverts to stand-by mode (see Figure 5-14).

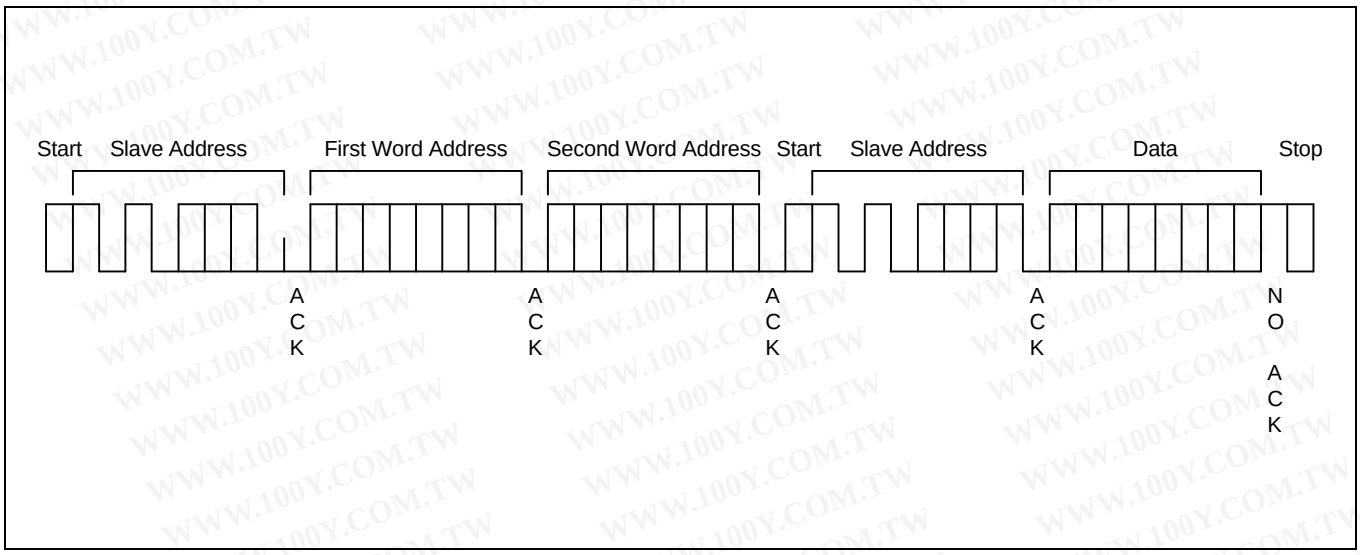


Figure 5-14. Random Address Byte Read Operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: current address sequential read operation, and random address sequential read operation. The first data is sent in either of the two ways, current address byte read operation or random address byte read operation described earlier. If the master responds with an ACK, the S524AD0XD1/D0XF1 continues transmitting data. If the master does not issue an ACK, generating a stop condition, the slave stops transmission, ending the sequential read operation.

Using this method, data is output sequentially from address “n” followed by address “n+1”. The word address pointer for read operations increments to all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer “rolls over” and the S524AD0XD1/D0XF1 continues to transmit data for each ACK it receives from the master (see Figure 5-15).

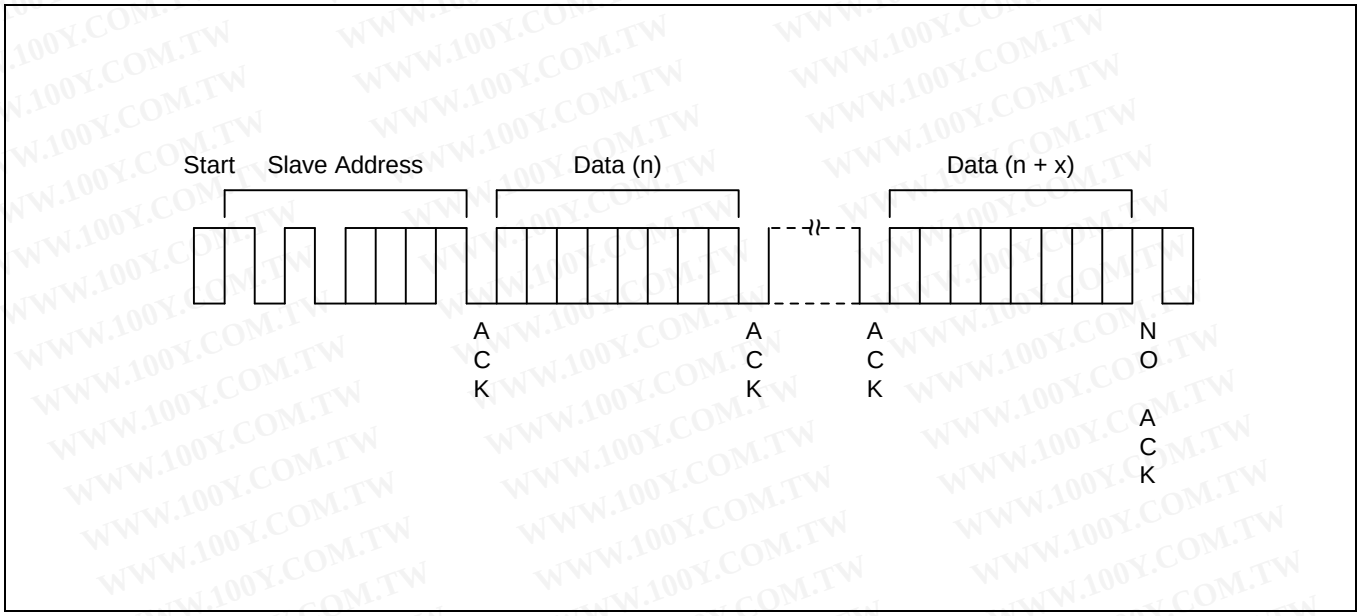


Figure 5-15. Sequential Read Operation

ELECTRICAL DATA

Table 5-2. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to + 7.0	V
Output voltage	V_O	–	– 0.3 to + 7.0	V
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	HBM	5000	V
		MM	500	

Table 5-3. D.C. Electrical Characteristics

(T_A = – 25 °C to + 70 °C (Commercial), – 40 °C to + 85 °C (Industrial), V_{CC} = 1.8 V to 5.5 V)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage		V_{IL}	SCL, SDA, A0, A1, A2	–	–	0.3 V_{CC}	V
Input high voltage		V_{IH}		0.7 V_{CC}	–	–	V
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Output leakage current		I_{LO}	V_O = 0 to V_{CC}	–	–	10	µA
Output Low voltage		V_{OL}	I_{OL} = 0.15 mA, V_{CC} = 1.8 V	–	–	0.2	V
			I_{OL} = 2.1 mA, V_{CC} = 2.5 V			0.4	
Supply current	Write	I_{CC1}	V_{CC} = 5.5 V, 400 kHz	–	–	3	mA
		I_{CC2}	V_{CC} = 1.8 V, 100 kHz	–	–	1	
	Read	I_{CC3}	V_{CC} = 5.5 V, 400 kHz	–	–	0.4	
		I_{CC4}	V_{CC} = 1.8 V, 100 kHz	–	–	60	µA
Stand-by current		I_{CC5}	V_{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	–	–	5	µA
		I_{CC6}	V_{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	–	–	1	

Table 5-3. D.C. Electrical Characteristics (Continued)

(T_A = – 25 °C to + 70 °C (Commercial), – 40 °C to + 85 °C (Industrial), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	25 °C, 1MHz, V_{CC} = 5 V, V_{IN} = 0 V, A0, A1, A2, SCL and WP pin	–	–	10	pF
Input/Output capacitance	$C_{I/O}$	25 °C, 1MHz, V_{CC} = 5 V, $V_{I/O}$ = 0 V, SDA pin	–	–	10	

Table 5-4. A.C. Electrical Characteristics

(T_A = – 25 °C to + 70 °C (Commercial), – 40 °C to + 85 °C (Industrial), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	V_{CC} = 1.8 to 5.5 V (Standard Mode)		V_{CC} = 2.5 to 5.5 V (Fast Mode)		Unit
			Min	Max	Min	Max	
External clock frequency	F_{clk}	–	0	400	0	1000	kHz
Clock High time	t_{HIGH}	–	0.6	–	0.5	–	µs
Clock Low time	t_{LOW}	–	1.3	–	0.5	–	µs
Rising time	t_R	SDA, SCL	–	0.3	–	0.3	µs
Falling time	t_F	SDA, SCL	–	0.3	–	0.1	µs
Start condition hold time	$t_{HD:STA}$	–	0.6	–	0.25	–	µs
Start condition setup time	$t_{SU:STA}$	–	0.6	–	0.25	–	µs
Data input hold time	$t_{HD:DAT}$	–	0	–	0	–	µs
Data input setup time	$t_{SU:DAT}$	–	0.1	–	0.1	–	µs
WP hold time	$t_{HD:WP}$	–	1.3	–	1.3	–	µs
WP setup time	$t_{SU:WP}$	–	0.6	–	0.6	–	µs
Stop condition setup time	$t_{SU:STO}$	–	0.6	–	0.25	–	µs
Bus free time	t_{BUF}	Before new transmission	1.3	–	0.5	–	µs
Data output valid from clock low	t_{AA}	–	0.1	0.9	0.05	0.55	µs
Noise spike width	t_{SP}	–	–	50	–	50	ns
Write cycle time	t_{WR}	–	–	5	–	5	ms

NOTES:

1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
2. When acting as a transmitter, the S524AD0XD1/D0XF1 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

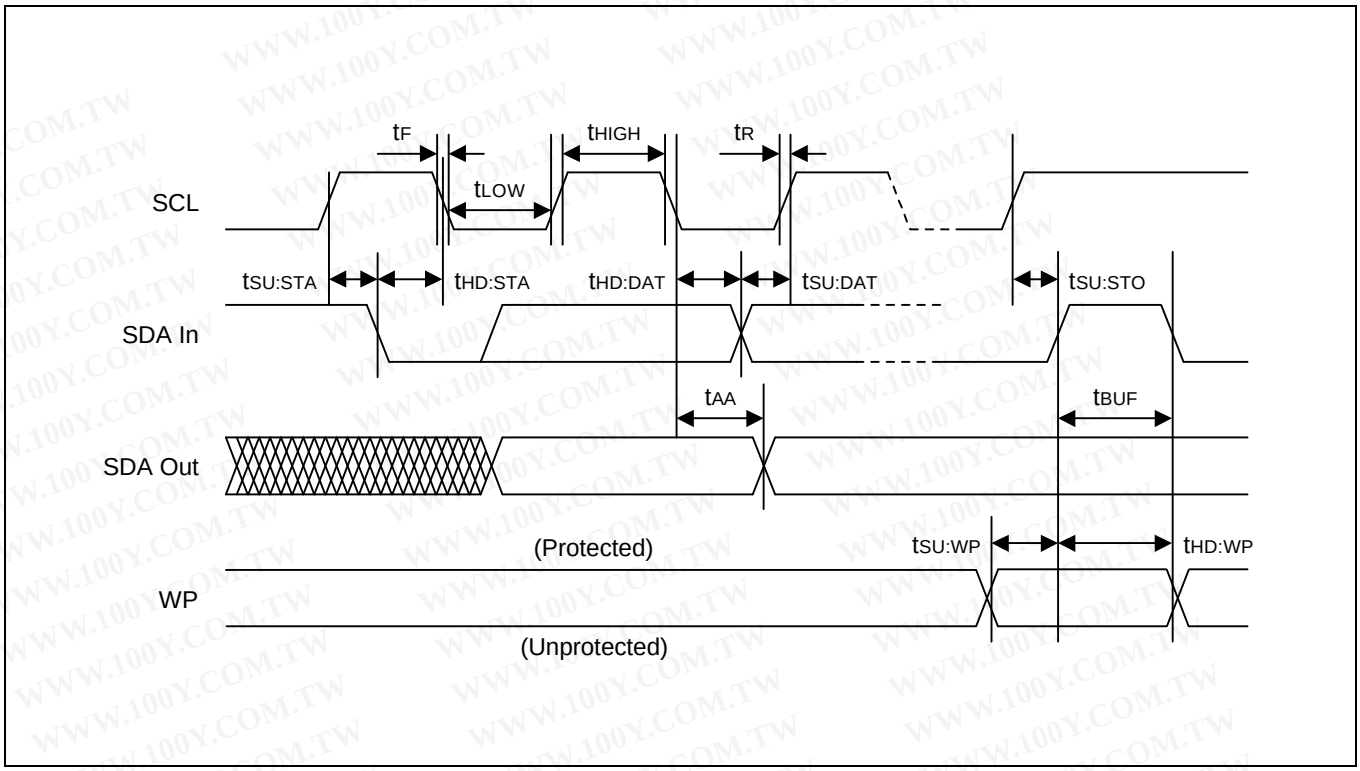


Figure 5-16. Timing Diagram for Bus Operations

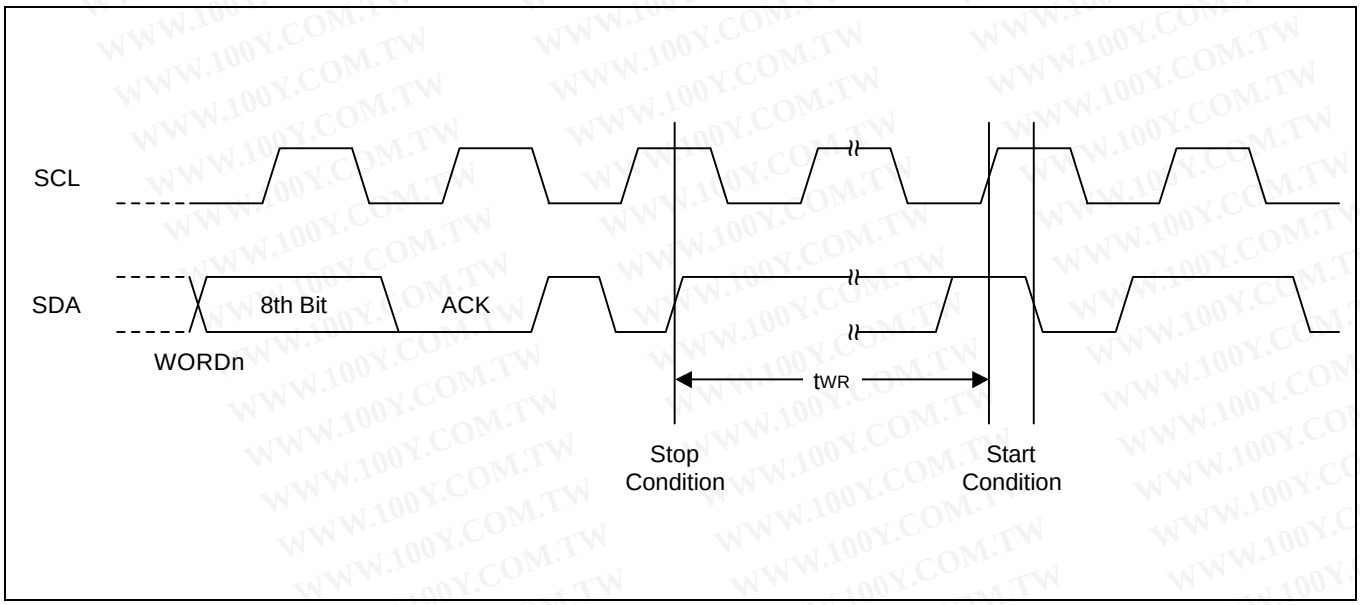


Figure 5-17. Write Cycle Timing Diagram

SAMSUNG ELECTRONICS

S524AE0XH1

512K-bit Serial EEPROM for Low Power

Preliminary

Data Sheet

OVERVIEW

The S524E0XH1 serial EEPROM has a 512K-bit (65,536 bytes) capacity, supporting the standard I²C™-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 128 bytes of data into the EEPROM in a single write operation. Another significant feature of the S524E0XH1 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

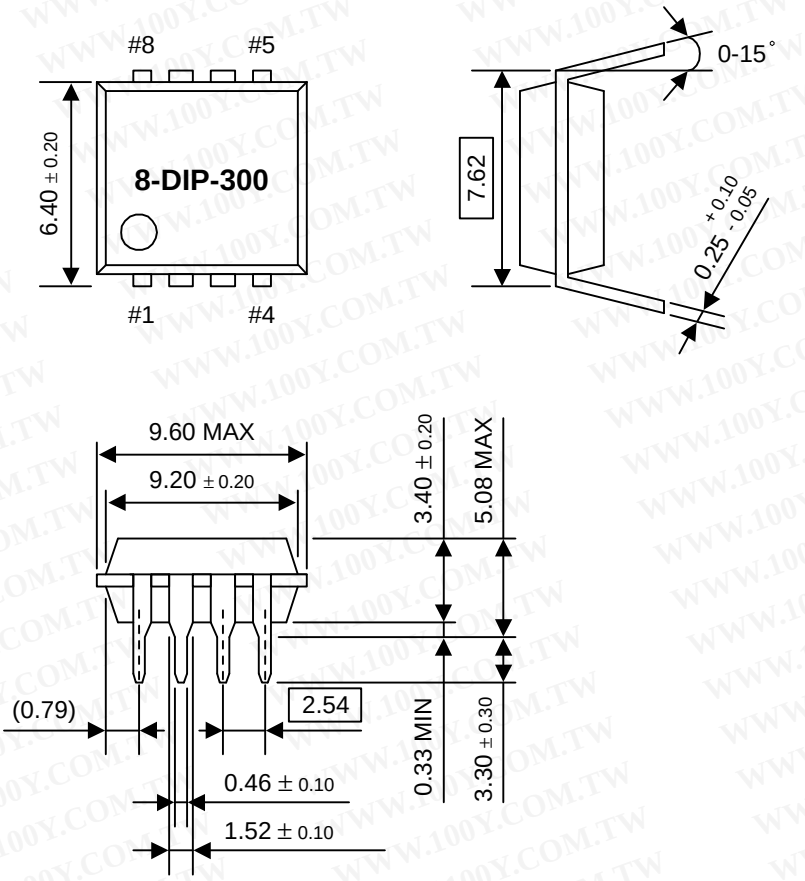
- 512K-bit (65,536 bytes) storage area
- 128-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 500,000 erase/write cycles
- 50 years data retention

Operating Characteristics

- Operating voltage
  - 1.8 V to 5.5 V
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 400 μA at 5.5 V
  - Maximum stand-by current: < 5 μA at 5.5 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 400 kHz at standard mode
  - 1 MHz at fast mode
- Electrostatic discharge (ESD)
  - 5,000 V (HBM)
  - 500 V (MM)

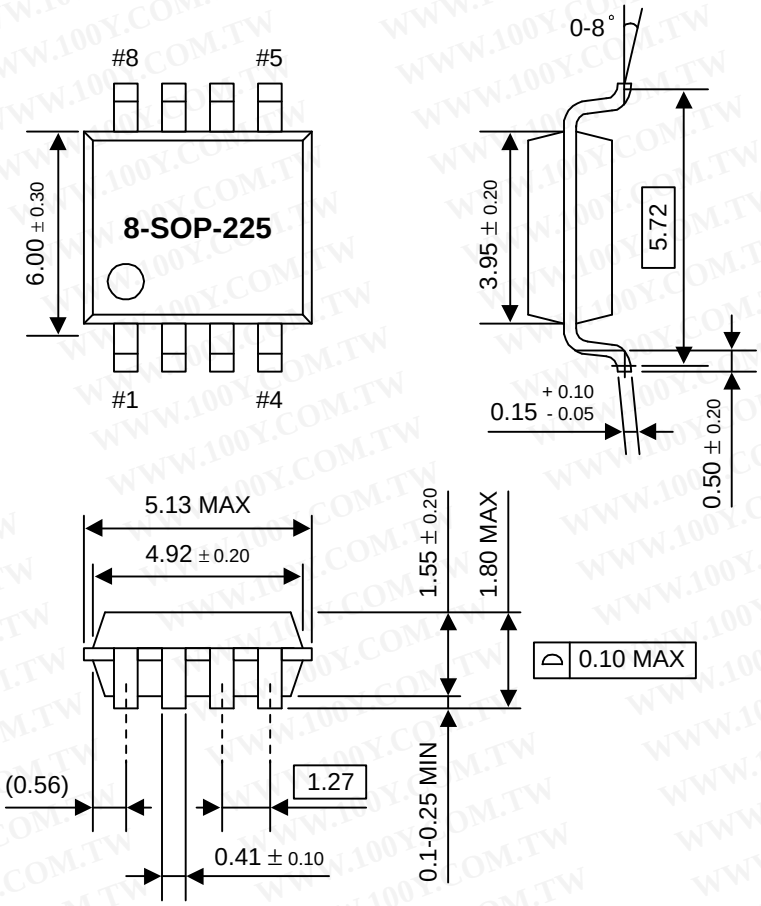
Packages

- 8-pin DIP, and SOP



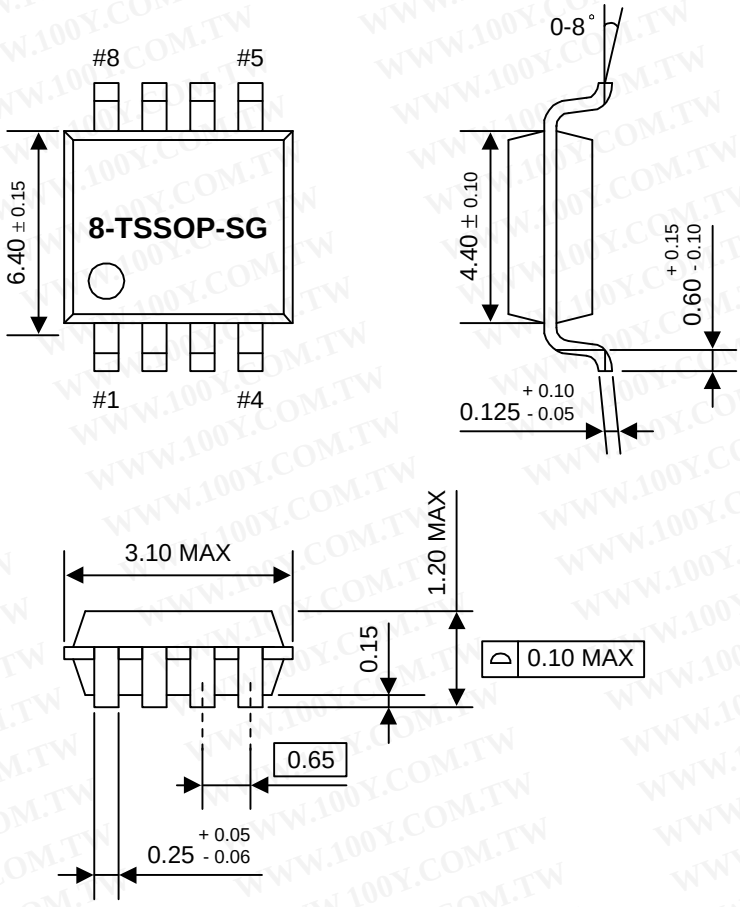
NOTE: Dimensions are in millimeters.

Figure 7-1. 8-DIP-300 Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 7-2. 8-SOP-225 Package Dimensions



NOTES:
1. Dimensions are in millimeters.
2. Package dimensions conform to JEDEC MO-153-AA.

Figure 7-3. 8-TSSOP Package Dimensions

SAMSUNG ELECTRONICS

Interfacing S524A Series Serial EEPROM to the S3C8095/S3C72F5 Microcontroller

Application Note

OVERVIEW

This application note describes an interface between the S524A40X21 serial EEPROM and Samsung S3C8095/S3C72F5 microcontroller. The S524A series support the standard I^{2}C™-bus serial data transmission protocol. S3C8095 is a 8-bit general purpose microcontroller, and S3C72F5 is a 4-bit general purpose microcontroller.

A typical circuit configuration between S3C8095/S3C72F5 and S524A40X21 is shown in Figure 8-1 and 8-2. As shown below, using the address inputs (A0, A1, A2), up to eight S524A40X21s can be connected to the same bus. The limited number of S524A series products (1 to 16 K-bit) which can be connected is shown in Table 8-1. The interface to the S3C8095/S3C72F5 uses there 2 I/O port lines. One of the lines is used to generate the serial clock (SCL), and the other is used as a bidirectional data line (SDA). It is recommended that an external pull-up resistor is configured to the SCL, SDL line. The S3C8095/S3C72F5 operate as a master which initiates a data transfer by generating the start condition on the bus, and a slave device S524A40X21 responds to the command issued by a master. The demonstration program which follows shows how the S524A40X21 serial EEPROM can be interfaced to the S3C8095/S3C72F5 microcontroller.

Table 8-1. S524A Series (1 to 16K-bit)

Device	EEPROM Size	Max Device Per Bus	Device Address Used
S524A40X10/40X11	1K-bit	8	A0, A1, A2
S524A40X20/40X21	2K-bit	8	A0, A1, A2
S524A40X40/40X41	4K-bit	4	A1, A2
S524A60X81	8K-bit	2	A2
S524A60X51	16K-bit	1	–

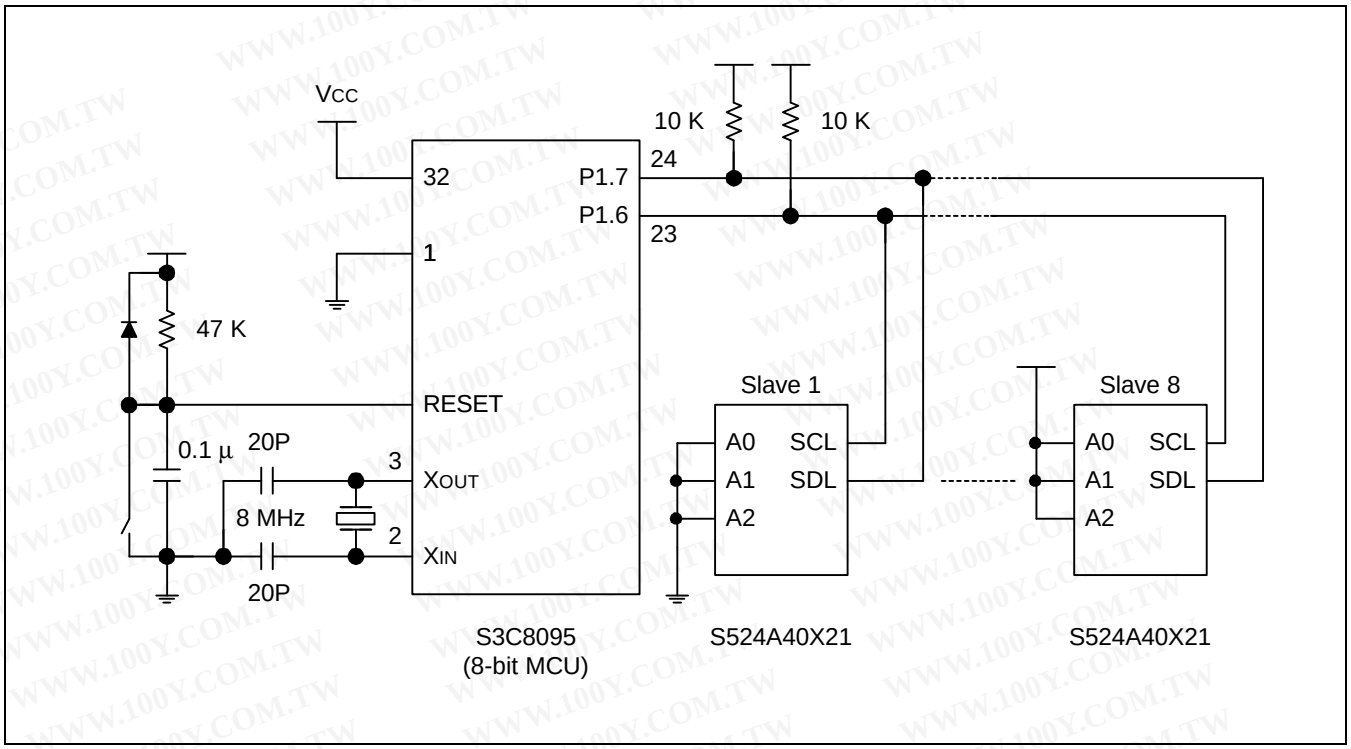


Figure 8-1. Typical Circuit Configuration 1

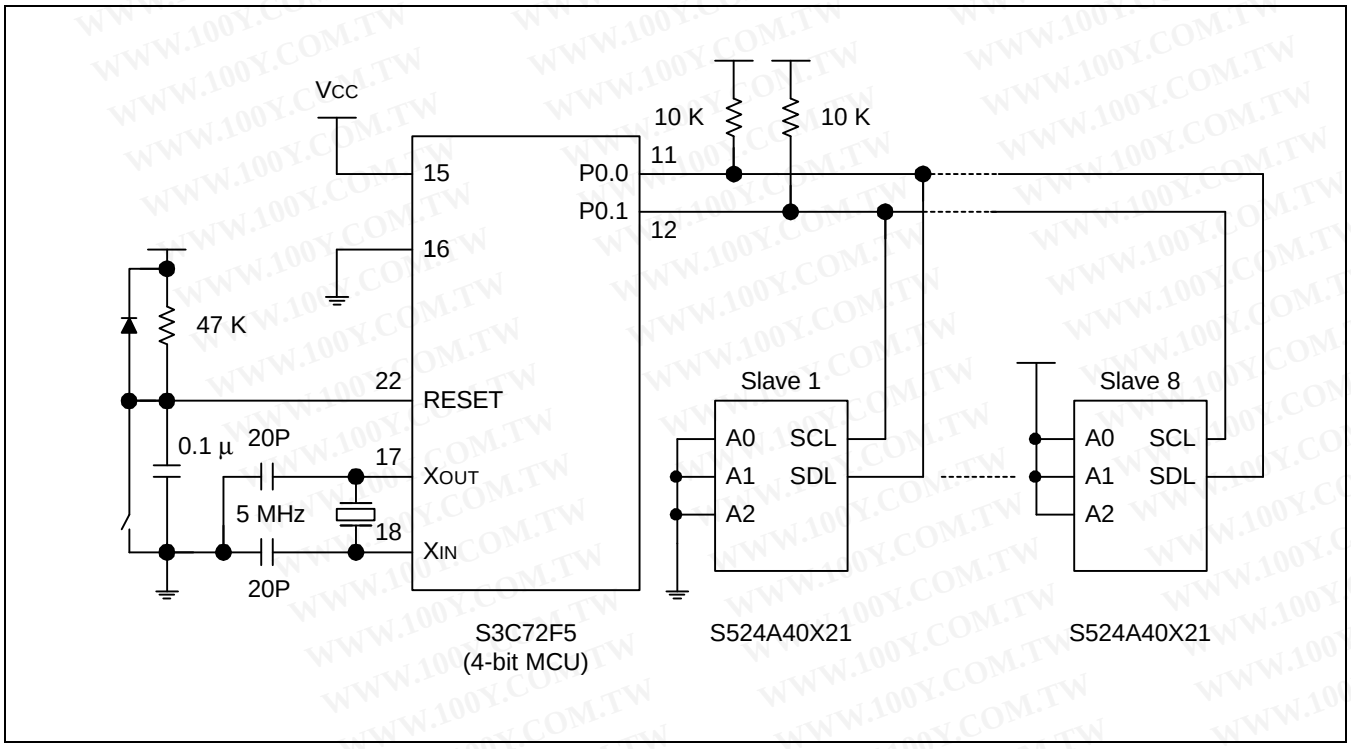


Figure 8-2. Typical Circuit Configuration 2

```
;*****************************************************************************************************************************

;This program demonstrates how the S524A40X21 serial EEPROM can be interfaced to the S3C8095
;microcontroller. This software includes random address byte read and byte write operation.
;If you use the 8 MHz crystal in Figure 8-1, SCL frequency will be approximately 50 kHz.

;*****************************************************************************************************************************
;                                                                    R14 = Word-address
;                                                                    R15 = Write-data to the EEPROM
;                                                                    ReadData = Read-data from the EEPROM
;*************************************************************************
;               Equation Table
;*************************************************************************
SDA             EQU     7H                      ;   SDA port (P1.7)
SCL             EQU     6H                      ;   SCL port (P1.6)
ReadData        EQU     40H
;*************************************************************************
;****************    Random Address Byte Read    ******************

; Start → Slave Addr.(A0) → Word Addr. → Start → #A1h → Data

;*************************************************************************

Read1Byte:      PUSH    R0
                PUSH    R1
                PUSH    R2
                CALL    IICbus_Start            ;   IIC bus protocol start
;
                LD      R0,#0A0h                ;   Slave address (A0)

                CLR     R2
RD_TxStart      LD      R1,#8                   ;   1byte (8bit) count
RD_DataShift    RLC     R0                      ;   Rotate left Data ( = R0)
                JP      C, RD_Data_1            ;   Bit value check(0 or 1)
RD_Data_0       AND     P1,#0FFh-(01<<SDA)      ;   Data “0” transfer
                CALL    IIC_Clock_1Bit
RD_Count8bit    DJNZ    R1,RD_DataShift
                AND     P1CONH,#00111111B       ;   SDA (P1.7) = Input Mode
                OR      P1,#01<<SCL             ;   Acknowledge clock
                NOP
                NOP
                NOP
                TM      P1,#01<<SDA             ;   Ack in?
                JP      NZ,CommuniFail
                AND     P1,#0FFh–(01<<SCL)
                OR      P1CONH,#01000000B       ;   SDA (P1.7) = Output Mode

;               (next page continued)
```

```
                CP      R2,#02                  ;  TxCount = R2
                JR      UGE,RxData
                CP      R2,#01
                JR      UGE,ReStart
;
                LD      R0,R14                  ;  TxCount++
                INC     R2                      ;  TxCount++
                JR      RD_TxStart
;
ReStart         OR      P1,#11000000B           ;  P1.7/P1.6 ← High (SDA,SCL)
                NOP
                NOP
                NOP
                AND     P1,#0FFh-(01<<SDA)      ;  IIC Start Condition
                NOP
                NOP
                NOP
                NOP
                AND     P1,#0FFh-(01<<SCL)
;
                LD      R0,#0A1h                ;  Slave Address for reading
                INC     R2                      ;  TxCount++
                JR      RD_TxStart
;
RxData          AND     P1CONH,#00111111B       ;  SDA (P1.7) = Input Mode
                NOP
                LD      R1,#8
RotateLoop      OR      P1,#01<<SCL             ;  SCL ← High
                TM      P1,#01<<SDA             ;  Data value check
                JR      NZ,SetCF
                RCF
                JR      DataRotate
;
SetCF           SCF
DataRotate      RLC     R0
                AND     P1,#0FFh-(01<<SCL)      ;  SCL ← Low
                DJNZ    R1,RotateLoop           ;  End of 1byte(8bit) ?
                LD      ReadData,R0

                OR      P1CONH,#01000000B       ;  SDA (P1.7) = Output
                OR      P1,#01<<SDA             ;  SDA ← High (ACK=High): communication
                                                ;  finished
                NOP
                NOP
                OR      P1,#01<<SCL             ;  SCL ← High (9th clock)
                NOP
                NOP

                AND     P1,#0FFh-(01<<SCL)      ;  SCL ← Low
                NOP

;               (next page continued)
```

```
GenlicStop      CALL    IICbus_Stop
                POP     R2
                POP     R1
                POP     R0
                RET
;
RD_Data_1       OR      P1,#01<<SDA                     ; Data “1” trasfer
                CALL    IIC_Clock_1Bit
                JP      RD_Count8bit
;
; ***************************************************************************
;******************        Byte Write Operation        ******************
; Start → Slave Addr.(A0) → Word addr. → Data
; ***************************************************************************
Write1Byte:     PUSH    R0
                PUSH    R1
                PUSH    R2
                CALL    IICbus_Start                    ;   IIC bus protocol start
;
                LD      R0,#0A0h                        ;   Slave address
                CLR     R2
WR_TxStart      LD      R1,#8                           ; 1 Byte (8bit) count
WR_DataShift    RLC     R0
                JR      C,WR_Data_1
WR_Data_0       AND     P1,#0FFh-(01<<SDA)              ;   Data “0” transfer
                CALL    IIC_Clock_1Bit

WR_Count8bit    DJNZ    R1,WR_DataShift                 ;   1byte check
;
                AND     P1CONH,#00111111B               ;   SDA (P1.7) = Input Mode
                OR      P1,#01<<SCL                     ;   Acknowledge clock
                NOP
                NOP
                NOP
                TM      P1,#01<<SDA                     ;   Ack in ?
                JR      NZ,CommuniFail
;
                AND     P1,#0FFh–(01<<SCL)
                OR      P1CONH,#01000000B               ;   SDA(P1.7) = Output Mode
;
                CP      R2,#2
                JR      UGE,TxStop
                CP      R2,#1
                JR      UGE,WriteData
                LD      R0,R14                          ;   Word Address
                INC     R2                              ;   TxCount++
                JR      WR_TxStart

;               (next page continued)
```

```
WriteData       LD      R0,R15                  ;  Data to be written to the EEPROM
                INC     R2                      ;  TxCount++
                JR      WR_TxStart
;
WR_Data_1       OR      P1,#01<<SDA             ;  Data “1” transfer
                CALL    IIC_Clock_1Bit
                JR      WR_Count8bit
;
CommuniFail     AND     P1,#0FFh–(01<<SCL)
                NOP
                NOP
                OR      P1CONH,#01000000B       ;  SDA(P1.7) = Output Mode
                JP      GenIicStop

TxStop          JP      GenIicStop

IICbus_Start    OR      P1,#11000000B           ;  P1.7/P1.6 ← High (SDA, SCL)
                NOP                             ;
                NOP
                NOP
                AND     P1,#0FFh–(01<<SDA)
                NOP
                NOP
                NOP
                NOP
                NOP
                AND     P1,#0FFh–(01<<SCL)
                RET

IIC_Clock_1Bit  OR      P1,#01<<SCL;            ;  Clock Generation.
                NOP
                NOP
                NOP
                AND     P1,#0FFh-(01<<SCL)
                NOP
                RET

IICbus_Stop     AND     P1,#0FFh-(01<<SDA)
                NOP
                NOP
                NOP
                OR      P1,#01<<SCL
                NOP
                NOP
                NOP
                NOP
                NOP
                OR      P1,#01<<SDA             ;  SDA ← High (Stop condition)
                RET
```

```
;*****************************************************************************************************************************

; This program demonstrates how the S524A40X21 serial EEPROM can be interfaced to the SAMSUNG
  S3C72F5 microcontroller. This software includes random address byte read and byte write operation.
; If you use the 5 MHz crystal oscillator, SCL frequency will be approximately 50 kHz

;*****************************************************************************************************************************

;*************************************************************************
;                Equation Table
;*************************************************************************

SDA_PORT        EQU             P0.0
SCL_PORT        EQU             P0.1
ReadAddr        EQU             20H
ReadData        EQU             22H
WriteAddr       EQU             30H
WriteData       EQU             32H
PMG1_BUF        EQU             40H
;*************************************************************************
;****************    Random Address Byte Read    ******************

; Start → Slave Addr.(A0) → Word Addr. → Start → #A1h → Data

;*************************************************************************

Read1Byte:      CALL    IICbus_Start            ;  IIC Interface start
                LD      Y,#0H
                LD      EA,#0A0h                ;  Slave Address (A0)

RD_TxStart      LD      Z,#7                    ;  1Byte (8bit)
RD_DataShift    ADC     EA,EA
                BTST    C
                JP      RD_Data_0

RD_Data_1       BITS    SDA_PORT                ;  Data "1" transfer
                CALL    IIC_Clock_1Bit
                JP      RD_Count8bit

RD_Data_0       BITR    SDA_PORT                ;  Data "0" transfer
                CALL    IIC_Clock_1Bit

RD_Count8bi     DECS    Z
                JP      RD_DataShift
                CALL    SdaInMode               ;  SDA Port Input Mode
                BITS    SCL_PORT
                NOP
                NOP
                NOP

;                (next page continued)
```

```
                BTSF    SDA_PORT                ;  ACK Check
                JP      CommuniFail
                BITR    SCL_PORT
                CALL    SdaOutMode
                CPSE    Y,#2H                   ;  TxCount = Y
                JP      NextR1
                JP      RxData

NextR1          CPSE    Y,#1H
                JP      NextR2
                JP      ReStart

NextR2          LD      EA,ReadAddr             ;  Pointed Address to Read
                INCS    Y                       ;  TxCount++
                JP      RD_TxStart

ReStart
                BITS    SDA_PORT                ;  SDA HIGH
                BITS    SCL_PORT                ;  SCL HIGH
                NOP
                NOP
                NOP
                NOP
                NOP
                BITR    SDA_PORT                ;  Start Condition
                NOP
                NOP
                NOP
                NOP
                NOP
                BITR    SCL_PORT
                NOP
                LD      EA,#0A1h                ;  Slave Address for Reading (A1)
                INCS    Y                       ;  Tx Count ++
                JP      RD_TxStart

RxData          CALL    SdaInMode
                NOP
                LD      EA,#00H                 ;  Clear
                LD      Z,#7                    ;  1Byte Count(8bit)

RotateLoop      BITS    SCL_PORT
                NOP
                NOP
                NOP
                BTSF    SDA_PORT
                JP      SetCF
                RCF                             ;  Data "0"
                JP      DataRotate

SetCF           SCF                             ;  Data "1"

;               (next page continued)
```

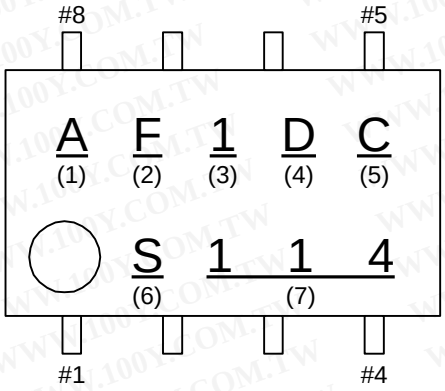
```
DataRotate      ADC     EA,EA
                BITR    SCL_PORT
                NOP
                NOP
                NOP
                DECS    Z
                JP      RotateLoop
                LD      ReadData,EA             ;  Save Read Data
                CALL    SdaOutMode
                BITS    SDA_PORT
                NOP
                NOP
                BITS    SCL_PORT
                NOP
                NOP
                BITR    SCL_PORT
                NOP

GenlicStop      CALL    IICbus_Stop
                RET

; *********************************************************************

;******************        Byte Write Operation        ******************

; Start → Slave Addr.(A0) → Word addr. → Data

; *********************************************************************

Write1Byte:     CALL    IICbus_Start
                LD      Y,#0H
                LD      EA,#Slave_WR            ;  Slave Address (A0)

WR_TxStart      LD      Z,#7                    ;  1Byte (8bit) count

WR_DataShift    ADC     EA,EA
                BTST    C
                JP      WR_Data_0

WR_Data_1       BITS    SDA_PORT                ;  Data “1” transfer
                CALL    IIC_Clock_1Bit
                BITR    SDA_PORT
                JP      WR_Count8bit

WR_Data_0       BITR    SDA_PORT                ;  Data “0” transfer
                CALL    IIC_Clock_1Bit

WR_Count8bit    DECS    Z                       ;  1byte check
                JP      WR_DataShift
                CALL    SdaInMode
                BITS    SCL_PORT

;               (next page continued)
```

```
                NOP
                NOP
                NOP
                BTSF    SDA_PORT                ;  ACK Check
                JP      CommuniFail

                BITR    SCL_PORT
                CALL    SdaOutMode
                CPSE    Y,#2H
                JP      NextW1
                JP      TxStop

NextW1          CPSE    Y,#1H
                JP      NextW2
                JP      WriteData

NextW2          LD      EA,WriteAddr            ;  Address to be written
                INCS    Y
                JP      WR_TxStart

WriteData       LD      EA,WriteData            ;  Data to be written
                INCS    Y
                JP      WR_TxStart

TxStop          JP      GenlicStop

IICbus_Start    CALL    SDASCL_OutMode
                NOP
                NOP
                NOP
                NOP
                NOP
                BITR    SDA_PORT                ;  Start Condition
                NOP
                NOP
                NOP
                NOP
                NOP
                BITR    SCL_PORT
                RET
IICbus_Stop     BITR    SDA_PORT
                NOP
                NOP
                BITS    SCL_PORT
                NOP
                NOP
                NOP
                NOP
                NOP
                BITS    SDA_PORT                ;  Stop Condition
                RET

;               (next page continued)
```

```
IIC_Clock_1Bit  BITS    SCL_PORT
                NOP
                NOP
                NOP
                BITR    SCL_PORT
                RET

SdaInMode       PUSH    EA
                LD      EA,PMG1_BUF
                AND     A,#1110B
                LD      PMG1_BUF,EA
                SMB     15
                LD      PMG1,EA                 ;   SDA INPUT
                SMB     0
                POP     EA
                RET

SdaOutMode      PUSH    EA
                SMB     0
                LD      EA,PMG1_BUF
                OR      A,#0001B
                LD      PMG1_BUF,EA
                SMB     15
                LD      PMG1,EA                 ;   SDA OUTPUT
                SMB     0
                POP     EA
                RET

CommuniFail     BITR    SCL_PORT
                NOP
                NOP
                CALL    SdaOutMode
                JP      GenlicStop


SDASCL_OutMode
                BITS    EMB
                SMB     15
                LD      EA,#00000001B
                LD      PNE1,EA                 ;   N-ch open drain (P0.0)
                LD      EA,#00000011B
                LD      PMG1,EA                 ;   SCL,SDA OUTPUT
                LD      PUMOD1,EA               ;   Pull-up enable
                SMB     0
                LD      PMG1_BUF,EA
                BITS    SDA_PORT
                NOP
                BITS    SCL_PORT
                RET
```

Marking Information

DIP/SOP



(1) Operating Voltage
- A = 1.8 V to 5.5 V
- L = 2.0 V to 5.5 V
- C = 2.5 V to 5.5 V

(2) EEPROM Density
- 1 = 1K-bit
- 2 = 2K-bit
- 4 = 4K-bit
- 8 = 8K-bit
- 5 = 16K-bit
- 9 = 32K-bit
- B = 64K-bit
- D = 128K-bit
- F = 256K-bit
- H = 512K-bit

(3) Write Protection
- 0 = Hardware and software
- 1 = Hardware Only

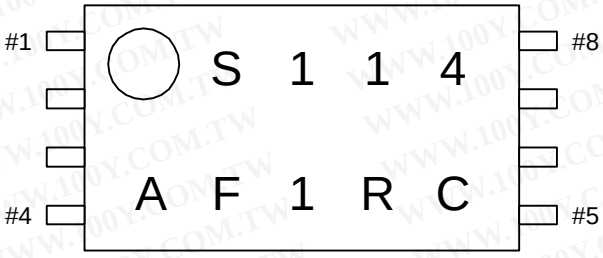
(4) Package Type
- D = DIP type
- S = SOP type
- R = TSSOP type

(5) Temperature Range
- C = -25° C to 70° C
- I = -40° C to 85° C

(6) Work Week Code

(7) Assembly Site Code

TSSOP



Ordering Information

S 5 2 4 A D 0 X F 1 - D C T 0

(1) (2) (3) (4) (5) (6) (7) (8) (9)

(1) Series Name
24: I^2C interface

(2) Operation Voltage
C: 2.5 V - 5.5 V
L: 2.0 V - 5.5 V
A: 1.8 V - 5.5 V

(3) Samsung's Internal Management Data

(4) ROM Size
1 = 1K-bit
2 = 2K-bit
4 = 4K-bit
8 = 8K-bit
5 = 16K-bit
9 = 32K-bit
B = 64K-bit
D = 128K-bit
F = 256K-bit
H = 512K-bit

(5) Write Protection
0 = Hardware and software
1 = Hardware only

(6) Package Type
D = DIP
R = TSSOP
S = SOP

(7) Temperature Range
C = -25° C to 70° C
I = -40° C to 85° C

(8) Package Type
B = Tube
T = Tape & Reel

(9) Customer Type
0 = None