

### FEATURES

- Integrated voltage regulator
- Upper/lower buffers swing to  $V_{DD}/GND$
- Single-supply operation: 7.5 V to 16.5 V
- Continuous current drive: 15 mA
- High peak output current: 150 mA
- Low offset voltage: 15 mV max
- Output voltage stable under transient load conditions

### APPLICATIONS

- TFT LCD monitor panels
- TFT LCD TV panels

### GENERAL DESCRIPTION

The ADD8709 is an 18-channel gamma reference for use in high-resolution TFT LCD monitor and TV panels. The output buffers feature low offset voltage and high current drive under transient load conditions to provide a more accurate and stable gamma curve. Two channels swing to  $V_{DD}$  and two channels swing to GND, increasing the overall range of the curve. An on-board voltage regulator is available for external applications. Here again, external component costs are reduced and the quality of the gray scale is increased.

The ADD8709 is specified over the temperature range of  $-40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$  and comes in a robust, low profile quad flat package.

### FUNCTIONAL BLOCK DIAGRAM



Figure 1. 48-Lead LQFP

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### Rev. 0

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**REVISION HISTORY**

7/04—Revision 0: Initial Version

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## ELECTRICAL CHARACTERISTICS

$7.5\text{ V} \leq V_{DD} \leq 16\text{ V}$ ,  $T_A @ 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ALL DEVICES						
POWER SUPPLY						
Supply Voltage	$V_S$		7.5		16	V
Supply Current	$I_{SYS}$	No load $-20^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		10.5	15	mA
					17	mA
VOLTAGE REGULATOR						
Dropout Voltage	$\Delta V_{DO}$	$I_L = 100\ \mu\text{A}$ $I_L = 5\ \text{mA}$		100	150	mV
Line Regulation	$REG_{LINE}$	$V_{IN} = 8.5\ \text{V to } 16.5\ \text{V}$ , $V_{OUT} = 8\ \text{V}$		0.01	0.20	%/V
Load Regulation	$REG_{LOAD}$	$I_O = 100\ \mu\text{A to } 10\ \text{mA}$		0.02	0.10	%/mA
Load Current	$I_O$			5		mA
Thermal Regulation	$REG_{THERMAL}$			0.005		%/W
GAMMA BUFFERS						
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{DD} = 7\ \text{V to } 17\ \text{V}$ , $-20^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$	68	90		dB
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$			5	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-20^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		20		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-20^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$		0.5	1.1	$\mu\text{A}$
					1.5	$\mu\text{A}$
Input Voltage Range			0		$V_{DD}$	V
Input Impedance	$Z_{IN}$			400		k $\Omega$
Input Capacitance	$C_{IN}$			1		pF
OUTPUT CHARACTERISTICS						
Output Performance (V1, V8, V9, V18)	$\Delta V_{OUT}^1$	$I_L = 20\ \text{mA}$ , $V_{DD} = 16\ \text{V}$		15		mV
Output Performance (V2 to V7, V10 to V17)	$\Delta V_{OUT}^1$	$I_L = 5\ \text{mA}$ , $V_{DD} = 16\ \text{V}$		5		mV
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\ \text{k}\Omega$ , $C_L = 200\ \text{pF}$	4	6		V/ $\mu\text{s}$
Bandwidth	BW	-3 dB, $R_L = 10\ \text{k}\Omega$ , $C_L = 200\ \text{pF}$		4.5		MHz
Settling Time to 0.1%	$t_s$	1 V, $R_L = 10\ \text{k}\Omega$ , $C_L = 200\ \text{pF}$		1.1		$\mu\text{s}$
Phase Margin	$\phi_O$	$R_L = 10\ \text{k}\Omega$ , $C_L = 200\ \text{pF}$		55		Degrees

<sup>1</sup>  $\Delta V_{OUT}$  is the shift from the desired output voltage under the specified current load.

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**ADD8709**

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage ( $V_{DD}$ )	18 V
Input Voltage	-0.5 V to $V_{DD}$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range <sup>1</sup>	-40°C to +100°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
ESD Tolerance (HBM)	±2000 V
ESD Tolerance (MM)	±150 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Package Characteristics

Package Type	$\theta_{JA}$	Unit
LQFP (ST)	74.57	°C/W

<sup>1</sup> See Application Notes section.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

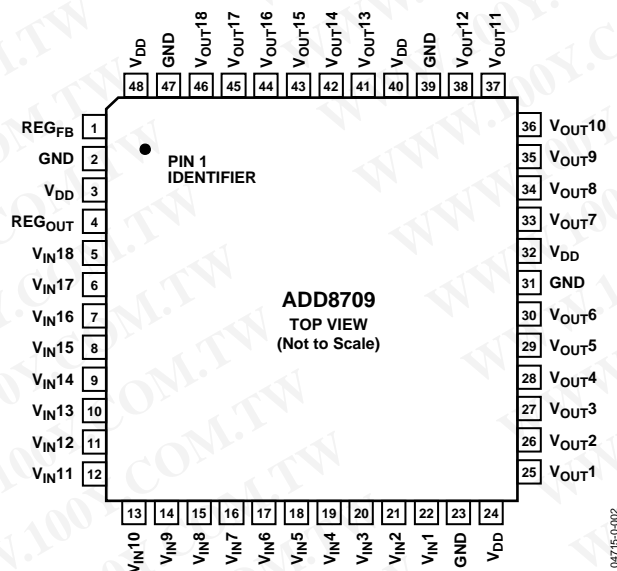


Figure 2. 48-Lead Low Profile Quad Flat Package (ST-48)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Name	Description
1	REG <sub>FB</sub>	Regulator Feedback	Compares a percentage of the regulator output to the internal voltage reference. Internal resistors are used to program the desired regulator output voltage.
2	GND	Ground	Ground. Nominally 0 V.
3	V <sub>DD</sub>	Supply	Supply voltage or source voltage. Nominally 16 V.
4	REG <sub>OUT</sub>	Regulator Output	Provides a regulated output voltage for use as a reference for additional external gamma channels.
5	V <sub>IN18</sub>	Input	Buffer input.
6	V <sub>IN17</sub>		
7	V <sub>IN16</sub>		
8	V <sub>IN15</sub>		
9	V <sub>IN14</sub>		
10	V <sub>IN13</sub>		
11	V <sub>IN12</sub>		
12	V <sub>IN11</sub>		
13	V <sub>IN10</sub>		
14	V <sub>IN9</sub>		
15	V <sub>IN8</sub>		
16	V <sub>IN7</sub>		
17	V <sub>IN6</sub>		
18	V <sub>IN5</sub>		
19	V <sub>IN4</sub>		
20	V <sub>IN3</sub>		
21	V <sub>IN2</sub>		
22	V <sub>IN1</sub>		
23	GND	Ground	Ground. Nominally 0 V.
24	V <sub>DD</sub>	Supply	Supply voltage. Nominally 16 V.
25	V <sub>OUT1</sub>	Output	Buffer output. Designed to have higher sink than source capability.
26	V <sub>OUT2</sub>		

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Pin No.	Mnemonic	Name	Description
27	V <sub>out3</sub>	Output	Buffer output.
28	V <sub>out4</sub>		
29	V <sub>out5</sub>		
30	V <sub>out6</sub>		
31	GND	Ground	Ground. Nominally 0 V.
32	V <sub>DD</sub>	Supply	Supply voltage. Nominally 16 V.
33	V <sub>out7</sub>	Output	Buffer output.
34	V <sub>out8</sub>		
35	V <sub>out9</sub>		
36	V <sub>out10</sub>		
37	V <sub>out11</sub>		
38	V <sub>out12</sub>		
39	GND	Ground	Ground. Nominally 0 V.
40	V <sub>DD</sub>	Supply	Supply voltage. Nominally 16 V.
41	V <sub>out13</sub>	Output	Buffer output.
42	V <sub>out14</sub>		
43	V <sub>out15</sub>		
44	V <sub>out16</sub>		
45	V <sub>out17</sub>	Output	Buffer output. Designed to have higher source than sink capability.
46	V <sub>out18</sub>		
47	GND	Ground	Ground. Nominally 0 V.
48	V <sub>DD</sub>	Supply	Supply voltage. Nominally 16 V.

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TYPICAL APPLICATIONS CIRCUIT

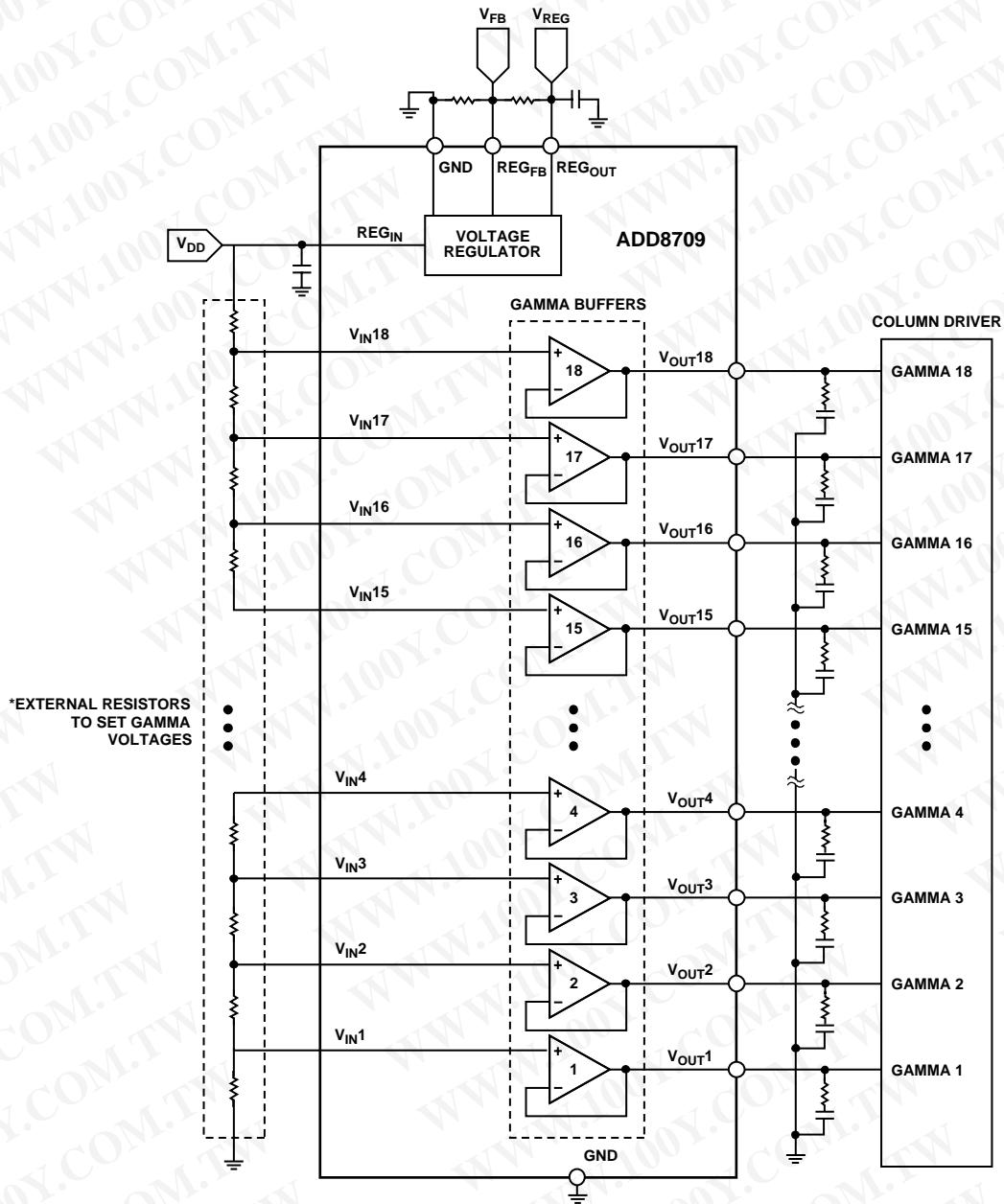


Figure 3.

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# TYPICAL PERFORMANCE CHARACTERISTICS

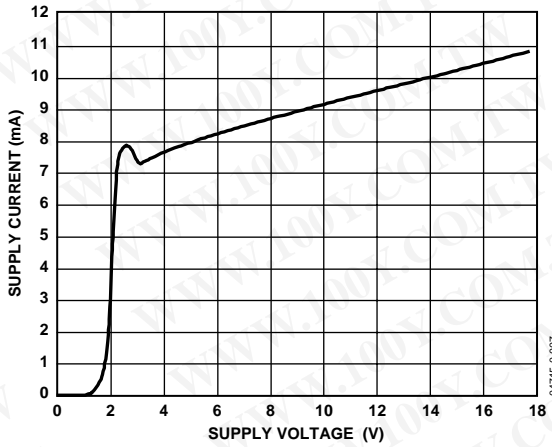


Figure 4. Supply Current vs. Supply Voltage

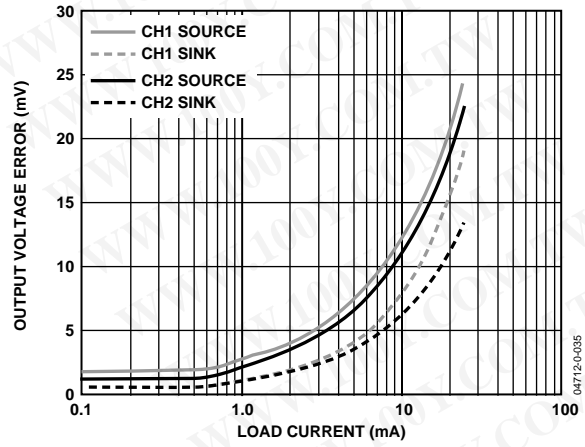


Figure 7. Output Voltage Error vs. Load Current

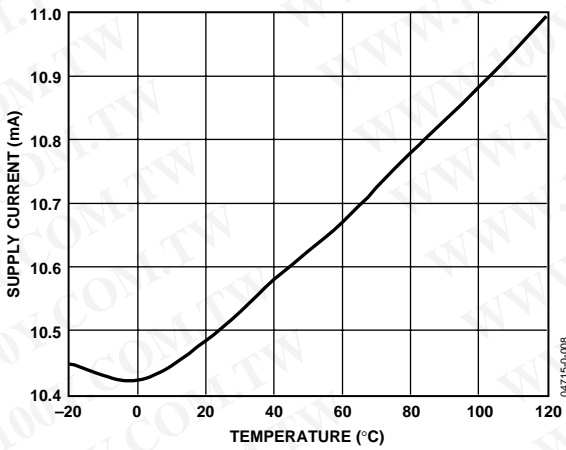


Figure 5. Supply Current vs. Temperature

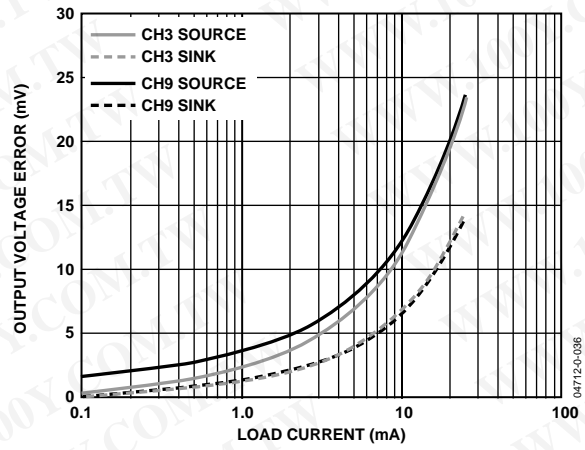


Figure 8. Output Voltage Error vs. Load Current

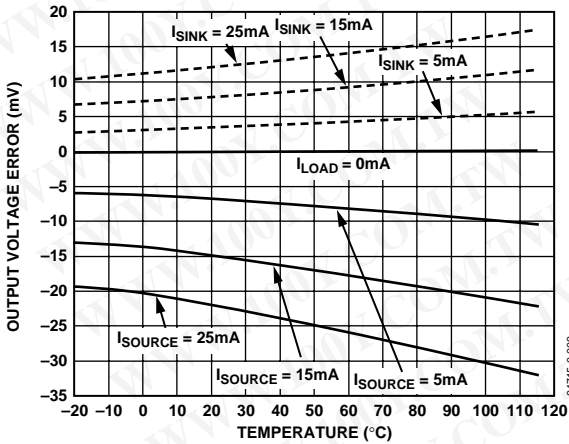


Figure 6. Output Voltage Error vs. Temperature

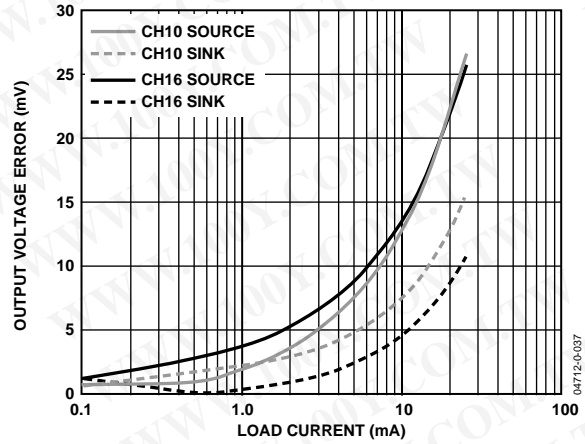


Figure 9. Output Voltage Error vs. Load Current



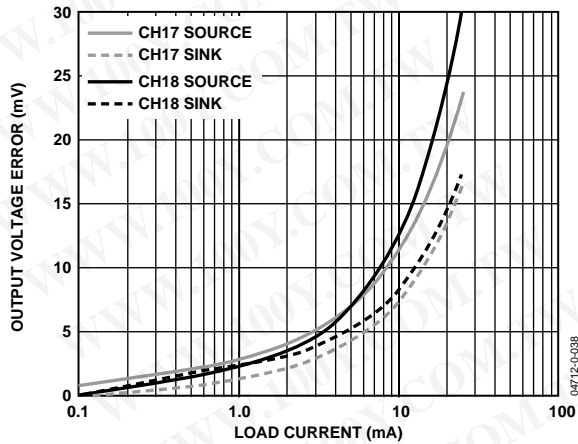


Figure 10. Output Voltage Error vs. Load Current

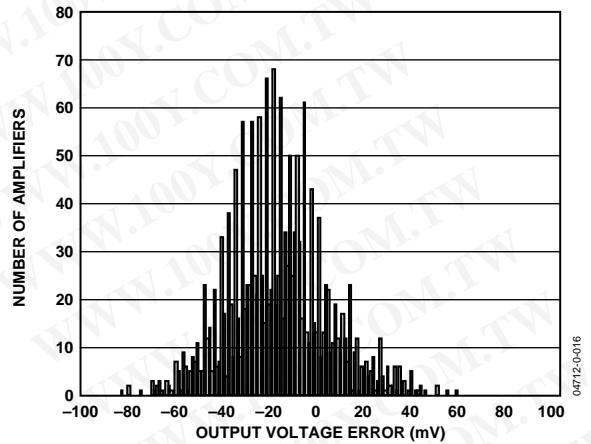


Figure 13. Output Voltage Error/Gamma 10 to 16

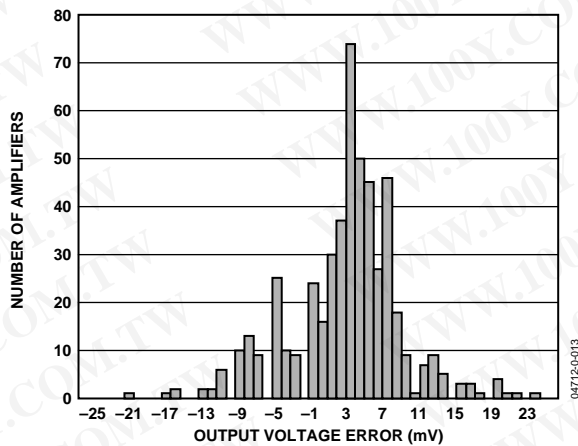


Figure 11. Output Voltage Error/Gamma 1 and 2

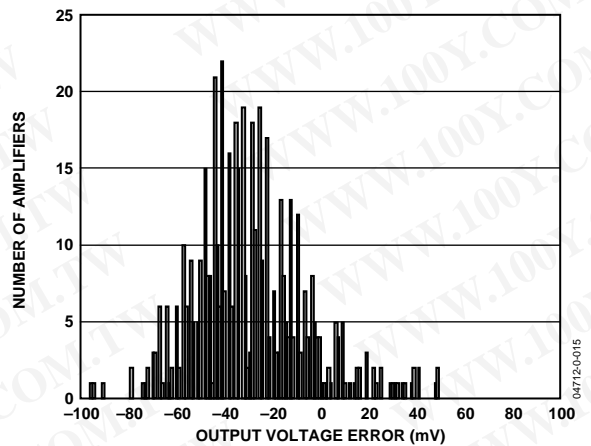


Figure 14. Output Voltage Error/Gamma 17 and 18

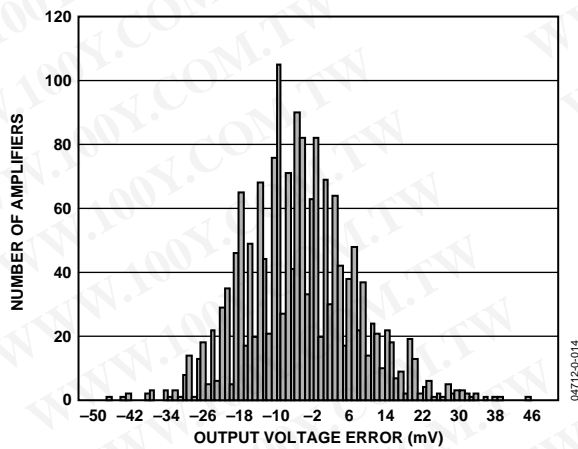


Figure 12. Output Voltage Error/Gamma 3 to 9

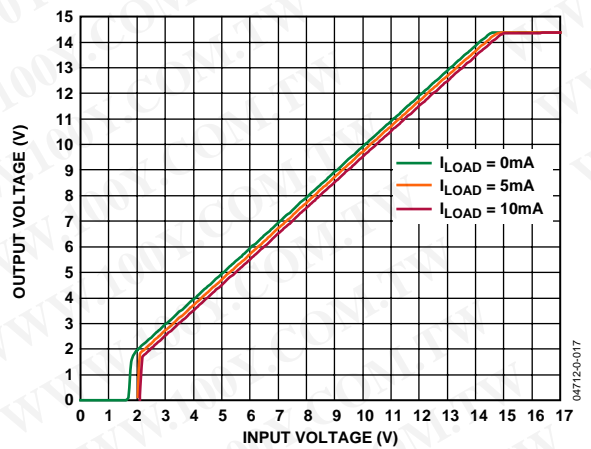


Figure 15. Dropout Characteristics

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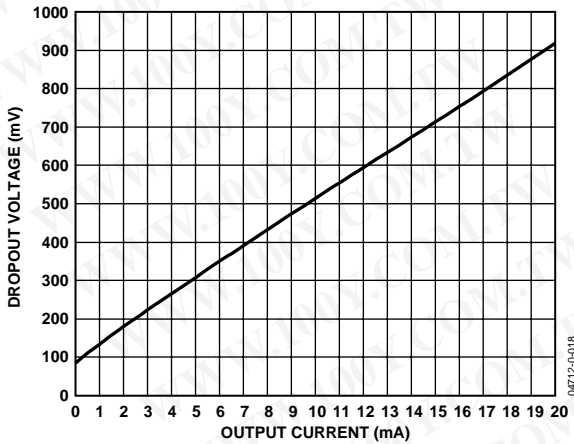


Figure 16. Dropout Voltage vs. Output Current

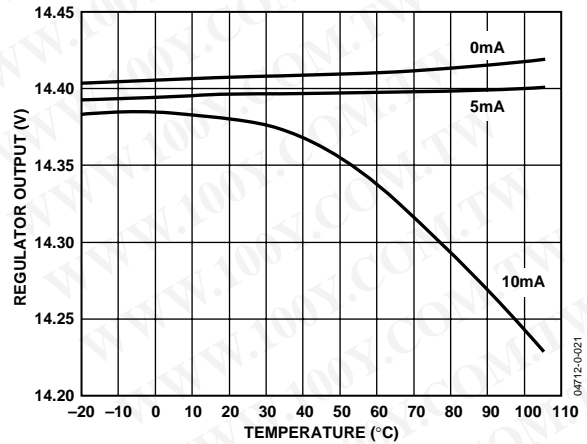


Figure 19. Regulator Output vs. Temperature

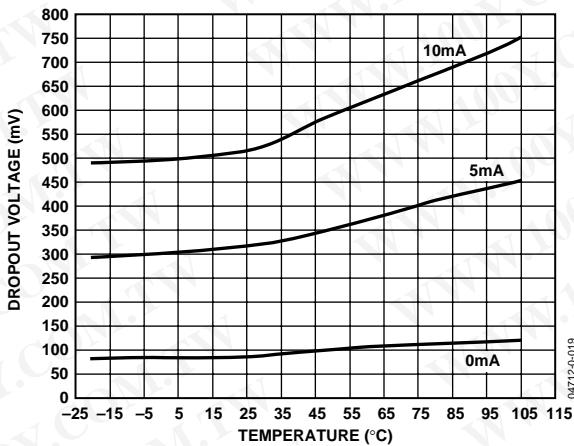


Figure 17. Dropout Voltage vs. Temperature

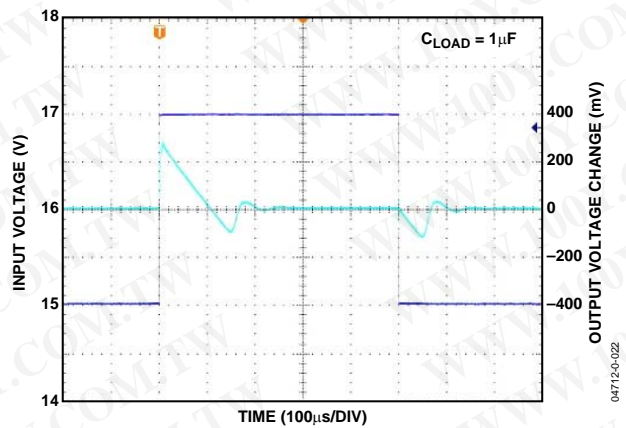


Figure 20. Regulator Line Transient Response

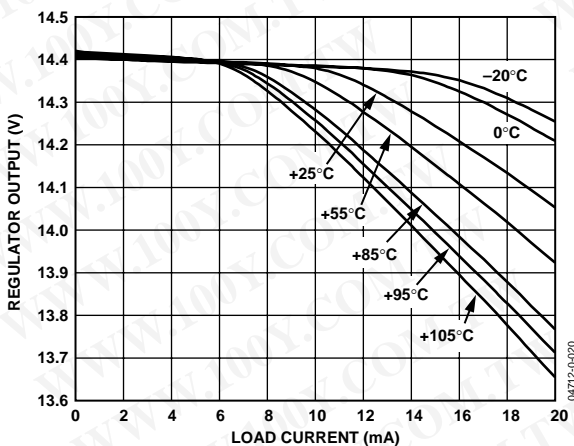


Figure 18. Regulator Output vs.  $I_{LOAD}$  Over Temperature

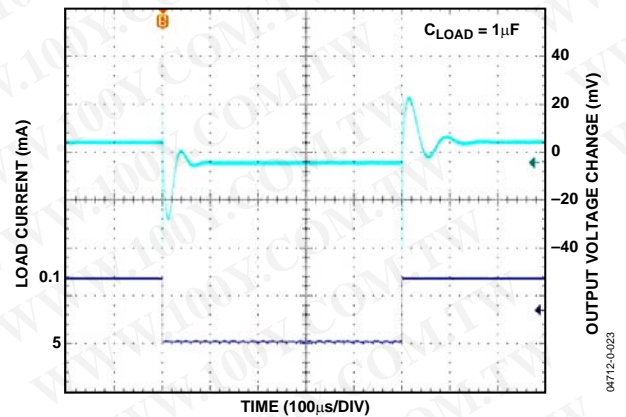


Figure 21. Regulator Load Transient Response

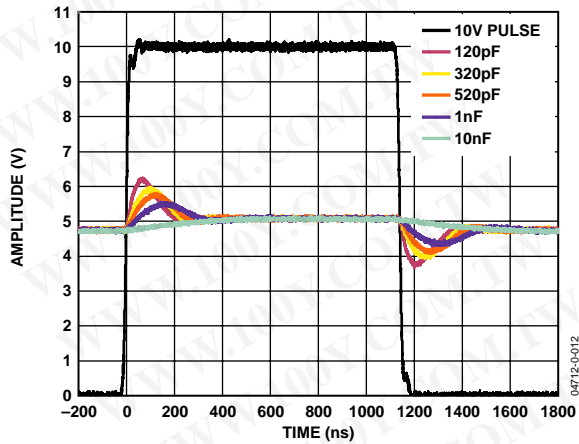


Figure 22. Transient Load Response vs. Capacitive Loading

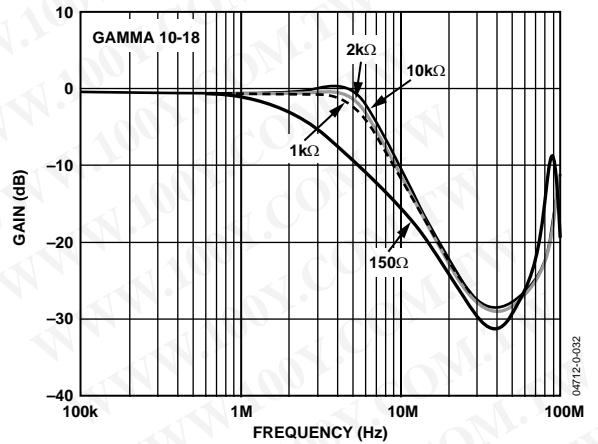


Figure 25. Frequency Response vs. Resistive Loading

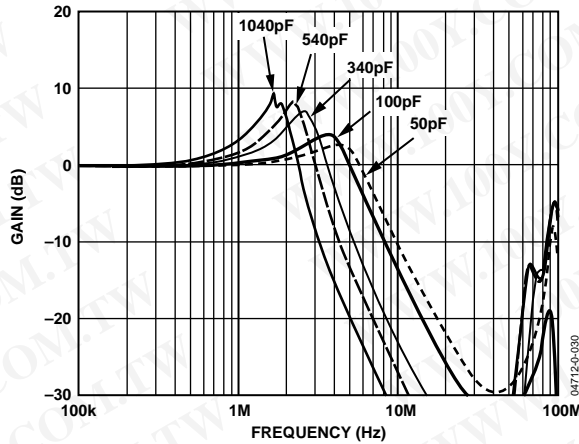


Figure 23. Frequency Response vs. Capacitive Loading

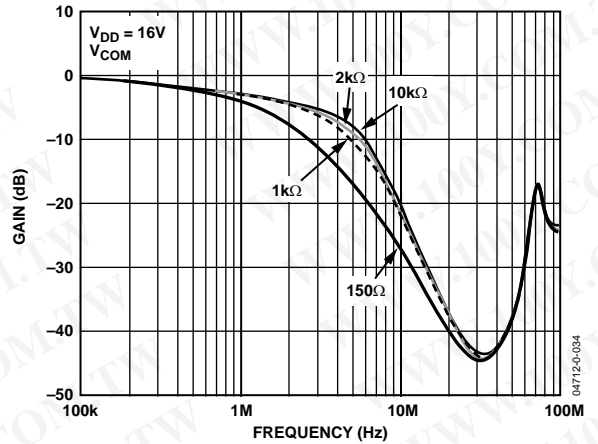


Figure 26. Frequency Response vs. Resistive Loading

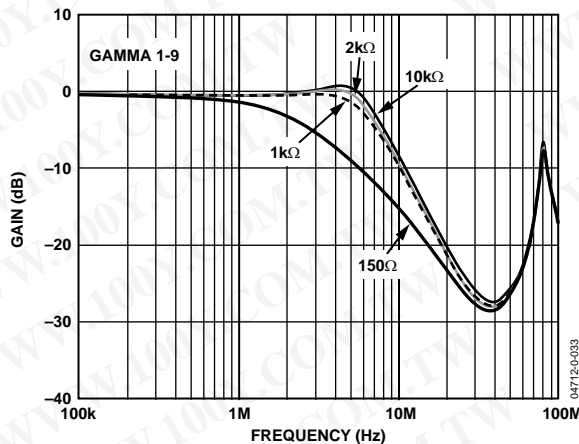


Figure 24. Frequency Response vs. Resistive Loading

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## APPLICATION NOTES

### MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADD8709 package is limited by the associated rise in junction temperature ( $T_J$ ) on the die. At approximately 150°C, the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADD8709. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

### OPERATING TEMPERATURE RANGE

The maximum junction temperature is as follows:

$$T_J = T_{AMB\ MAX} + \theta_{JA} \times W_{MAX}$$

where:

$T_{AMB\ MAX}$  = maximum ambient temperature specified on the data sheet.

$\theta_{JA}$  = junction-to-ambient thermal resistance, in °C/watt.

$W_{MAX}$  = maximum power dissipated in the device, in watts.

For the ADD8709,  $W_{MAX}$  can be calculated with the following equation:

$$W_{MAX} = V_{DD} \times I_{SYS} + V_{OUT} \times I_{OUT} + V_{DO} \times I_O$$

where:

$V_{DD} \times I_{SYS}$  = nominal system power requirements

$V_{OUT} \times I_{OUT}$  = amplifier load power dissipation

$V_{DO} \times I_O$  = regulator load power dissipation

### Example 1

The estimated power consumption of the ADD8709 in extreme cases is as follows:

$$V_{DD} \times I_{SYS} = 15\text{ V} \times 15\text{ mA}$$

$$V_{OUT} \times I_{OUT} = (8\text{ V} \times 5\text{ mA/channel}) \times 18\text{ channels}$$

$$V_{DO} \times I_O = 0.6\text{ V} \times 5\text{ mA}$$

$$W_{MAX} = (15\text{ V} \times 15\text{ mA}) + (8\text{ V} \times 5\text{ mA/channel} \times 18\text{ channel}) + (0.6\text{ V} \times 5\text{ mA}) = 0.948\text{ W}$$

$$\theta_{JA} = 74.57^\circ\text{C/W}, T_{AMB\ MAX} = 45^\circ\text{C}$$

$$T_J = 45^\circ\text{C} + (74.57^\circ\text{C/W}) \times (0.948\text{ W}) = 115.7^\circ\text{C}$$

Here, 150°C is the maximum junction temperature that is guaranteed before the part breaks down, while 125°C is the maximum process limit. Because  $T_J$  is < 150°C and < 125°C, this example demonstrates a condition where the part should perform within process limits.

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OUTLINE DIMENSIONS

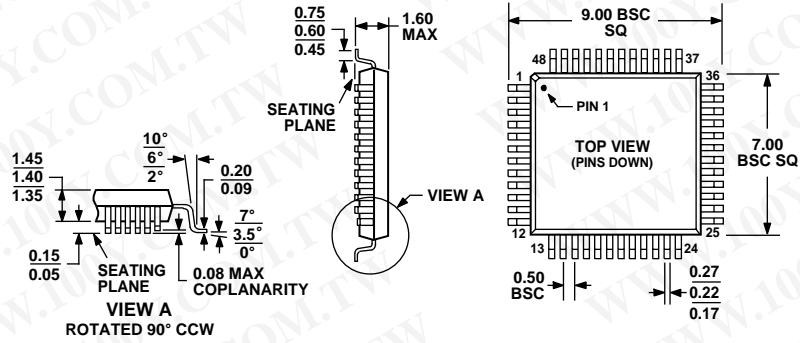


Figure 27. 48-Lead Low Profile Quad Flat Package (ST-48)  
Dimensions shown in millimeters

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# ADD8709

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADD8709ASTZ-REEL <sup>2</sup>	-40°C to +100°C	48-Lead Low Profile Quad Flat Package	ST-48
ADD8709ASTZ-REEL7 <sup>2</sup>	-40°C to +100°C	48-Lead Low Profile Quad Flat Package	ST-48

<sup>1</sup> Available in reels only.

<sup>2</sup> Z = Pb-free part.

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