M51995AP/FP

SWITCHING REGULATOR CONTROL

DESCRIPTION

M51995A is the primary switching regulator controller which is especially designed to get the regulated DC voltage from AC power supply.

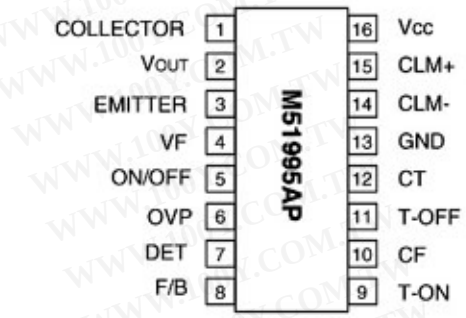
This IC can directly drive the MOS-FET with fast rise and fast fall output pulse.

Type M51995A has the functions of not only high frequency OSC and fast output drive but also current limit with fast response and high sensibility so the true "fast switching regulator" can be realized.

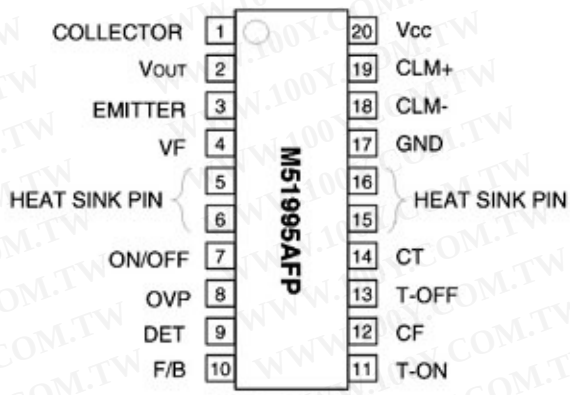
It has another big feature of current protection to short and over current,owing to the integrated timer-type protection circuit,if few parts are added to the primary side.

The M51995A is equivalent to the M51977 with externally re-settable OVP(over voltage protection)circuit.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4



Outline 20P2N-A

Connect the heat sink pin to GND.

FEATURES

- 500kHz operation to MOS FET
  - •Output current.....±2A
  - •Output rise time 60ns,fall time 40ns
  - •Modified totempole output method with small through current
- Compact and light-weight power supply
  - •Small start-up current.....90μA typ.
  - •Big difference between "start-up voltage" and "stop voltage" makes the smoothing capacitor of the power input section small. Start-up threshold 16V,stop voltage 10V
  - •Packages with high power dissipation are used to with-stand the heat generated by the gate-drive current of MOS FET. 16-pin DIP,20-pin SOP 1.5W(at 25°C)
- Simplified peripheral circuit with protection circuit and built-in large-capacity totempole output
  - •High-speed current limiting circuit using pulse-by-pulse method(Two system of CLM+pin,CLM-pin)
  - •Protection by intermittent operation of output over current..... .....Timer protection circuit
  - •Over-voltage protection circuit with an externally re-settable latch(OVP)
  - •Protection circuit for output miss action at low supply voltage(UVLO)
- High-performance and highly functional power supply
  - •Triangular wave oscillator for easy dead time setting

APPLICATION

Feed forward regulator,fly-back regulator

RECOMMENDED OPERATING CONDITIONS

Supply voltage range.....12 to 36V

Operating frequency.....less than 500kHz

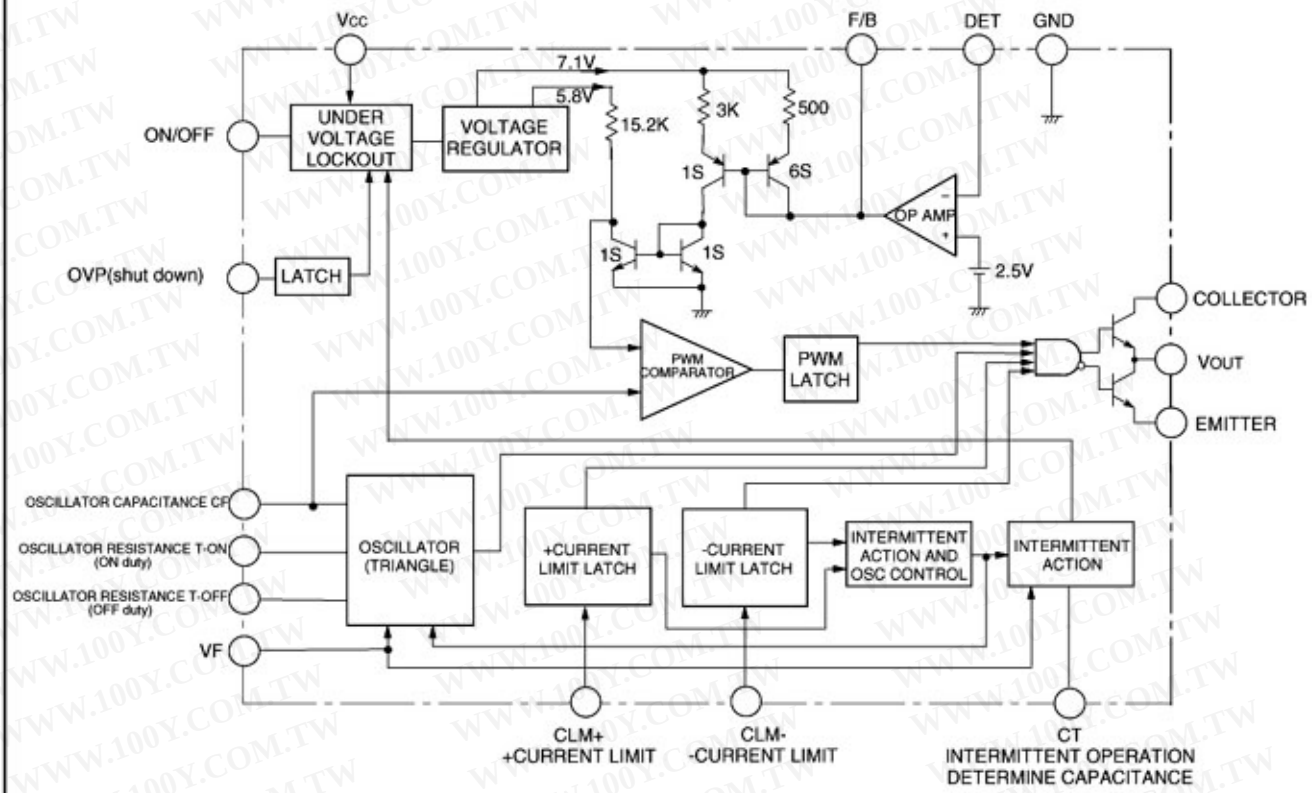
Oscillator frequency setting resistance

- •T-ON pin resistance RON.....10k to 75kΩ
- •T-OFF pin resistance ROFF.....2k to 30kΩ

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-34970699
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

RENESAS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		36	V
V_C	Collector voltage		36	V
I_O	Output current	Peak	±2	A
		Continuous	±0.15	
V_{VF}	V_F terminal voltage		Vcc	V
$V_{ON/OFF}$	ON/OFF terminal voltage		Vcc	V
V_{CLM-}	CLM-terminal voltage		-4.0 to +4.0	V
V_{CLM+}	CLM+terminal voltage		-0.3 to +4.0	V
I_{OVP}	OVP terminal current		8	mA
V_{DET}	DET terminal voltage		6	V
I_{DET}	DET terminal input current		5	mA
V_{FB}	F/B terminal voltage		0~10	V
I_{TON}	T-ON terminal input current		-1	mA
I_{TOFF}	T-OFF terminal input current		-2	mA
P_d	Power dissipation	Ta=25°C	1.5	W
K_θ	Thermal derating factor	Ta>25°C	12	mW/°C
T_{opr}	Operating temperature		-30 to +85	°C
T_{stg}	Storage temperature		-40 to +125	°C
Tj	Junction temperature		150	°C

Note 1."+" sign shows the direction of current flow into the IC and "-" sign shows the current flow from the IC.
2.This terminal has the constant voltage characteristic of 6 to 8V,when current is supplied from outside.The maximum allowable voltage is 6V when the constant voltage is applied to this terminal.And maximum allowable current into this terminal is 5mA.
3.The low impedance voltage supply should not be applied to the OVP terminal.

ELECTRICAL CHARACTERISTICS (V_{CC}=18V, Ta=25°C, unless otherwise noted)

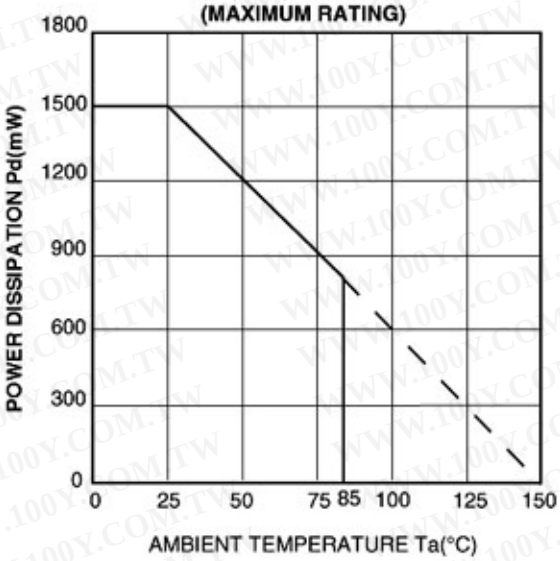
Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Supply voltage circuit current	V_{CC}	Operating supply voltage range		$V_{CC(STOP)}$	—	35	V
	$V_{CC(START)}$	Operation start up voltage		15.2	16.2	17.2	V
	$V_{CC(STOP)}$	Operation stop voltage		9.0	9.9	10.9	V
	ΔV_{CC}	Difference voltage between operation start and stop	$\Delta V_{CC}=V_{CC(START)}-V_{CC(STOP)}$	5.0	6.3	7.6	V
	I_{CCL}	Stand-by current	Vcc=14.5V,Ta=25°C	50	90	140	µA
			Vcc=14.5V,-30≤Ta≤85°C	40	90	190	µA
	I_{CCO}	Operating circuit current	Vcc=30V	10	15	21	mA
	$I_{CC\ OFF}$	Circuit current in OFF state	Vcc=25V	0.95	1.31	5.0	mA
			Vcc=14V	50	90	140	µA
	$I_{CC\ CT}$	Circuit current in timer OFF state	Vcc=25V	0.95	1.35	2.0	mA
			Vcc=14V	—	160	240	µA
	$I_{CC\ OVP}$	Circuit current in OVP state	Vcc=25V	1.3	2.0	3.0	mA
			Vcc=9.5V	125	200	310	µA
ON/OFF	$V_{THH\ ON/OFF}$	ON/OFF terminal high threshold voltage		2.1	2.6	3.1	V
	$V_{THL\ ON/OFF}$	ON/OFF terminal low threshold voltage		1.9	2.4	2.9	V
	$\Delta V_{THON/OFF}$	ON/OFF terminal hysteresis voltage		0.1	0.2	3.0	V
F/B	I_{FBMIND}	Current at 0% duty	F/B terminal input current	-2.1	-1.54	-1.0	mA
	I_{FBMAXD}	Current at maximum duty	F/B terminal input current	-0.90	-0.55	-0.40	mA
	ΔI_{FB}	Current difference between max and 0% duty	$\Delta I_{FB}=I_{FBMIND}-I_{FBMAXD}$	-1.35	-0.99	-0.70	mA
	V_{FB}	Terminal voltage	F/B terminal input current=0.95mA	4.9	5.9	7.1	V
	R_{FB}	Terminal resistance		420	600	780	Ω
Detection	V_{DET}	Detection voltage		2.4	2.5	2.6	V
	I_{INDET}	Input current of detection amp	V_{DET}=2.5V	—	1.0	3.0	µA
	G_{AVDET}	Voltage gain of detection amp		30	40	—	dB
OVP	V_{THOVPH}	OVP terminal H threshold voltage		540	750	960	mV
	ΔV_{THOVP}	OVP terminal hysteresis voltage	$\Delta V_{THOVP}=V_{THOVPH}-V_{THOVPL}$		30		mV
	I_{THOVP}	OVP terminal threshold current		80	150	250	µA
	I_{INOVP}	OVP terminal input current	V_{OVP}=400mV	80	150	250	µA
	V_{CCOVPC}	OVP reset supply voltage	OVP terminal is open. (high impedance)	7.5	9.0	10.0	V
	$V_{CC(STOP)}-V_{CCOVPC}$	Difference supply voltage between operation stop and OVP reset		0.55	1.20	—	V
	I_{THOVPC}	Current from OVP terminal for OVP reset	Vcc=30V	-480	-320	-213	µA
			Vcc=18V	-210	-140	-93	
Timer	f_{TIMER}	Timer frequency	C_T=4.7µF	0.27	0.40	0.60	Hz
	I_{TIMECH}	Timer charge current	V_{CT}=3.3V,Ta=-5°C	-193	-138	-102	µA
			Ta=25°C	-178	-127	-94	
			Ta=85°C	-147	-105	-78	
	$TIME_{OFF/ON}$	OFF time/ON time ratio		7.0	8.7	11.0	—
CLM-	V_{THCLM-}	CLM- terminal threshold voltage	-5≤Ta≤85°C	-220	-200	-180	mV
	I_{INCLM-}	CLM- terminal current	V_{CLM-}=-0.1V	-170	-125	-90	µA
	T_{PDCLM-}	Delay time from CLM- to V_{OUT}		—	100	—	ns
CLM+	V_{THCLM+}	CLM+ terminal threshold voltage	-5≤Ta≤85°C	180	200	220	mV
	I_{INCLM+}	CLM+ terminal current	V_{CLM+}=0V	-270	-205	-140	µA
	T_{PDCLM+}	Delay time from CLM+ to V_{OUT}		—	100	—	ns

ELECTRICAL CHARACTERISTICS (V_{CC}=18V, Ta=25°C, unless otherwise noted)(CONTINUE)

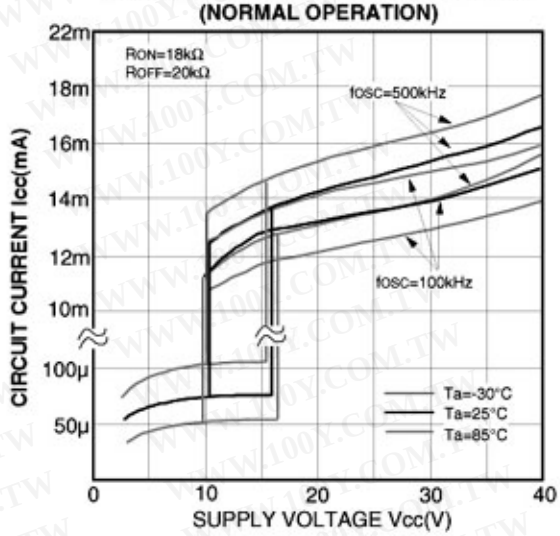
Block	Symbol	Parameter		Test conditions	Limits			Unit
					Min.	Typ.	Max.	
Oscillator	f_{OSC}	Oscillating frequency		R_{ON}=20kΩ, R_{OFF}=17kΩ C_F=220pF, -5≤Ta≤85°C	170	188	207	kHz
	T_{DUTY}	Maximum ON duty			47.0	50.0	53.0	%
	V_{OSCH}	Upper limit voltage of oscillation waveform		f_{OSC}=188kHz	3.97	4.37	4.77	V
	V_{OSCL}	Lower limit voltage of oscillation waveform		f_{OSC}=188kHz	1.76	1.96	2.16	V
	ΔV_{OSC}	Voltage difference between upper limit and lower limit of OSC waveform		f_{OSC}=188kHz	2.11	2.41	2.71	V
V_F	f_{OSCVF}	OSC frequency in CLM operating state	V_F=5V	R_{ON}=20kΩ, R_{OFF}=17kΩ C_F=220pF	170	188	207	kHz
			V_F=2V		108	124	143	
	T_{VFDUTY}	Duty in CLM operating state	V_F=0.2V	Min off duty/Max on duty	11.0	13.7	22.0	—
	V_{THTIME}	V_F voltage at timer operating start			2.7	3.0	3.3	V
	I_{VF}	V_F terminal input current		Source current	—	2	6	μA
Output	V_{OL1}	Output low voltage		Vcc=18V, Io=10mA	—	0.05	0.4	V
	V_{OL2}			Vcc=18V, Io=100mA	—	0.7	1.4	V
	V_{OL3}			Vcc=5V, Io=1mA	—	0.69	1.0	V
	V_{OL4}			Vcc=5V, Io=100mA	—	1.3	2.0	V
	V_{OH1}	Output high voltage		Vcc=18V, Io=-10mA	16.0	16.5	—	V
	V_{OH2}			Vcc=18V, Io=-100mA	15.5	16.0	—	V
	T_{RISE}	Output voltage rise time		No load	—	50	—	ns
	T_{FALL}	Output voltage fall time		No load	—	35	—	ns

TYPICAL CHARACTERISTICS

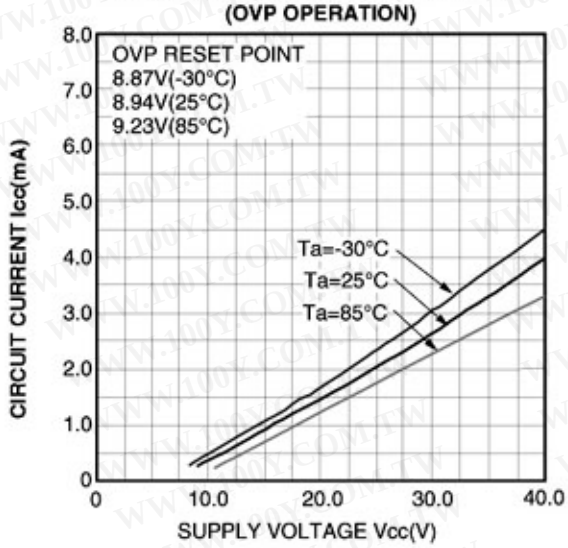
THERMAL DERATING
(MAXIMUM RATING)



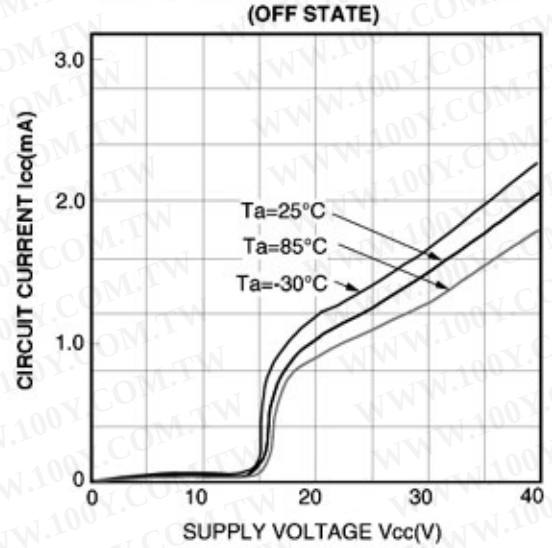
CIRCUIT CURRENT VS.SUPPLY VOLTAGE
(NORMAL OPERATION)



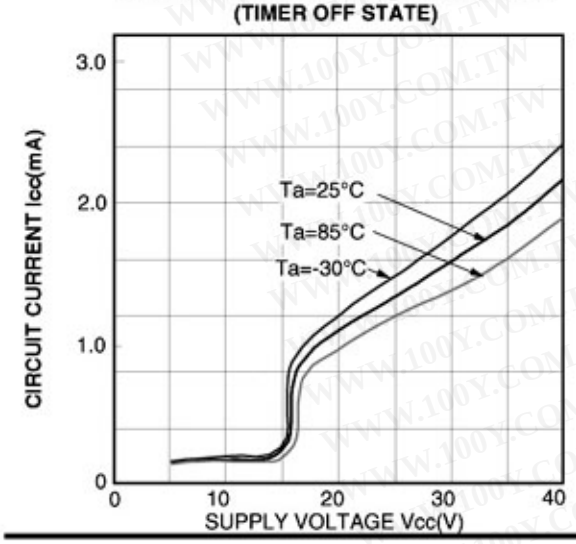
CIRCUIT CURRENT VS.SUPPLY VOLTAGE
(OVP OPERATION)



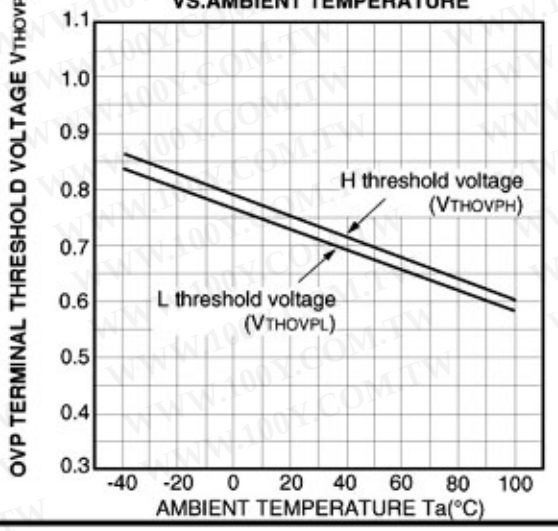
CIRCUIT CURRENT VS.SUPPLY VOLTAGE
(OFF STATE)



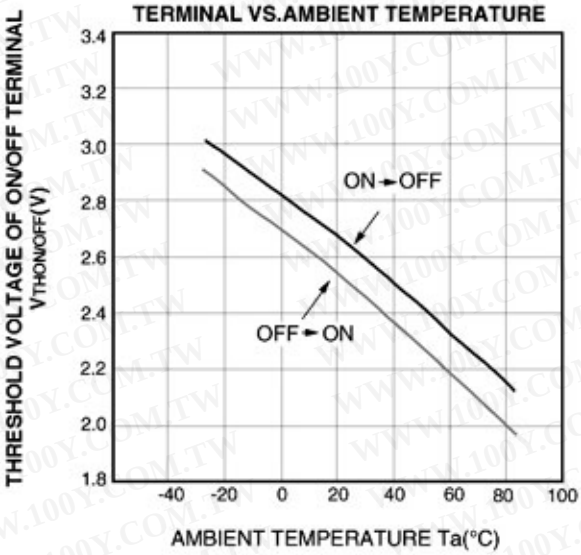
CIRCUIT CURRENT VS.SUPPLY VOLTAGE
(TIMER OFF STATE)



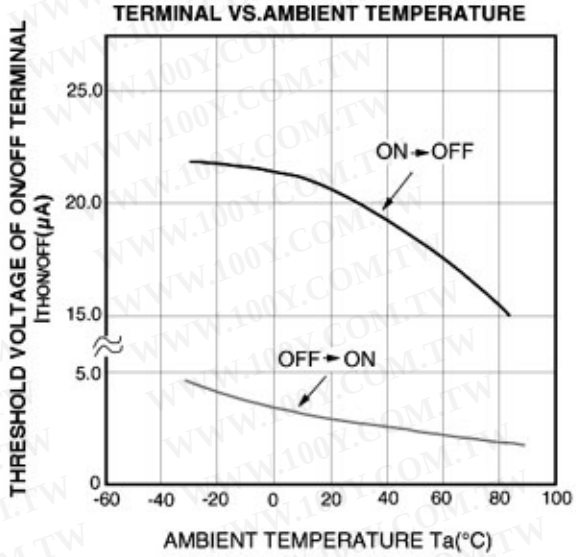
OVP TERMINAL THRESHOLD VOLTAGE
VS.AMBIENT TEMPERATURE



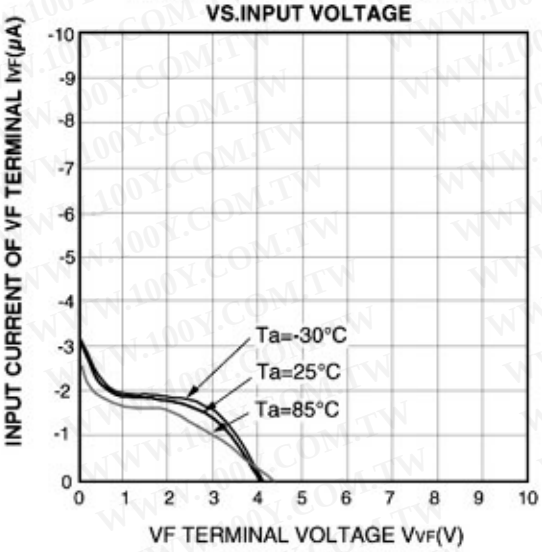
THRESHOLD VOLTAGE OF ON/OFF TERMINAL VS.AMBIENT TEMPERATURE



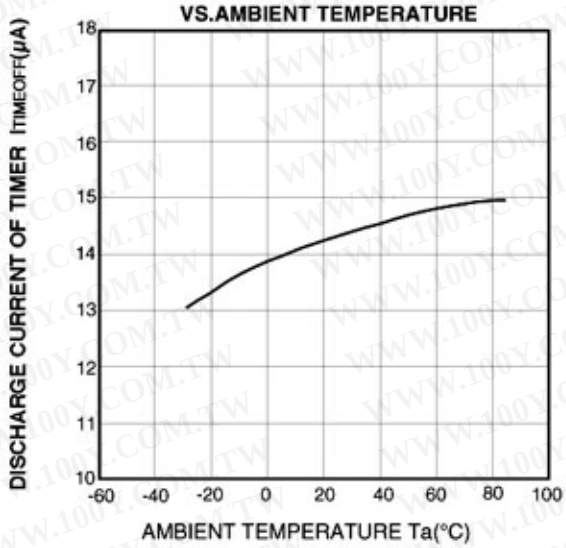
THRESHOLD VOLTAGE OF ON/OFF TERMINAL VS.AMBIENT TEMPERATURE



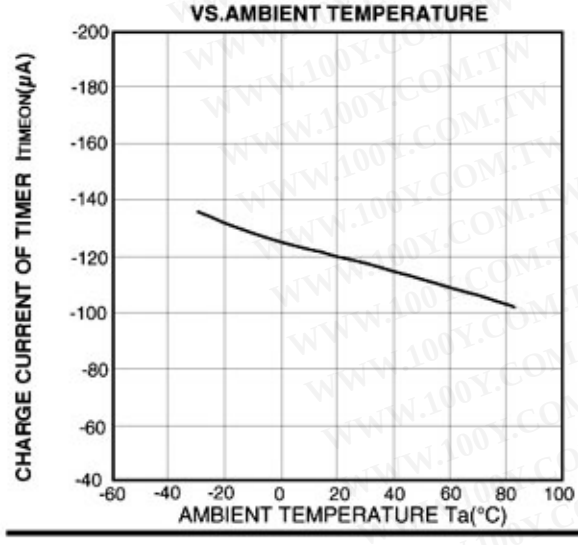
INPUT CURRENT OF VF TERMINAL VS.INPUT VOLTAGE



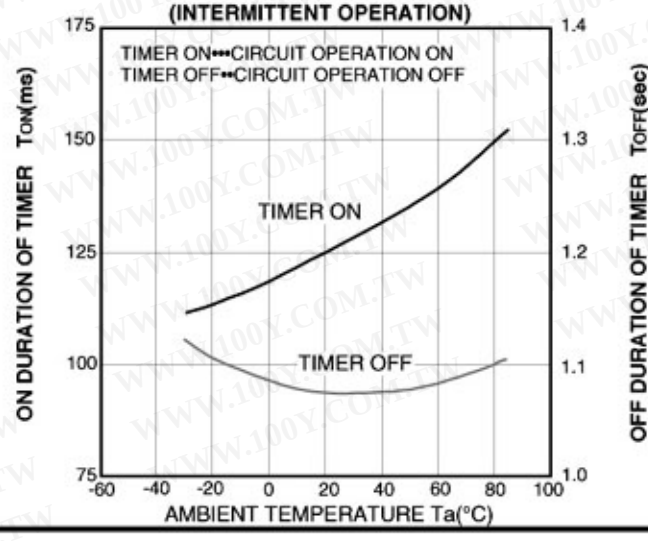
DISCHARGE CURRENT OF TIMER VS.AMBIENT TEMPERATURE



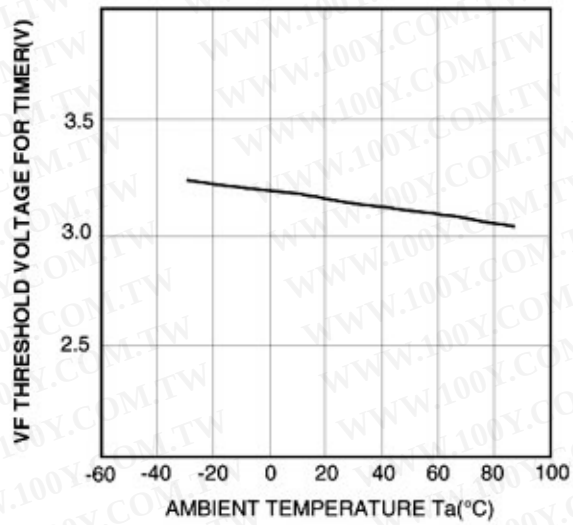
CHARGE CURRENT OF TIMER VS.AMBIENT TEMPERATURE



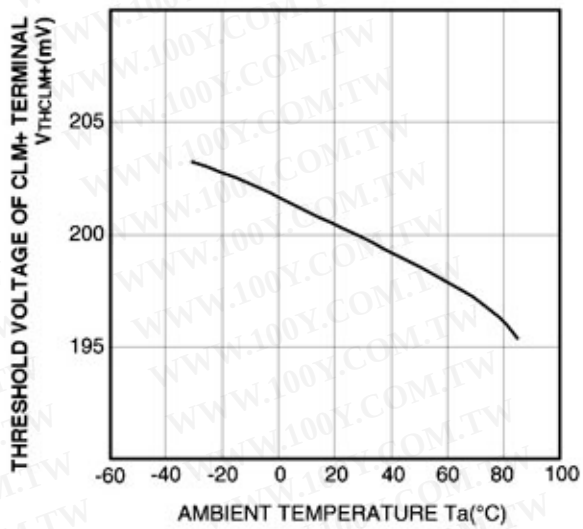
ON AND OFF DURATION OF TIMER VS.AMBIENT TEMPERATURE (INTERMITTENT OPERATION)



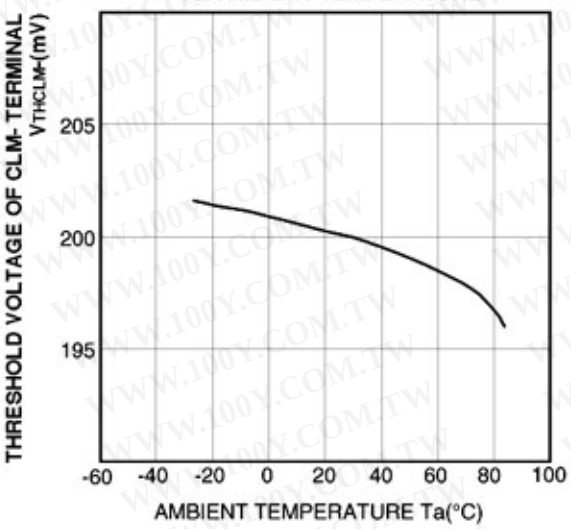
VF THRESHOLD VOLTAGE FOR TIMER VS. AMBIENT TEMPERATURE



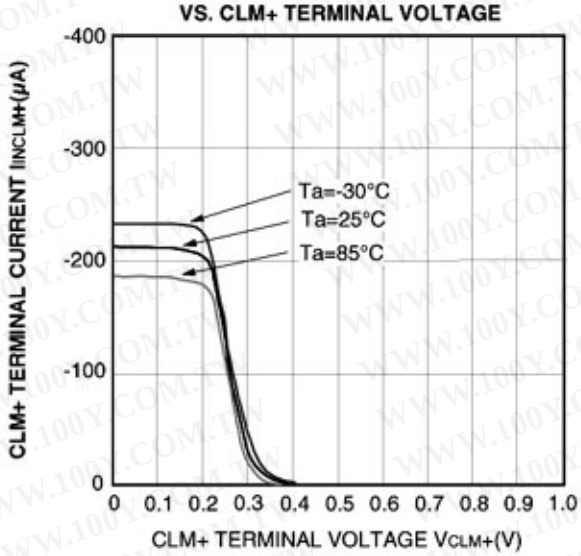
THRESHOLD VOLTAGE OF CLM+ TERMINAL VS. AMBIENT TEMPERATURE



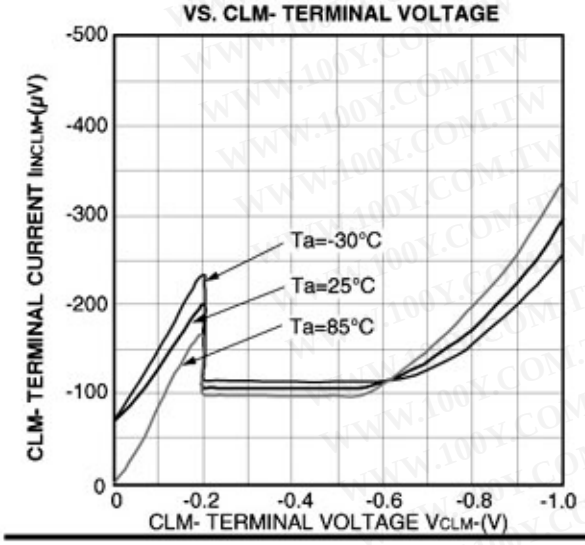
THRESHOLD VOLTAGE OF CLM- TERMINAL VS. AMBIENT TEMPERATURE



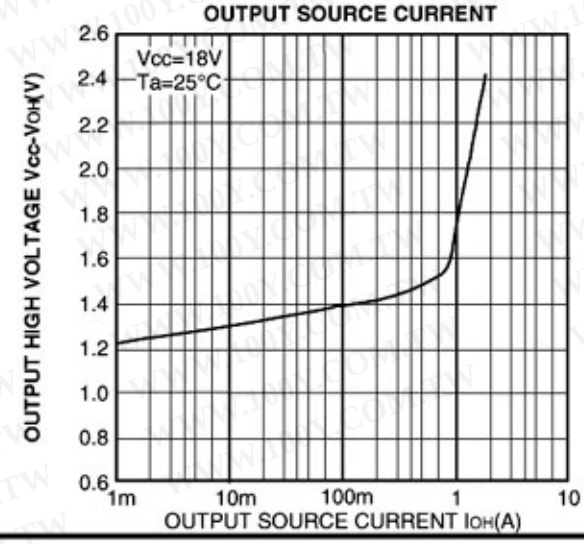
CLM+ TERMINAL CURRENT VS. CLM+ TERMINAL VOLTAGE



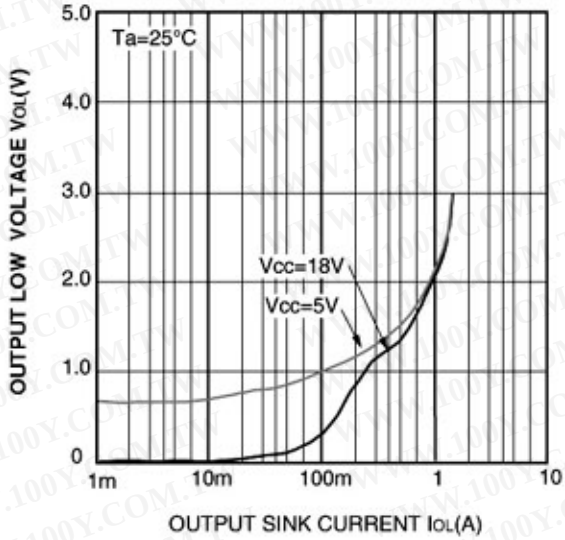
CLM- TERMINAL CURRENT VS. CLM- TERMINAL VOLTAGE



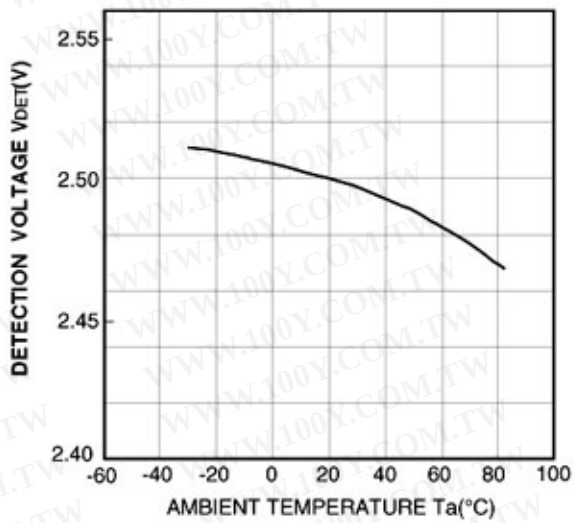
OUTPUT HIGH VOLTAGE VS. OUTPUT SOURCE CURRENT



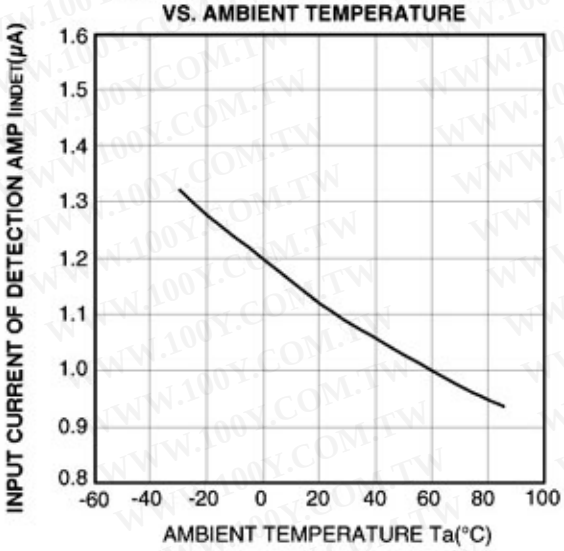
OUTPUT LOW VOLTAGE
VS. OUTPUT SINK CURRENT



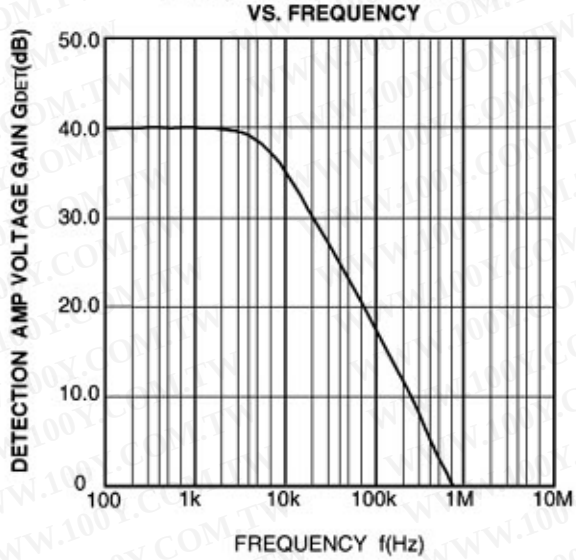
DETECTION VOLTAGE
VS. AMBIENT TEMPERATURE



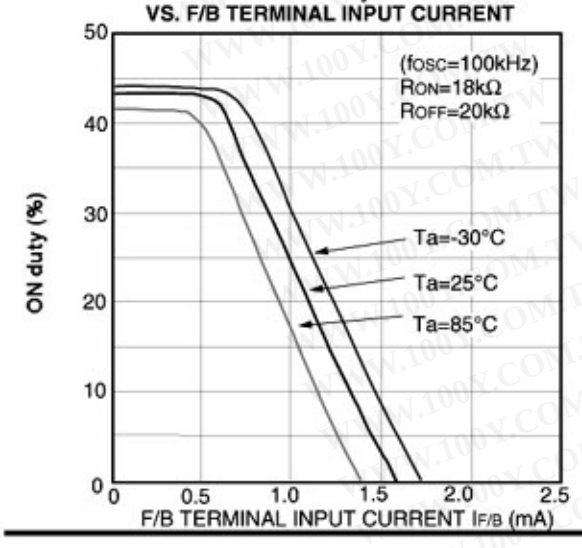
INPUT CURRENT OF DETECTION AMP
VS. AMBIENT TEMPERATURE



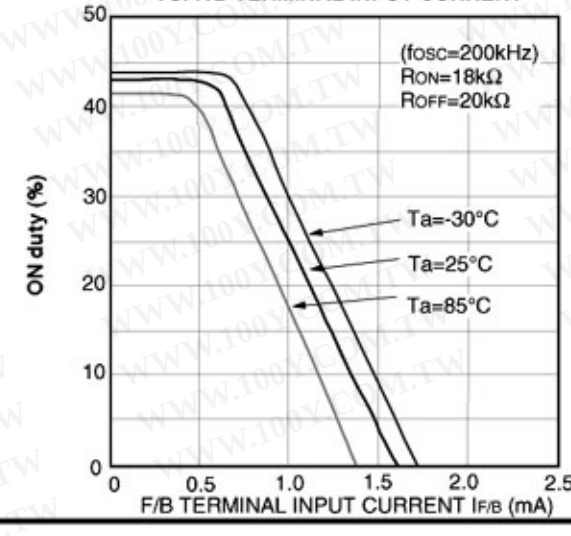
DETECTION AMP VOLTAGE GAIN
VS. FREQUENCY



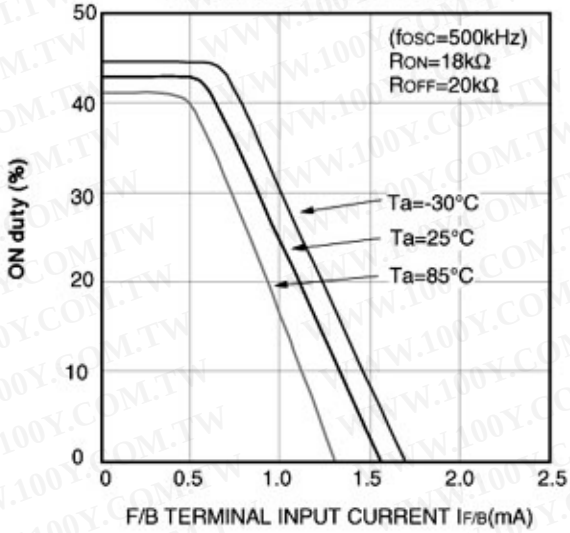
ON duty
VS. F/B TERMINAL INPUT CURRENT



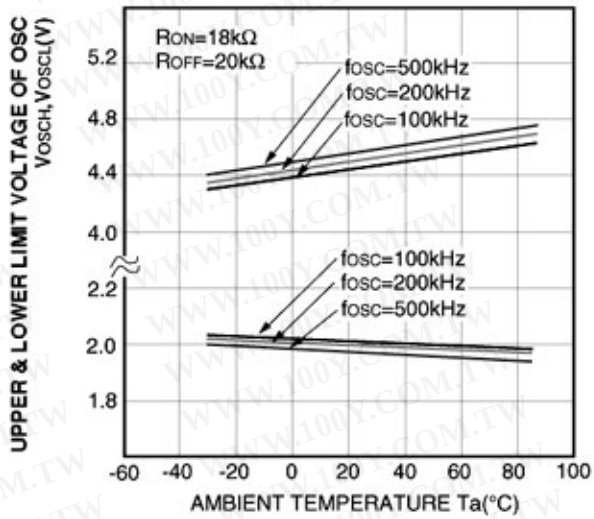
ON duty
VS. F/B TERMINAL INPUT CURRENT



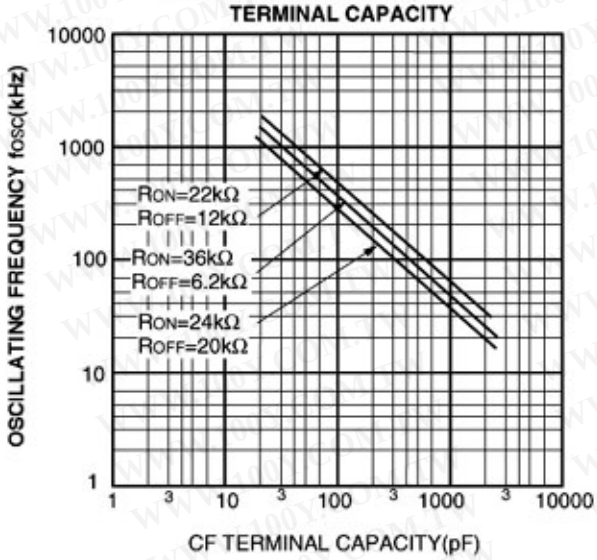
ON duty VS.
F/B TERMINAL INPUT CURRENT



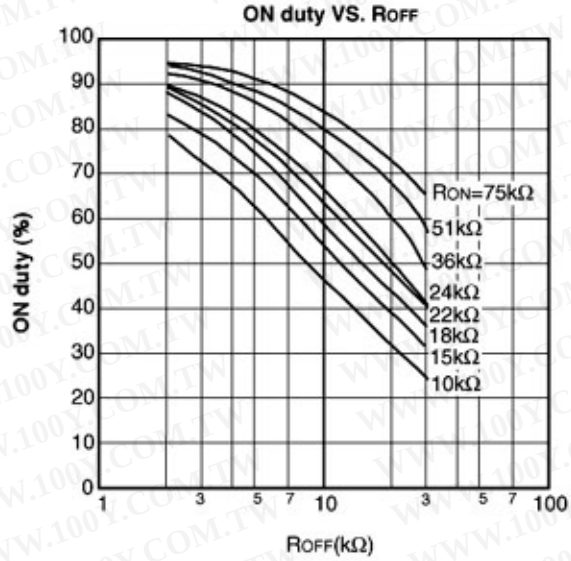
UPPER & LOWER LIMIT VOLTAGE OF OSC
VS. AMBIENT TEMPERATURE



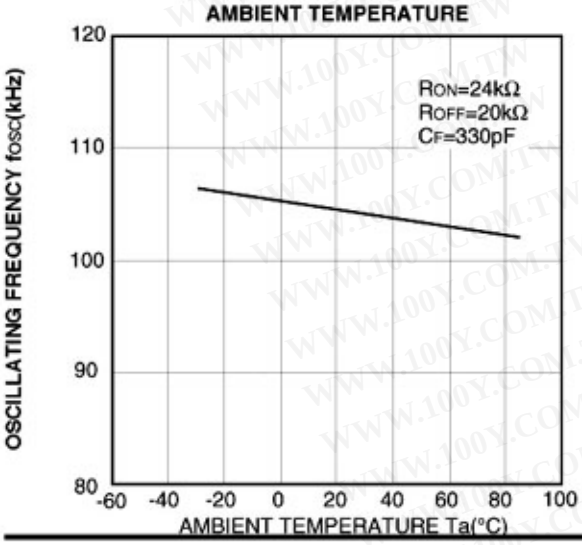
OSCILLATING FREQUENCY VS. CF
TERMINAL CAPACITY



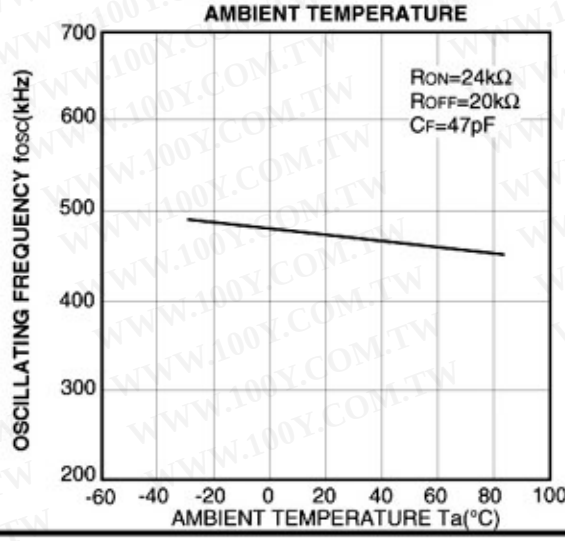
ON duty VS. ROFF



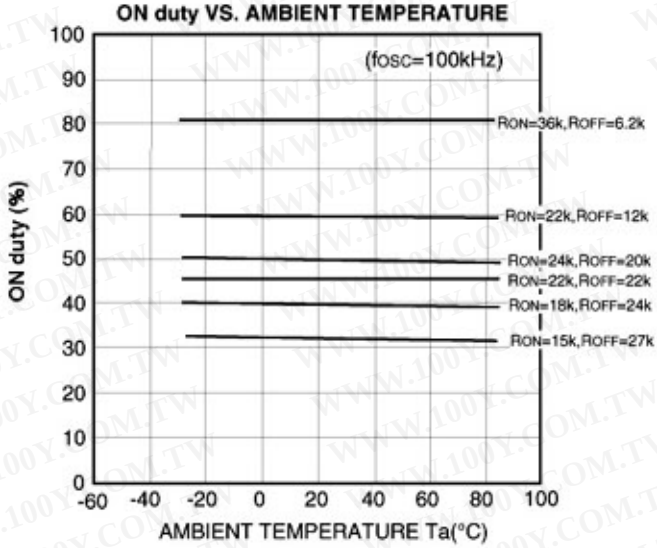
OSCILLATING FREQUENCY VS.
AMBIENT TEMPERATURE



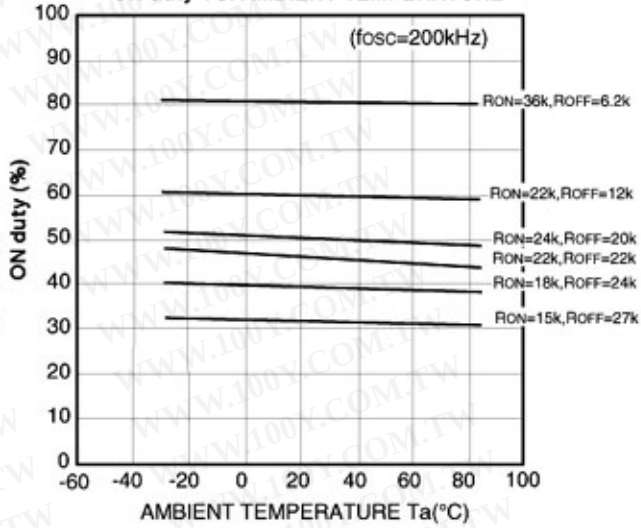
OSCILLATING FREQUENCY VS.
AMBIENT TEMPERATURE



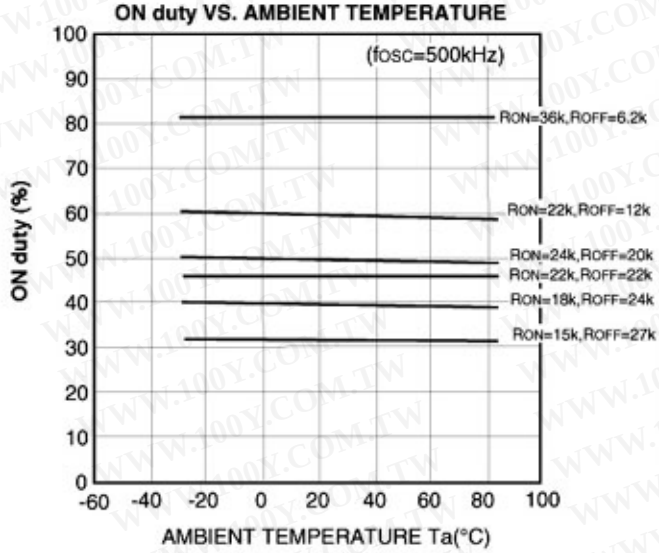
ON duty VS. AMBIENT TEMPERATURE



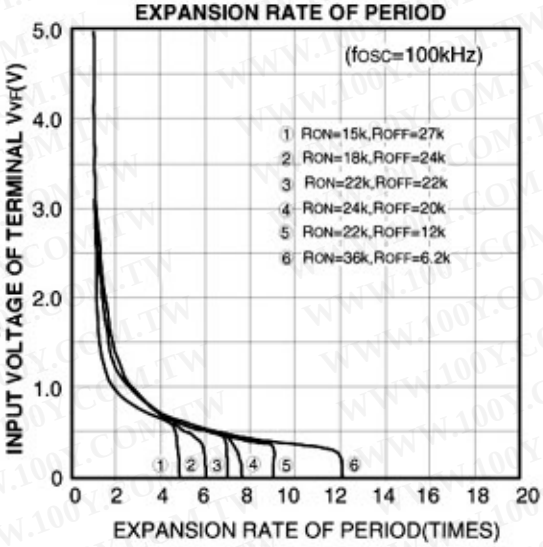
ON duty VS. AMBIENT TEMPERATURE



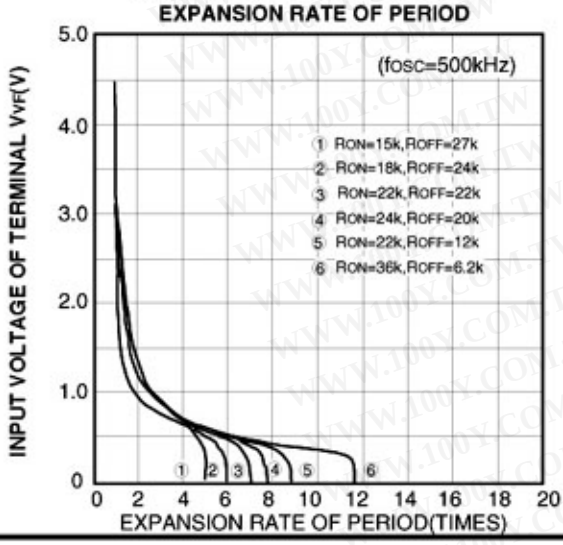
ON duty VS. AMBIENT TEMPERATURE



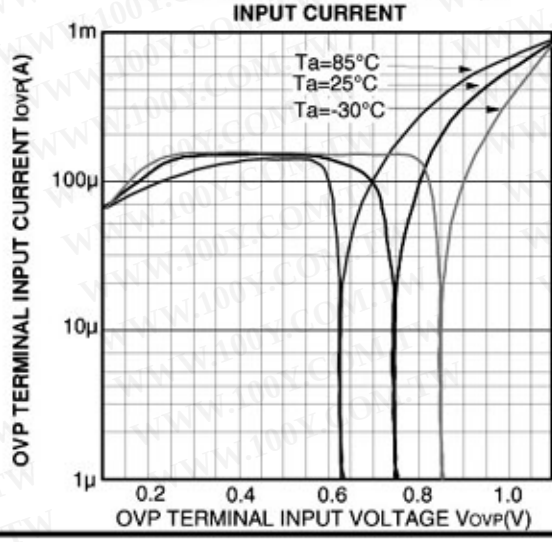
INPUT VOLTAGE OF TERMINAL VS. EXPANSION RATE OF PERIOD

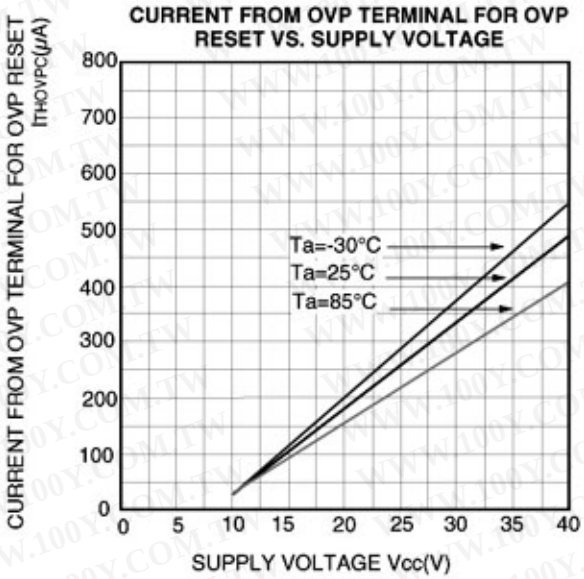


INPUT VOLTAGE OF TERMINAL VS. EXPANSION RATE OF PERIOD



OVP TERMINAL INPUT VOLTAGE VS. INPUT CURRENT




CURRENT FROM OVP TERMINAL FOR OVP RESET VS. SUPPLY VOLTAGE
CURRENT FROM OVP TERMINAL FOR OVP RESET ITHOVPC(μA)
800
700
600
500
400
300
200
100
0
0
5
10
15
20
25
30
35
40
Ta=-30°C
Ta=25°C
Ta=85°C
SUPPLY VOLTAGE Vcc(V)

FUNCTION DESCRIPTION

Type M51995AP and M51995AFP are especially designed for off-line primary PWM control IC of switching mode power supply (SMPS) to get DC voltage from AC power supply.
Using this IC,smart SMPS can be realized with reasonable cost and compact size as the number of external electric parts can be reduced and also parts can be replaced by reasonable one.
In the following circuit diagram,MOS-FIT is used for output transistor,however bipolar transistor can be used with no problem.

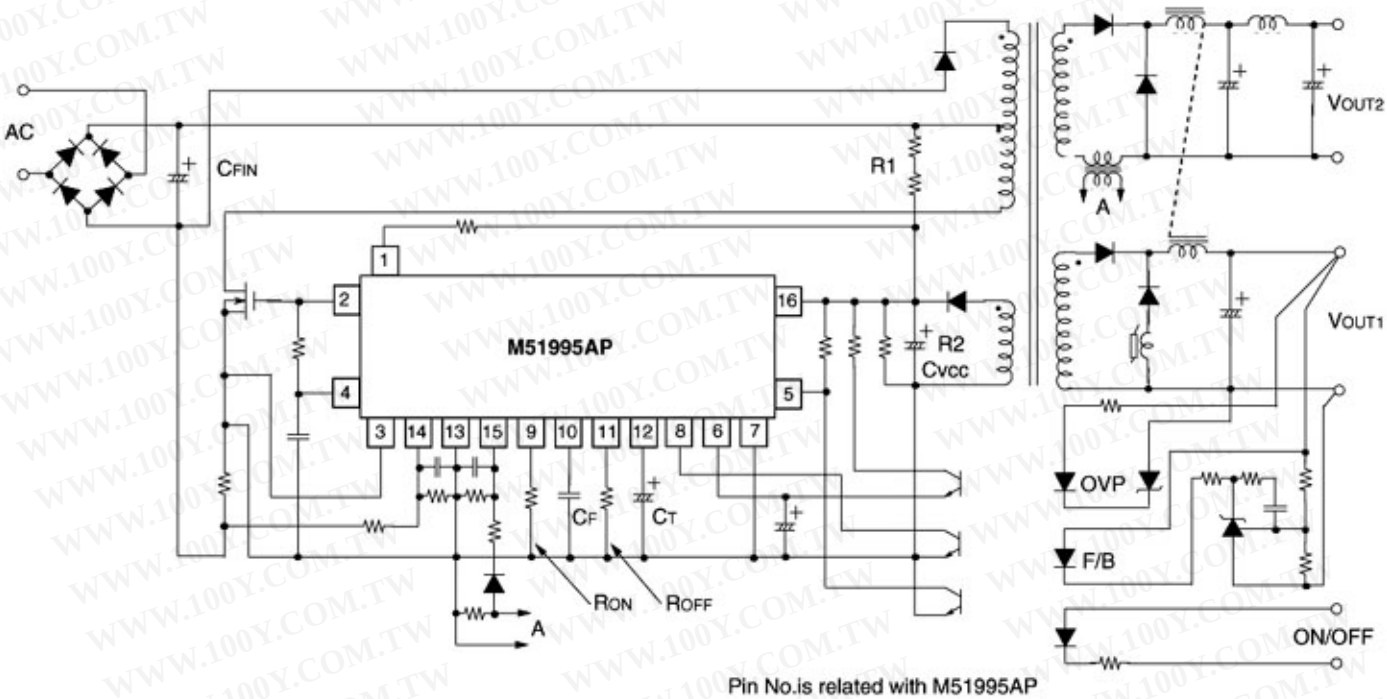


Fig.1 Example application circuit diagram of feed forward regulator

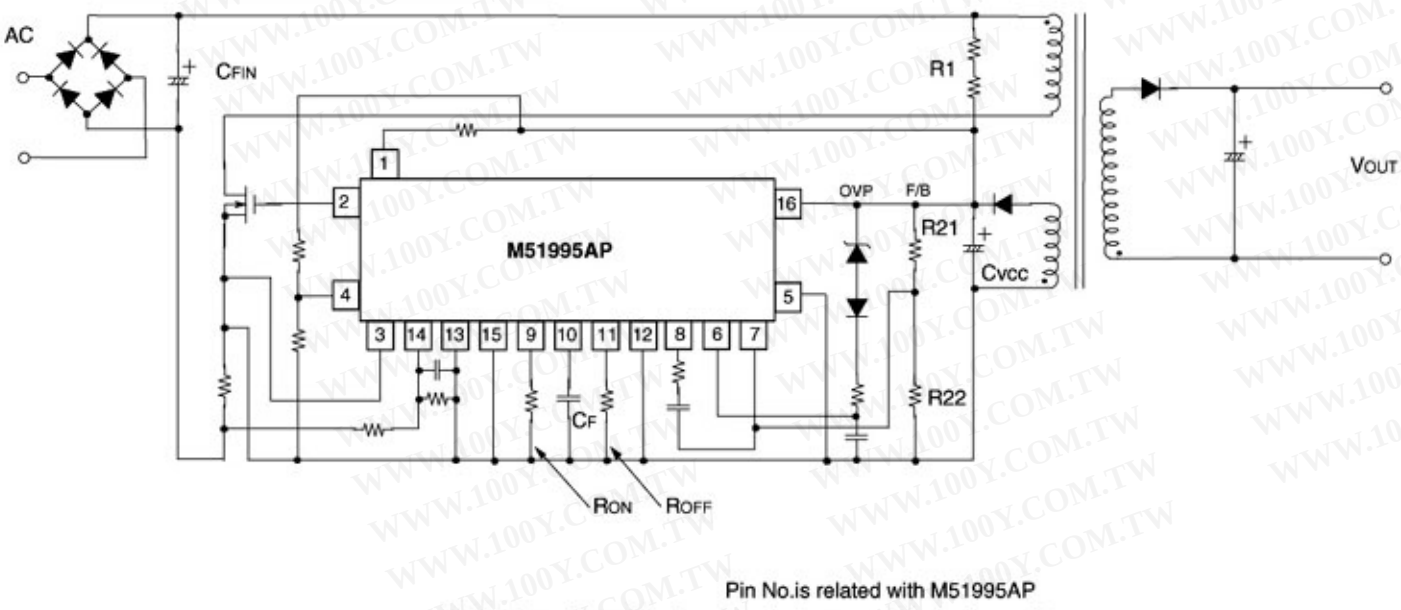


Fig.2 Example application circuit diagram of fly-back regulator

Start-up circuit section

The start-up current is such low current level as typical 90μA,as shown in Fig.3,when the Vcc voltage is increased from low level to start-up voltage $V_{CC(START)}$.
In this voltage range,only a few parts in this IC,which has the function to make the output voltage low level,is alive and Icc current is used to keep output low level.The large voltage difference between $V_{CC(START)}$ and $V_{CC(STOP)}$ makes start-up easy,because it takes rather long duration from $V_{CC(START)}$ to $V_{CC(STOP)}$.

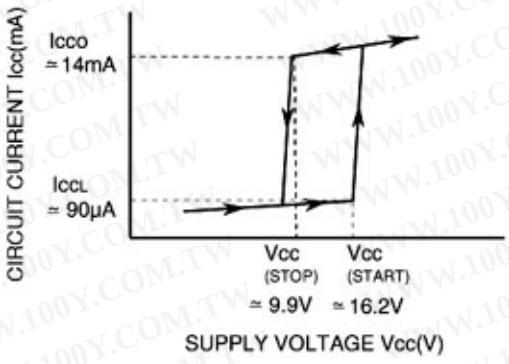


Fig.3 Circuit current vs.supply voltage

Oscillator section

The oscillation waveform is the triangle one.The ON-duration of output pulse depends on the rising duration of the triangle waveform and dead-time is decided by the falling duration.
The rising duration is determined by the product of external resistor R_{ON} and capacitor C_F and the falling duration is mainly determined by the product of resistor R_{OFF} and capacitor C_F.

(1)Oscillator operation when intermittent action and OSC control circuit does not operate

Fig.4 shows the equivalent charging and discharging circuit diagram of oscillator when the current limiting circuit does not operate.It means that intermittent action and OSC control circuit does not operate.
The current flows through R_{ON} from the constant voltage source of 5.8V.C_F is charged up by the same amplitude as R_{ON} current,when internal switch SW1 is switched to "charging side".The rise rate of C_F terminal is given as

$$\simeq \frac{V_{T\,-\,ON}}{R_{ON} \times C_F} \text{ (V/s)} \quad \text{.....(1)}$$

where $V_{T\,-\,ON} \simeq 4.5V$

The maximum on duration is approximately given as

$$\simeq \frac{(V_{OSCH}-V_{OSCL}) \times R_{ON} \times C_F}{V_{T\,-\,ON}} \text{ (s)} \quad \text{.....(2)}$$

where $V_{OSCH} \simeq 4.4V$
$V_{OSCL} \simeq 2.0V$

C_F is discharged by the summed-up of R_{OFF} current and one sixteenth (1/16) of R_{ON} current by the function of Q2,Q3 and Q4 when SW1,SW2 are switched to "discharge side".

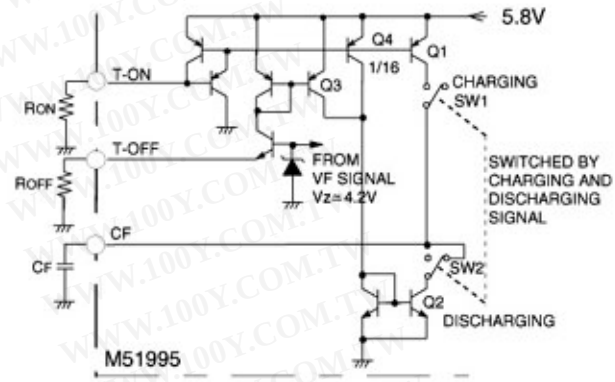


Fig.4 Schematic diagram of charging and discharging control circuit for OSC.capacitor C_F

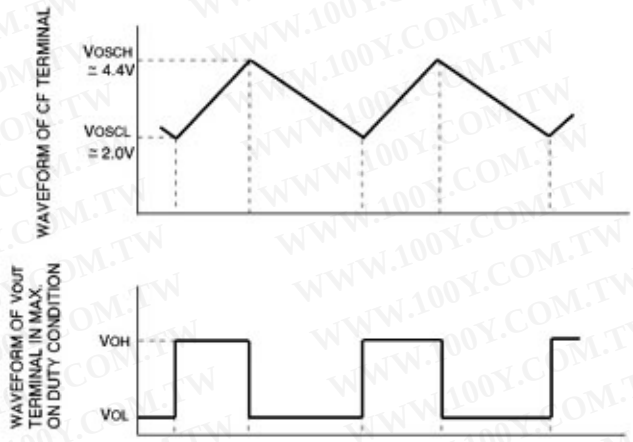


Fig.5 OSC.waveform at normal condition (no-operation of intermittent action and OSC.control circuit)

So fall rate of CF terminal is given as

$$\simeq \frac{V_{T\,-\,OFF}}{R_{OFF} \times C_F} + \frac{V_{T\,-\,ON}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \text{.....(3)}$$

The minimum off duration approximately is given as

$$\simeq \frac{(V_{OSCH}-V_{OSCL}) \times C_F}{\frac{V_{T-OFF}}{R_{OFF}} + \frac{V_{T-ON}}{16 \times R_{ON}}} \text{ (s)} \quad \text{.....(4)}$$

where $V_{T\,-\,OFF} \simeq 3.5V$

The cycle time of oscillation is given by the summation of Equations 2 and 4.
The frequency including the dead-time is not influenced by the temperature because of the built-in temperature compensating circuit.

(2)Oscillator operation when intermittent action and OSC control circuit operates.

When over current signal is applied to CLM+ or CLM- terminal,and the current limiting circuit,intermittent action and OSC control circuit starts to operate.In this case T-OFF terminal voltage depends on VF terminal voltage,so the oscillation frequency decreases and dead-time spreads.

The rise rate of oscillation waveform is given as

$$\simeq \frac{V_{T\text{-}ON}}{R_{ON} \times C_F} \text{ (V/s)} \quad \text{.....(5)}$$

The fall rate of oscillation waveform is given as

$$\simeq \frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \text{.....(6)}$$

where $V_{T\text{-}ON} \simeq 4.5V$

V_{VF};V_F terminal voltage

$V_{VFO} \simeq 0.4V$

V_{VF}-V_{FO}=0 if V_{VF}-V_{VFO}<0

V_{VF}-V_{VFO}=$V_{T\text{-}OFF}$ if V_{VF}-V_{VFO}>$V_{T\text{-}OFF} \simeq 3.5V$

So when V_{VF}>3.5V,the operation is just same as that in the no current limiting operation state.
The maximum on-duration is just same as that in the no-operation state of intermittent and oscillation control circuit and is given as follows;

$$\simeq \frac{(V_{OSCH} - V_{OSCL}) \times R_{OFF} \times C_F}{V_{T\text{-}ON}} \text{ (s)} \quad \text{.....(7)}$$

The minimum off-duration is approximately given as;

$$\simeq \frac{(V_{OSCH} - V_{OSCL}) \times C_F}{\frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F}} \text{ (s)} \quad \text{.....(8)}$$

The oscillation period is given by the summation of Equation(7) and (8).
As shown in Fig.7,the internal circuit kills the first output pulse in the output waveform.The output waveform will appear from the second pulse cycle because the duration of first cycle takes C_F charging time longer comparing with that at the stable operating state.
Usually the applied voltage to VF terminal must be proportional the output voltage of the regulator.
So when the over current occurs and the output voltage of the regulator becomes low,the off-duration becomes wide.
There are two methods to get the control voltage,which depends on the output voltage,on primary side.For the fly back type regulator application,the induced voltage on the third or bias winding is dependent on output voltage.On the other hand,for the feed forward type regulator application,it can be used that the output voltage depends on the product of induced voltage and "on-duty",as the current of choke coil will continue at over load condition,it means the "continuous current" condition.
Fig.8 shows one of the examples for VF terminal application for the feed forward type regulator.

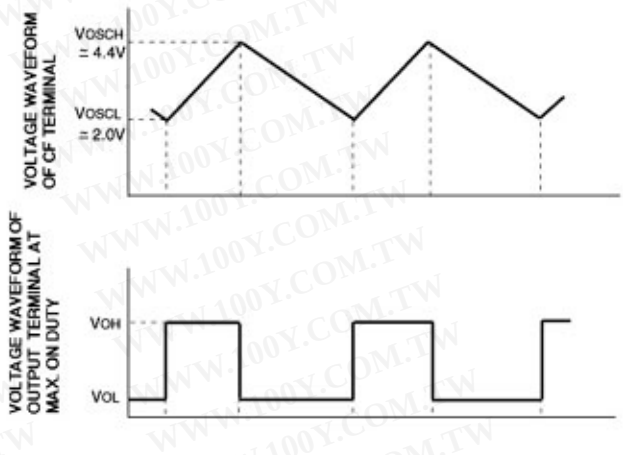


Fig.6 OSC.waveform with operation of intermittent and OSC.control circuit operation

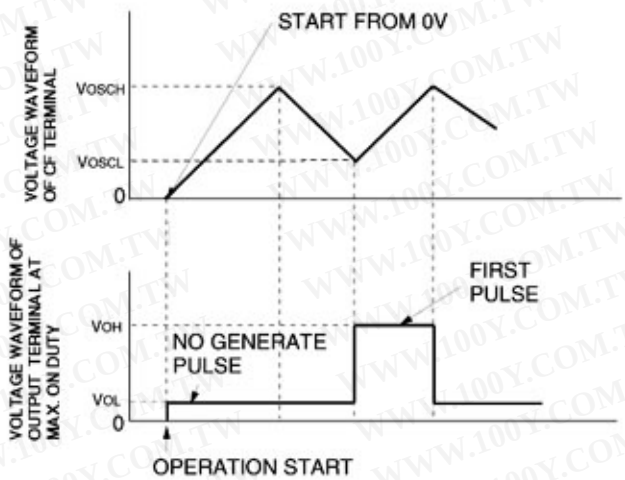


Fig.7 Relation between OSC. and output waveform circuit operation at start up

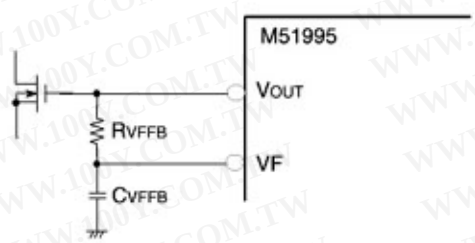


Fig.8 Feedback loop with low pass filter from output to VF terminal

choke coil will continue at over load condition,it means the "continuous current" condition.
Fig.8 shows one of the examples for VF terminal application for the feed forward type regulator.

PWM comparator and PWM latch section

Fig.9 shows the PWM comparator and latch section. The on-duration of output waveform coincides with the rising duration of CF terminal waveform,when the infinitive resistor is connected between F/B terminal and GND.
When the F/B terminal has finite impedance and current flows out from F/B terminal,"A" point potential shown in Fig.9 depends on this current.So the "A" point potential is close to GND level when the flow-out current becomes large.
"A" point potential is compared with the CF terminal oscillator waveform and PWM comparator,and the latch circuit is set when the potential of oscillator waveform is higher than "A" point potential.
On the other hand,this latch circuit is reset by high level signal during the dead-time of oscillation(falling duration of oscillation waveform).So the "B" point potential or output waveform of latch circuit is the one shown in Fig.10.
The final output waveform or "C" point potential is got by combining the "B" point signal and dead-time signal logically.(please refer to Fig.10)

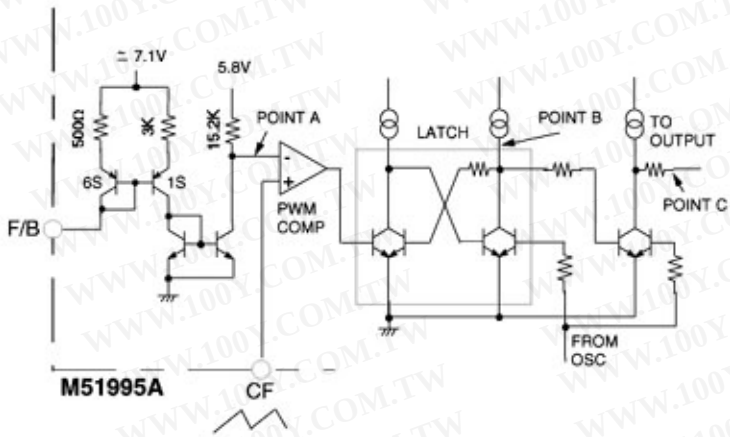


Fig.9 PWM comparator and latch circuit

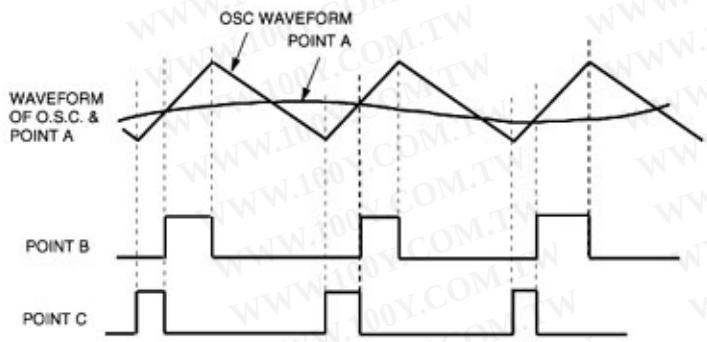
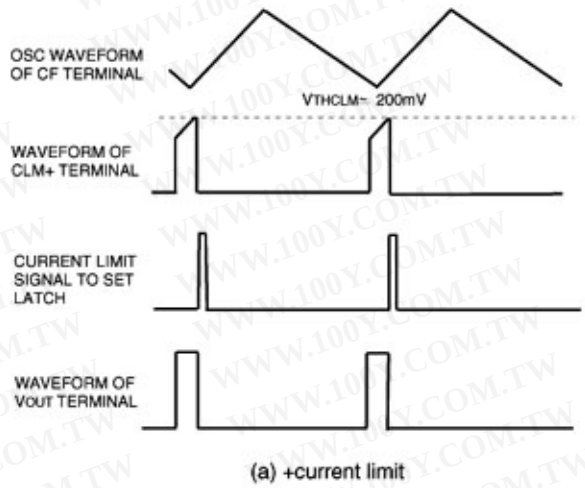


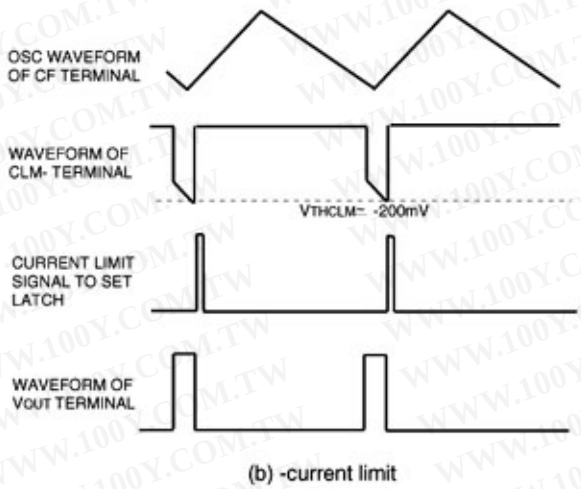
Fig.10 Waveforms of PWM comparator input point A, latch circuit points B and C

Current limiting section

When the current-limit signal is applied before the crossing instant of "A" pint potential and CF terminal voltage shown in Fig.9,this signal makes the output "off" and the off state will continue until next cycle.Fig.11 shows the timing relation among them.
The current limiting circuit has two input terminals,one has the detector-sensitivity of +200mV to the GND terminal and the other has -200mV.The circuit will be latched if the input signal is over the limit of either terminal.
If the current limiting circuit is set,no waveform is generated at output terminal however this state is reset during the succeeding dead-time.
So this current limiting circuit is able to have the function in every cycle,and is named "pulse-by-pulse current limit".



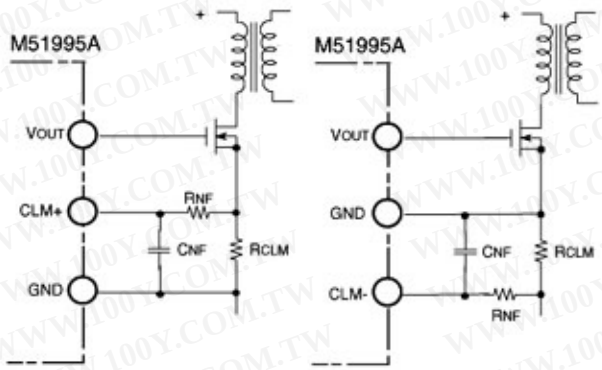
(a) +current limit



(b) -current limit

Fig.11 Operating waveforms of current limiting circuit

It is rather recommended to use not "CLM+" but "CLM-" terminal,as the influence from the gate drive current of MOS-FIT can be eliminated and wide voltage rating of + 4V to -4V is guaranteed for absolute maximum rating.
There happen some noise voltage on R_{CLM} during the switching of power transistor due to the snubber circuit and stray capacitor of the transformer windings.
To eliminate the abnormal operation by the noise voltage,the low pass filter,which consists of R_{NF} and C_{NF} is used as shown in Fig.12.
It is recommended to use 10 to 100Ω for R_{NF} because such range of R_{NF} is not influenced by the flow-out current of some 200μA from C_{LM} terminal and C_{NF} is designed to have the enough value to absorb the noise voltage.

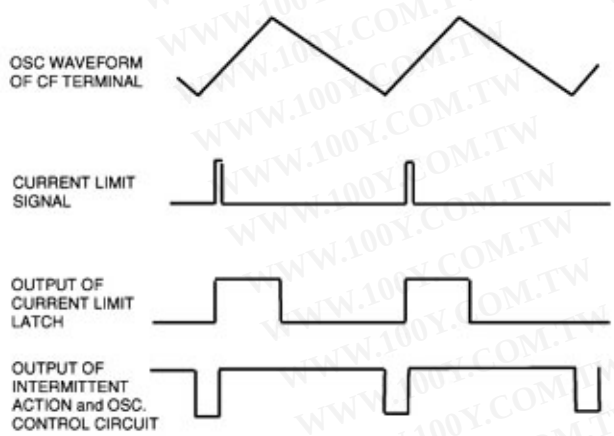


(a)In case of CLM+ (b)In case of CLM-

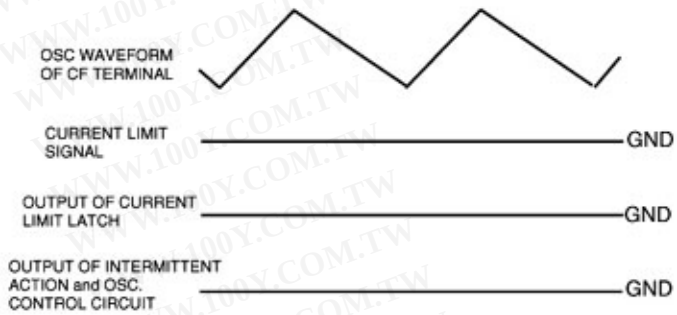
Fig.12 How to connect current limit circuit

Intermittent action and oscillation control section

When the internal current limiting circuit states to operate and also the VF level decreases to lower than the certain level of some 3V,the dead-time spreads and intermittent action and OSC control circuit(which is one of the timer-type-protection circuit)starts to operate.
The intermittent action and OSC control circuit is the one to generate the control signal for oscillator and intermittent action circuit.
Fig.13 shows the timing-chart of this circuit.When the output of intermittent action and oscillation control is at "high" level,the waveform of oscillator depends on the VF terminal voltage and the intermittent action circuit begins to operate.



(a) With current limit signal



(b) Without current limit signal

Fig.13 Timing chart of intermittent and OSC.control circuit

Intermittent action circuit section

Intermittent action circuit will start to operate when the output signal from the intermittent action and oscillation control circuit are "high" and also VF terminal voltage is lower than V_{THTIME} of about 3V.
Fig.14 shows the block diagram of intermittent action circuit.Transistor Q is on state when VF terminal voltage is higher than V_{THTIME} of about 3V,so the CT terminal voltage is near to GND potential.
When VF terminal voltage is lower than V_{THTIME},Q becomes "off" and the CT has the possibility to be charged up.
Under this condition,if the intermittent action and oscillation control signal become "high" the switch SWA will close only in this "high" duration and C_T is charged up by the current of 120μA through SW_A (SW_B is open) and CT terminal potential will rise.The output pulse can be generated only this duration.
When the CT terminal voltage reaches to 8V,the control logic circuit makes the SW_A "off" and SW_B "on",in order to flow in the $I_{TIMEOFF}$ of 15μA to CT terminal.
The IC operation will be ceased in the falling duration.
On the other hand,when CT terminal voltage decreases to lower than 2V,the IC operation will be reset to original state,as the control logic circuit makes the SW_A "on" and SW_B "off".
Therefore the parts in power circuit including secondary rectifier diodes are protected from the overheat by the over current.

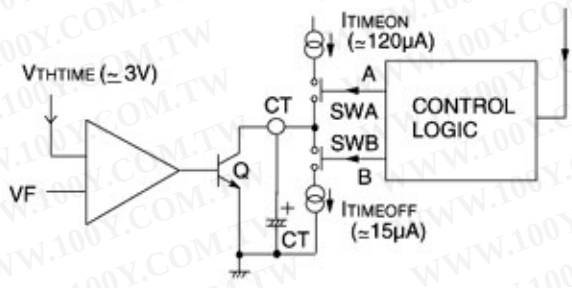


Fig.14 Block diagram of intermittent action circuit

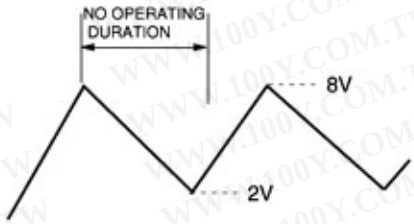


Fig.15 Waveform of CT terminal

Fig.16 shows the Icc versus Vcc in this timer-off duration.
In this duration the power is not supplied to IC from the third winding of transformer but through from the resistor R1 connected toVcc line.
If the R1 shown in Fig.1 and 2 is selected adequate value,Vcc terminal voltage will be kept at not so high or low but adequate value,as the Icc versus Vcc characteristics has such the one shown in Fig.16.

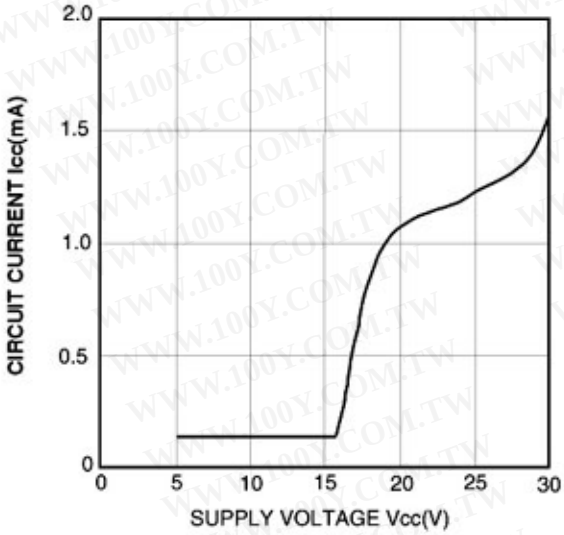


Fig.16 Icc vs.Vcc in timer-off duration of intermittent action circuit

To ground the CT terminal is recommended,when the intermittent mode is not used.
In this case the oscillated frequency will become low but the IC will neither stop the oscillation nor change to the intermittent action mode,when the current limit function becomes to operate and the VF terminal voltage becomes low.

Voltage detector circuit(DET) section

The DET terminal can be used to control the output voltage which is determined by the winding ratio of fly back transformer in fly-back system or in case of common ground circuit of primary and secondary in feed forward system.
The circuit diagram is quite similar to that of shunt regulator type 431 as shown in Fig.17.As well known from Fig.17 and Fig.18,the output of OP AMP has the current-sink ability,when the DET terminal voltage is higher than 2.5V but it becomes high impedance state when lower than 2.5V DET terminal and F/B terminal have inverting phase characteristics each other,so it is recommended to connect the resistor and capacitor in series between them for phase compensation.It is very important,one can not connect by resistor directly as there is the voltage difference between them and the capacitor has the DC stopper function.

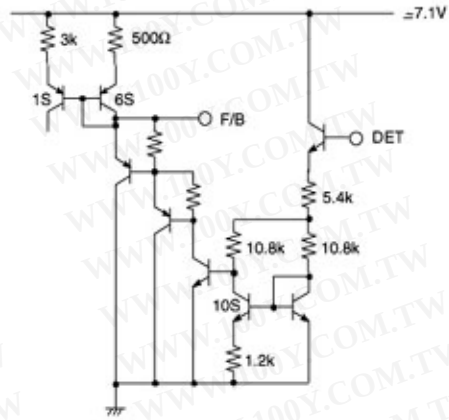


Fig.17 Equivalent circuit diagram of voltage detector

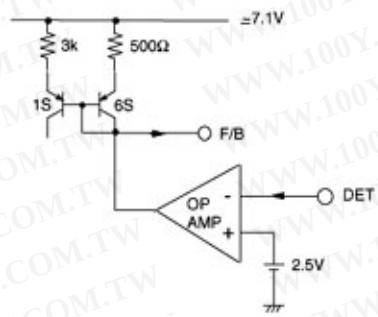


Fig.18 Equivalent circuit diagram of voltage detector

ON-OFF circuit section

Fig.19 shows the circuit diagram of ON-OFF circuit.The current flown into the ON-OFF terminal makes the Q4 "on" and the switching operation stop.On the other hand.the switching operation will recover as no current flown into ON/OFF terminal makes Q4 "off" As the constant current source connected to Q4 base terminal has such the hysteresis characteristics of 20μA at operation and 3μA at stopping.So the unstable operation is not appeared even if the ON/OFF terminal voltage signal varies slowly.

Fig.20 shows how to connect the ON/OFF terminal.The switching operation will stop by swich-off and operate by switch-on.
Transistor or photo transistor can be replaced by this switch,of course.No resistor of 30 to 100kΩ is connected and ON/OFF terminal is directly connected to GND,when it is not necessary to use the ON/OFF operation.
Fig.21 shows the Icc versus Vcc characteristics in OFF state and Vcc will be kept at not so high or low but at the adequate voltage,when R1 shown in Fig.1 and 2 is selected properly.

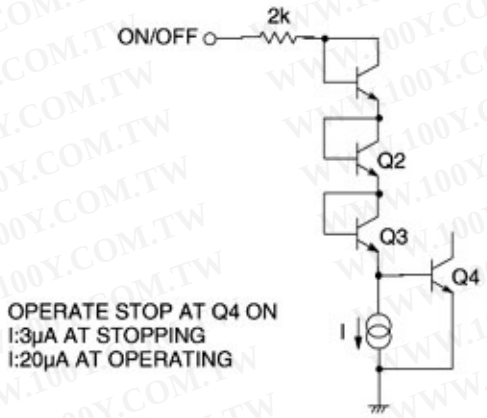


Fig.19 ON/OFF circuit

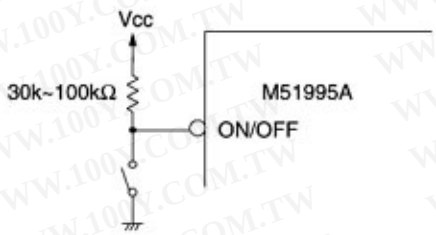


Fig.20 Connecting of ON/OFF terminal

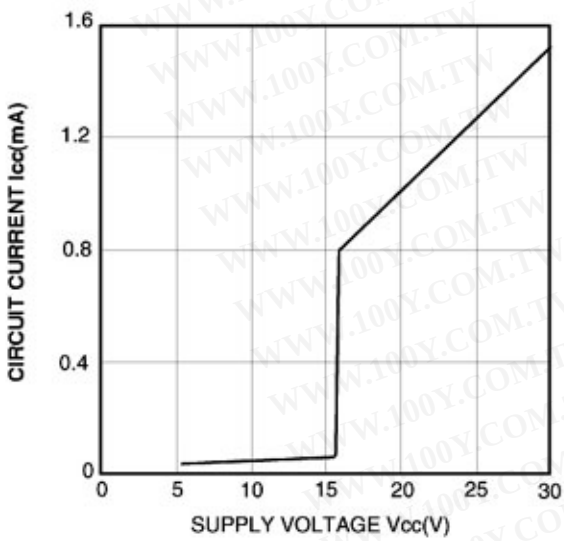


Fig.21 Icc vs.Vcc in OFF state

OVP circuit(over voltage protection circuit)section

OVP circuit is basically positive feedback circuit constructed by Q2,Q3 as shown in Fig.22.
Q2,Q3 turn on and the circuit operation of IC stops,when the input signal is applied to OVP terminal.(threshold voltage ≃ 750mV)
The current value of I2 is about 150μA when the OVP does not operates but it decreases to about 2μA when OVP operates.
It is necessary to input the sufficient larger current(800μA to 8mA)than I2 for triggering the OVP operation.
The reason to decrease I2 is that it is necessary that Icc at the OVP rest supply voltage is small.
It is necessary that OVP state holds by circuit current from R1 in the application example,so this IC has the characteristic of small Icc at the OVP reset supply voltage(≃stand-by current + 20μA)
On the other hand,the circuit current is large in the higher supply voltage,so the supply voltage of this IC doesn't become so high by the voltage drop across R1.
This characteristic is shown in Fig.23.
The OVP terminal input current in the voltage lower than the OVP threshold voltage is based on I2 and the input current in the voltage higher than the OVP threshold voltage is the sum of the current flowing to the base of Q3 and the current flowing from the collector of Q2 to the base.
For holding in the latch state,it is necessary that the OVP terminal voltage is kept in the voltage higher than V_{BE} of Q3.
So if the capacitor is connected between the OVP terminal and GND,even though Q2 turns on in a moment by the surge voltage,etc,this latch action does not hold if the OVP terminal voltage does not become higher than V_{BE} of Q3 by charging this capacitor.
For resetting OVP state,it is necessary to make the OVP terminal voltage lower than the OVP L threshold voltage or make Vcc lower than the OVP reset supply voltage.
As the OVP reset voltage is settled on the rather high voltage of 9.0V,SMPS can be reset in rather short time from the switch-off of the AC power source if the smoothing capacitor is not so large value.

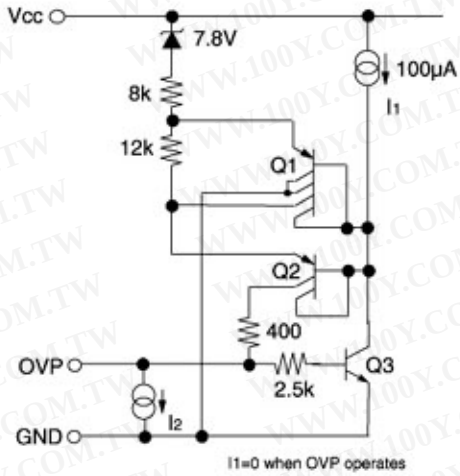


Fig.22 Detail diagram of OVP circuit

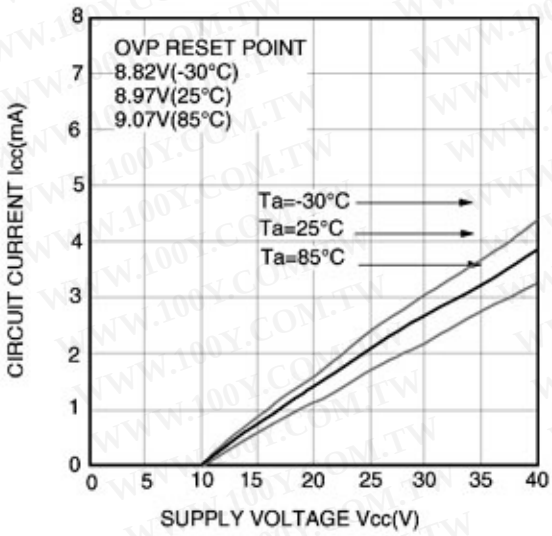


Fig.23 CIRCUIT CURRENT VS. SUPPLY VOLTAGE (OVP OPERATION)

Output section

It is required that the output circuit have the high sink and source abilities for MOS-FET drive.It is well known that the "totempole circuit has high sink and source ability.However,it has the demerit of high through current.
For example,the through current may reach such the high current level of 1A,if type M51995A has the "conventional" totempole circuit.For the high frequency application such as higher than 100kHz,this through current is very important factor and will cause not only the large Icc current and the inevitable heat-up of IC but also the noise voltage.
This IC uses the improved totempole circuit,so without deteriorating the characteristic of operating speed,its through current is approximately 100mA.

APPLICATION NOTE OF TYPE M51995AP/FP

Design of start-up circuit and the power supply of IC

(1)The start-up circuit when it is not necessary to set the start and stop input voltage

Fig.24 shows one of the example circuit diagram of the start-up circuit which is used when it is not necessary to set the start and stop voltage.
It is recommended that the current more than 300μA flows through R1 in order to overcome the operation start-up current $I_{CC(START)}$ and Cvcc is in the range of 10 to 47μF.The product of R1 by Cvcc causes the time delay of operation,so the response time will be long if the product is too much large.

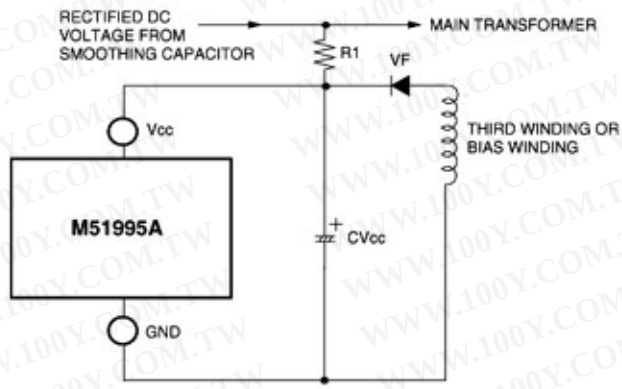


Fig.24 Start-up circuit diagram when it is not necessary to set the start and stop input voltage

Just after the start-up,the Icc current is supplied from Cvcc,however,under the steady state condition ,IC will be supplied from the third winding or bias winding of transformer,the winding ratio of the third winding must be designed so that the induced voltage may be higher than the operation-stop voltage $V_{CC(STOP)}$.
The Vcc voltage is recommended to be 12V to 17V as the normal and optimum gate voltage is 10 to 15V and the output voltage(V_{OH}) of type M51995AP/FP is about(Vcc-2V).

It is not necessary that the induced voltage is settled higher than the operation start-up voltage $V_{CC(START)}$,and the high gate drive voltage causes high gate dissipation,on the other hand,too low gate drive voltage does not make the MOS-FET fully on-state or the saturation state.

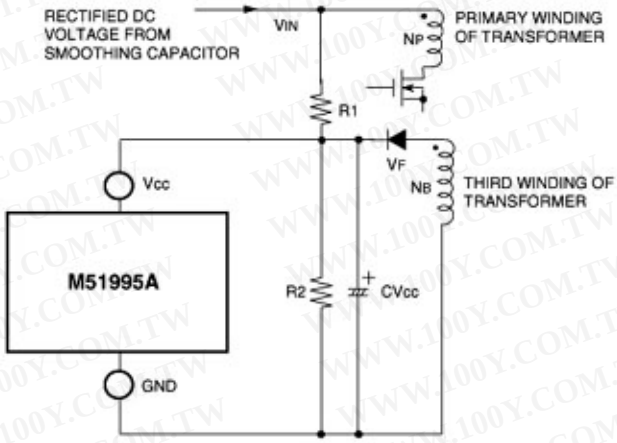


Fig.25 Start-up circuit diagram when it is not necessary to set the start and stop input voltage

(2)The start-up circuit when it is not necessary to set the start and stop input voltage

It is recommend to use the third winding of "forward winding" or "positive polarity" as shown in Fig.25,when the DC source voltages at both the IC operation start and stop must be settled at the specified values.
The input voltage($V_{IN(START)}$),at which the IC operation starts,is decided by R1 and R2 utilizing the low start-up current characteristics of type M51995AP/FP.
The input voltage($V_{IN(STOP)}$),at which the IC operation stops,is decided by the ratio of third winding of transformer.
The $V_{IN(START)}$ and $V_{IN(STOP)}$ are given by following equations.

$$V_{IN(START)} \simeq R1 \cdot I_{CCL} + \left(\frac{R1}{R2} + 1\right) \cdot V_{CC(START)} \quad \text{.....(9)}$$

$$V_{IN(STOP)} \simeq (V_{CC(STOP)} - V_F) \cdot \frac{N_P}{N_B} + \frac{1}{2} V'_{IN\ RIP(P-P)} \quad \text{.....(10)}$$

where

I_{CCL} is the operation start-up current of IC
$V_{CC(START)}$ is the operation start-up voltage of IC
$V_{CC(STOP)}$ is the operation stop voltage of IC
V_F is the forward voltage of rectifier diode
$V'_{IN(P-P)}$ is the peak to peak ripple voltage of

$$\text{Vcc terminal} \simeq \frac{N_B}{N_P} V'_{IN\ RIP(P-P)}$$

It is required that the $V_{IN(START)}$ must be higher than $V_{IN(STOP)}$. When the third winding is the "fly back winding" or "reverse polarity",the $V_{IN(START)}$ can be fixed,however,$V_{IN(STOP)}$ can not be settled by this system,so the auxiliary circuit is required.

(3)Notice to the Vcc,Vcc line and GND line

To avoid the abnormal IC operation,it is recommended to design the Vcc is not vary abruptly and has few spike voltage,which is induced from the stray capacity between the winding of main transformer.
To reduce the spike voltage,the Cvcc,which is connected between Vcc and ground,must have the good high frequency characteristics.
To design the conductor-pattern on PC board,following cautions must be considered as shown in Fig.26.
(a)To separate the emitter line of type M51995A from the GND line of the IC
(b)The locate the C_{VCC} as near as possible to type M51995A and connect directly
(c)To separate the collector line of type M51995A from the Vcc line of the IC
(d)To connect the ground terminals of peripheral parts of ICs to GND of type M51995A as short as possible

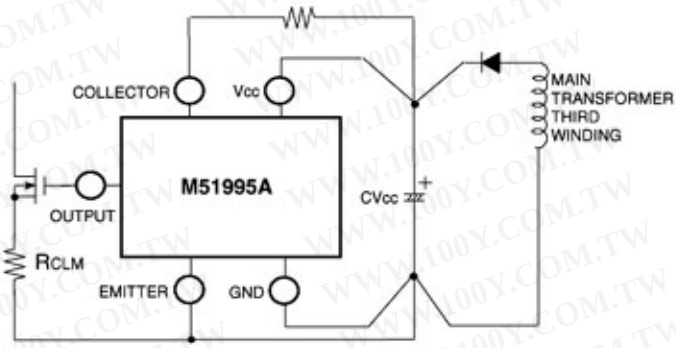


Fig.26 How to design the conductor-pattern of type M51995A on PC board(schematic example)

(4)Power supply circuit for easy start-up

When IC start to operate,the voltage of the C_{VCC} begins to decrease till the C_{VCC} becomes to be charged from the third winding of main-transformer as the Icc of the IC increases abruptly.In case shown in Fig.24 and 25,some "unstable start-up" or "fall to start-up" may happen, as the charging interval of C_{VCC} is very short duration;that is the charging does occur only the duration while the induced winding voltage is higher than the C_{VCC} voltage,if the induced winding voltage is nearly equal to the "operation-stop voltage" of type M51995.
It is recommended to use the 10 to 47μF for C_{VCC1},and about 5 times capacity bigger than C_{VCC1} for C_{VCC2} in Fig.27.

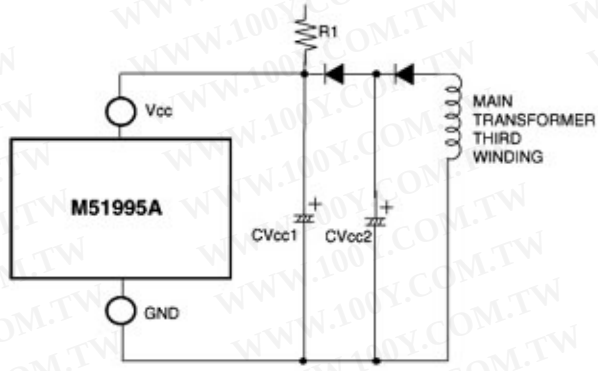


Fig.27 DC source circuit for stable start-up

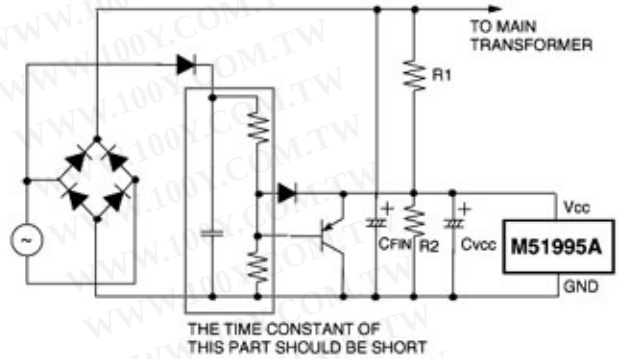


Fig.29 Example circuit diagram to make the OVP-reset-time fast

OVP circuit

(1)To avoid the miss operation of OVP

It is recommended to connect the capacitor between OVP terminal and GND for avoiding the miss operation by the spike noise.
The OVP terminal is connected with the sink current source (~150μA) in IC when OVP does not operate,for absorbing the leak current of the photo coupler in the application.
So the resistance between the OVP terminal and GND for leak-cut is not necessary.
If the resistance is connected,the supply current at the OVP reset supply voltage becomes large.
As the result,the OVP reset supply voltage may become higher than the operation stop voltage.
In that case,the OVP action is reset when the OVP is triggered at the supply voltage a little high than the operation stop voltage.
So it should be avoided absolutely to connect the resistance between the OVP terminal and GND.

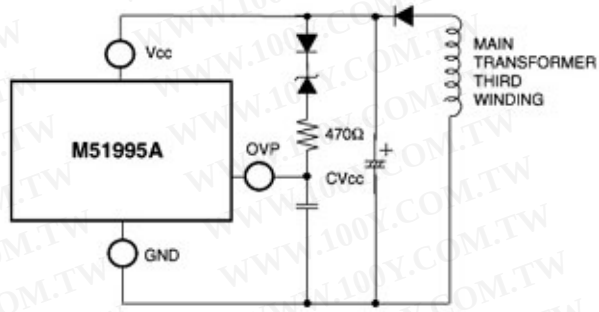


FIG.30 OVP setting method using the induced third winding voltage on fly back system

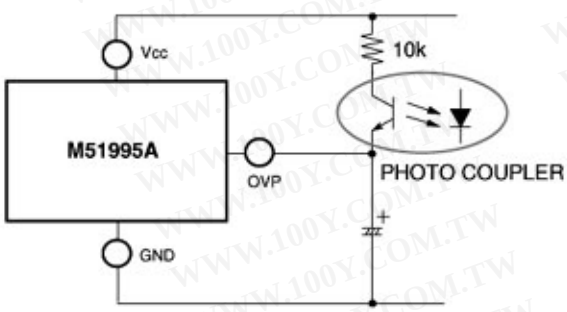


Fig.28 Peripheral circuit of OVP terminal

(2)Application circuit to make the OVP-reset time fast

The reset time may becomes problem when the discharge time constant of CFIN • (R1+R2) is long. Under such the circuit condition,it is recommended to discharge the CVCC forcedly and to make the Vcc low value.This makes the OVP-reset time fast.

(3)OVP setting method using the induced third winding voltage on fly back system

For the over voltage protection (OVP),the induced fly back type third winding voltage can be utilized,as the induced third winding voltage depends on the output voltage.Fig.30 shows one of the example circuit diagram.

Current limiting circuit

(1)Peripheral circuit of CLM+,CLM- terminal

Fig.31 and 32 show the example circuit diagrams around the CLM+ and CLM- terminal.It is required to connect the low pass filter,as the main current or drain current contains the spike current especially during the turn-on duration of MOS-FIT. 1,000pF to 22,000pF is recommended for C_{NF} and the R_{NF1} and R_{NF2} have the functions both to adjust the "current-detecting-sensitivity" and to consist the low pass filter.

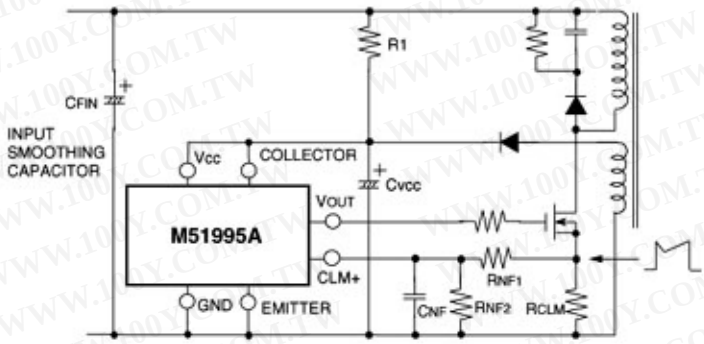


Fig.31 Peripheral circuit diagram of CLM+ terminal

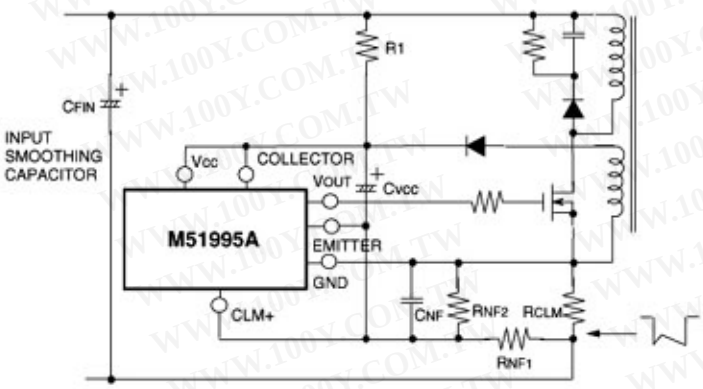


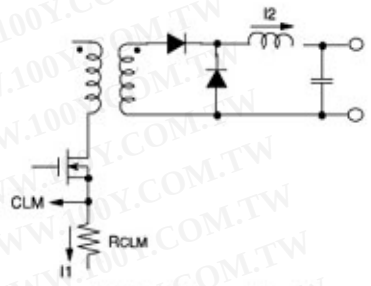
Fig.32 Peripheral circuit diagram of CLM- terminal

To design the R_{NF1} and R_{NF2},it is required to consider the influence of CLM terminal source current(I_{INCLM+} or I_{NFCLM-}), which value is in the range of 90 to 270μA.
In order to be not influenced from these resistor paralleled value of R_{NF1} and R_{NF2},(R_{NF1}/R_{NF2})is recommended to be less than 100Ω.
The R_{CLM} should be the non-inductive resistor.

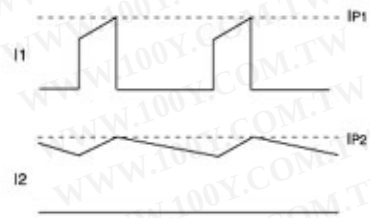
(2)Over current limiting curve

(a)In case of feed forward system

Fig.33 shows the primary and secondary current wave-forms under the current limiting operation.
At the typical application of pulse by pulse primary current detecting circuit,the secondary current depends on the primary current.As the peak value of secondary current is limited to specified value,the characteristics curve of output voltage versus output current become to the one as shown in Fig.34.



(a) Feed forward system



(b) Primary and secondary current

Fig.33 Primary and secondary current waveforms under the current limiting operation condition on feed forward system

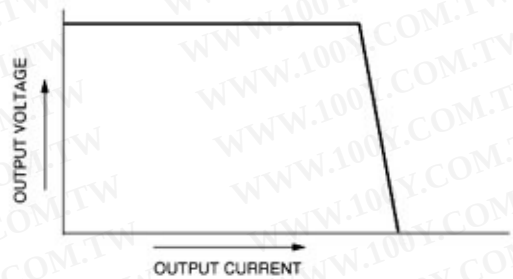


Fig.34 Over current limiting curve on feed forward system

The demerit of the pulse by pulse current limiting system is that the output pulse width can not reduce to less than some value because of the delay time of low pass filter connected to the CLM terminal and propagation delay time T_{PDCLM} from CLM terminal to output terminal of type M51995A.The typical T_{PDCLM} is 100ns.
As the frequency becomes higher,the delay time must be shorter.And as the secondary output voltage becomes higher,the dynamic range of on-duty must be wider;it means that it is required to make the on-duration much more narrower. So this system has the demerit at the higher oscillating frequency and higher output voltage applications.
To improve these points,the oscillating frequency is set low using the characteristics of VF terminal.When the current limiting circuit operates under the over current condition,the oscillating frequency decreases in accordance with the decrease of VF terminal voltage,if the VF is lower than 3.5V.And also the dead time becomes longer.

Under the condition of current limiting operation,the output current I2 continues as shown in Fig.33.So the output voltage depends on the product of the input primary voltage V_{IN} and the on-duty.
If the third winding polarity is positive ,the Vcc depends on V_{IN},so it is concluded that the smoothed voltage of V_{OUT} terminal depends on the output DC voltage of the SMPS.
So the sharp current limiting characteristics will be got,if the V_{OUT} voltage if feed back to VF terminal through low pass filter as shown in Fig.35.

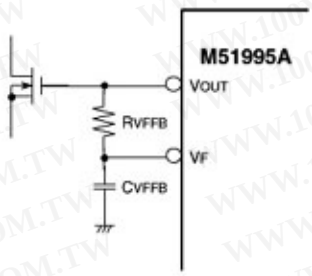


Fig.35 Feed back loop through low pass filter from V_{OUT} to V_F terminal

It is recommended to use 15kΩ for R_{VFFB},and 10,000pF for C_{VFFB} in Fig.35.
Fig.36 shows how to control the knee point where the frequency becomes decrease.

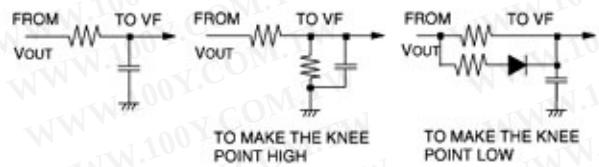


Fig.36 How to control the knee point

(b)In case of fly back system

The DC output voltage of SMPS depends on the Vcc voltage of type M51995A when the polarity of the third winding is negative and the system is fly back.So the operation of type M51995A will stop when the Vcc becomes lower than "Operation-stop voltage" of M51995A when the DC output voltage of SMPS decreases under specified value at over load condition.

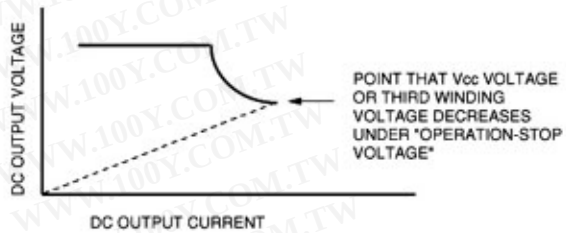


Fig.37 Over current limiting curve on fly back system

However,the M51995A will non-operate and operate intermittently,as the Vcc voltage rises in accordance with the decrease of Icc current.
The fly back system has the constant output power characteristics as shown in Fig.37 when the peak primary current and the operating frequency are constant.
To control the increase of DC output current,the operating frequency is decreased using the characteristics of VF terminal when the over current limiting function begins to operate.
The voltage which mode by dividing the Vcc is applied to VF terminal as shown in Fig.38,as the induced third winding voltage depends on the DC output voltage of SMPS.
15kΩ or less is recommended for R_2 in Fig.38,it is noticed that the current flows through R_1 and R_2 will superpose on the $I_{CC(START)}$ current.
If the R_1 is connected to Cvcc2 in Fig.27,the current flows through R_1 and R_2 is independent of the $I_{CC(START)}$.

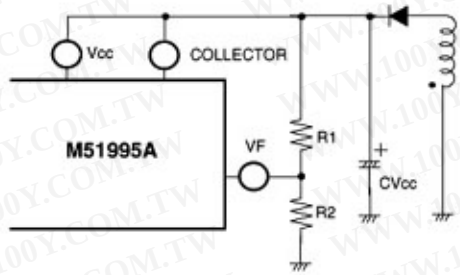


Fig.38 Circuit diagram to make knee point low on fly back system

(c)Application circuit to keep the non-operating condition when over load current condition will continue for specified duration

The CT terminal voltage will begin to rise and the capacitor connected to CT terminal will be charged-up,if the current limiting function starts,and VF terminal voltage decreases below V_{THTIME}(~3V).
If the charged-up CT terminal voltage is applied to OVP terminal through the level-shifter consisted of buffer transistor and resistor,it makes type M51995A keep non-operating condition.

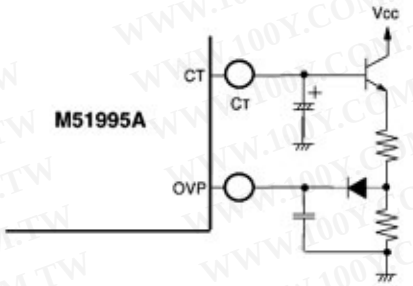


Fig.39 Application circuit diagram to keep the non-operating condition when over load current condition will continue for specified duration

Output circuit

(1)The output terminal characteristics at the Vcc voltage lower than the "Operation-stop" voltage

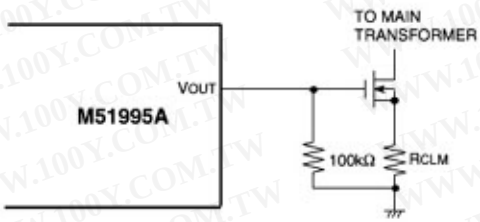


Fig.40 Circuit diagram to prevent the MOS-FIT gate potential rising

The output terminal has the current sink ability even though the Vcc voltage lower than the "Operation-stop" voltage or Vcc(STOP) (It means that the terminal is "Output low state" and please refer characteristics of output low voltage versus sink current.)
This characteristics has the merit not to damage the MOS-FIT at the stop of operation when the Vcc voltage decreases lower than the voltage of Vcc(STOP),as the gate charge of MOS-FIT,which shows the capacitive load characteristics to the output terminal,is drawn out rapidly.
The output terminal has the draw-out ability above the Vcc voltage of 2V,however,lower than the 2V,it loses the ability and the output terminal potential may rise due to the leakage current.
In this case, it is recommended to connect the resistor of 100kΩ between gate and source of MOS-FIT as shown in Fig.40.

(2)MOS-FIT gate drive power dissipation

Fig.41 shows the relation between the applied gate voltage and the stored gate charge.
In the region ① ,the charge is mainly stored at CGS as the depletion is spread and CGD is small owing to the off-state of MOS-FIT and the high drain voltage.
In the region ② ,the CGD is multiplied by the "mirror effect" as the characteristics of MOS-FIT transfers from off-state to on-state.
In the region ③ ,both the CGD and CGS affect to the characteristics as the MOS-FIT is on-state and the drain voltage is low.

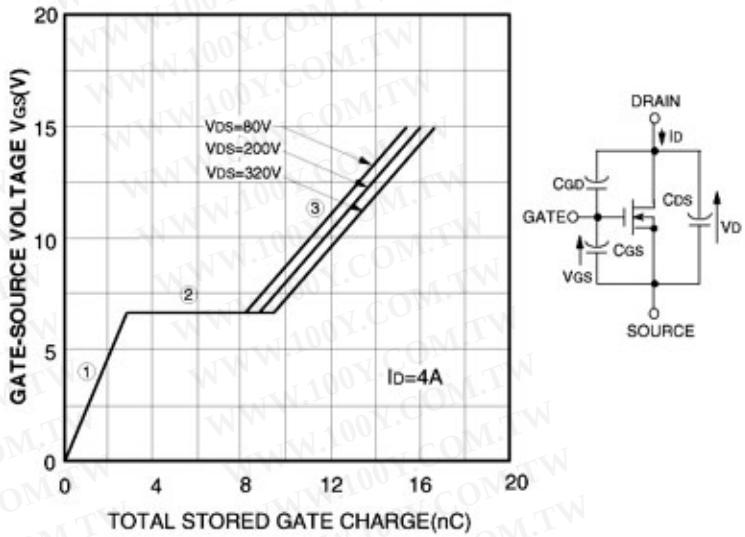


Fig.41 The relation between applied gate-source voltage and stored gate charge

The charging and discharging current caused by this gate charge makes the gate power dissipation.The relation between gate drive current ID and total gate charge QGSH is shown by following equation;

$$I_D = Q_{GSH} \cdot f_{OSC} \quad \text{.....(11)}$$

Where

fOSC is switching frequency

As the gate drive current may reach up to several tenths milliamperes at 500kHz operation,depending on the size of MOS-FIT,the power dissipation caused by the gate current can not be neglected.
In this case,following action will be considered to avoid heat up of type M51995A.
(1) To attach the heat sink to type M51995A
(2) To use the printed circuit board with the good thermal conductivity
(3) To use the buffer circuit shown next section

(3)Output buffer circuit

It is recommended to use the output buffer circuit as shown in Fig.42,when type M51995A drives the large capacitive load or bipolar transistor.

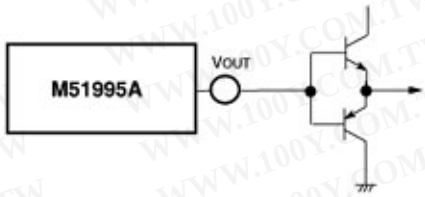


Fig.42 Output buffer circuit diagram

DET

Fig.43 shows how to use the DET circuit for the voltage detector and error amplifier.
For the phase shift compensation,it is recommended to connected the CR network between det terminal and F/B terminal.

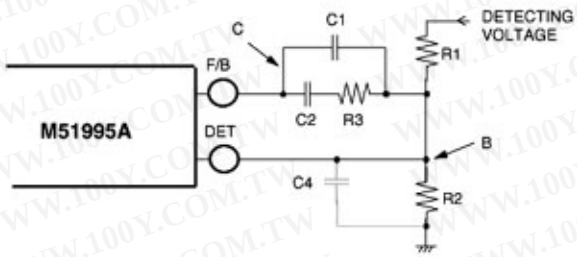


Fig.43 How to use the DET circuit for the voltage detector

Fig.44 shows the gain-frequency characteristics between point B and point C shown in Fig.43.
The G1,ω_1 and ω_2 are given by following equations;

$$G1 = \frac{R3}{R1/R2} \quad \text{.....(11)}$$

$$\omega_1 = \frac{1}{C2 \cdot R3} \quad \text{.....(12)}$$

$$\omega_2 = \frac{C1 + C2}{C1 \cdot C2 \cdot R3} \quad \text{.....(13)}$$

At the start of the operation,there happen to be no output pulse due to F/B terminal current through C1 and C2,as the potential of F/B terminal rises sharply just after the start of the operation.

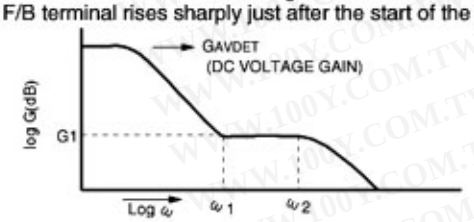


Fig.44 Gain-frequency characteristics between point B and C shown in Fig.43

Not to lack the output pulse,is recommended to connect the capacitor C4 as shown by broken line.
Please take notice that the current flows through the R1 and R2 are superposed to Icc(START).Not to superpose,R1 is connected to Cvcc2 as shown in Fig.27.

How to get the narrow pulse width during the start of operation

Fig.45 shows how to get the narrow pulse width during the start of the operation.If the pulse train of forcedly narrowed pulse-width continues too long,the misstart of operation may happen,so it is recommended to make the output pulse width narrow only for a few pulse at the start of operation.0.1μF is recommended for the C.

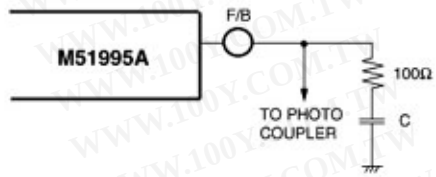


Fig.45 How to get the narrow pulse width during the start of operation

How to synchronize with external circuit

Type M51995A has no function to synchronize with external circuit,however,there is some application circuit for synchronization as shown in Fig.46.If this circuit is used,the synchronization may be out of order at the overload condition when the current limiting function starts to operate and VF terminal voltage becomes lower than 3V.

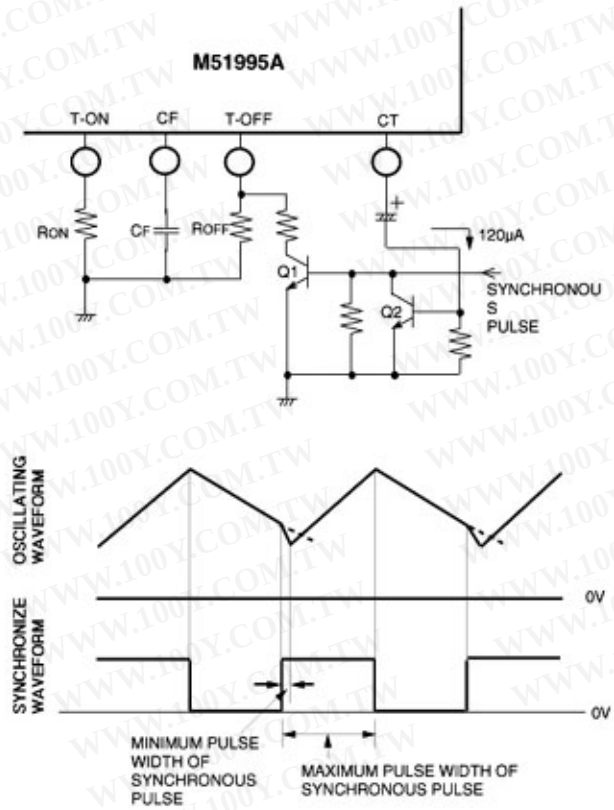


Fig.46 How to synchronize with external circuit

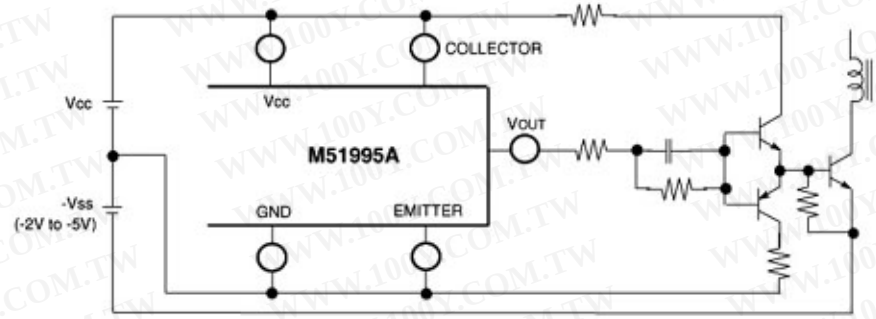


Fig.47 Driver circuit diagram (1) for bipolar transistor

Driver circuit for bipolar transistor

When the bipolar transistor is used instead of MOS-FIT,the base current of bipolar transistor must be sinked by the negative base voltage source for the switching-off duration,in order to make the switching speed of bipolar transistor fast one. In this case,over current can not be detected by detecting resistor in series to bipolar transistor,so it is recommended to use the CT(current transformer).
For the low current rating transistor,type M51995A can drive it directly as shown in Fig.48.

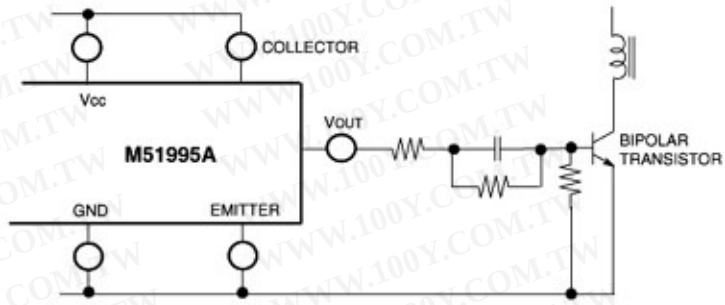
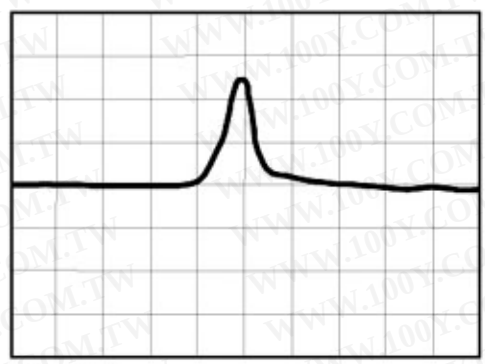


Fig.48 Driver circuit diagram (2) for bipolar transistor

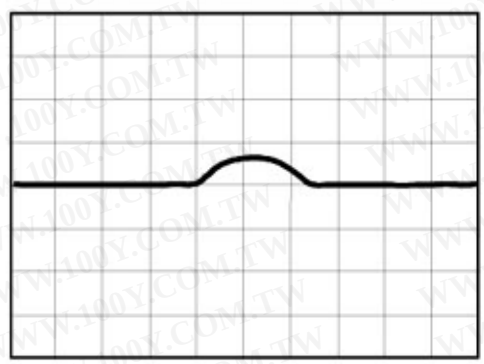
Attention for heat generation

The maximum ambient temperature of type M51995A is +85°C,however,the ambient temperature in vicinity of the IC is not uniform and varies place by place,as the amount of power dissipation is fearfully large and the power dissipation is generated locally in the switching regulator.
So it is one of the good idea to check the IC package temperature.
The temperature difference between IC junction and the surface of IC package is 15°C or less,when the IC junction temperature is measured by temperature dependency of forward voltage of pin junction,and IC package temperature is measured by "thermo-viewer",and also the IC is mounted on the "phenol-base" PC board in normal atmosphere.
So it is concluded that the maximum case temperature(surface temperature of IC) rating is 120°C with adequate margin.
As type M51995 has the modified totempole driver circuit, the transient through current is very small and the total power dissipation is decreased to the reasonable power level.Fig.49 shows the transient rush (through)current waveforms at the rising and falling edges of output pulse,respectively.



H-Axis : 20ns/div
V-Axis : 50mA/div

AT RISING EDGE OF OUTPUT PULSE



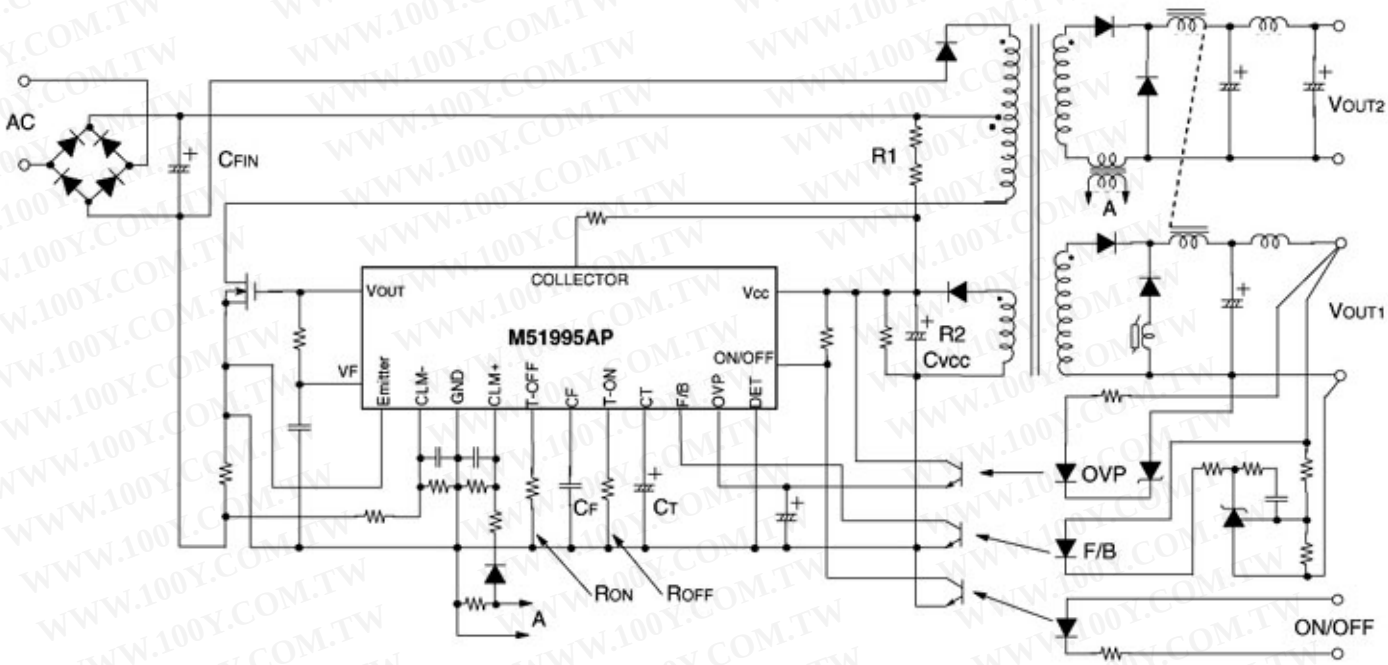
H-Axis : 20ns/div
V-Axis : 10mA/div

AT RISING EDGE OF OUTPUT PULSE

Fig.49 Through current waveform of totempole driver circuit at no-load and Vcc of 18V condition

APPLICATION EXAMPLE

Feed forward types SMPS with multi-output.



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