bq40z60 Programmable Battery Pack Manager

1 Features

- Fully Integrated 2-Series to 4-Series Cell Li-Ion or Li-Polymer Battery Pack Manager
- Input Voltage Range on Pack+: 2.5 V to 25 V
- Battery Charger Efficiency > 92%
- Battery Charger Operation Range: 4 V to 25 V
- Battery Charger, 1-MHz Synchronous Buck Controller for External NFETs
  - Soft Start to Limit In-Rush Current
  - Current Limit Protection for External Switches
  - Programmable Charging
    - Supports JEITA/Enhanced Charging Modes
- Fuel Gauging
  - High Resolution 16-Bit Integrator for Coulomb Counter
  - ADC, 16-Bit for Precision V, I, and T Measurements with 16-Channel Multiplexer
  - Support for Simultaneous CC and ADC Sampling (Power Conversion)
  - Supports Two-Wire SMBus v2.0 Interface with Accelerated 400-kHz Programming Option
  - SHA-1 Hash Message Authentication Code (HMAC) Responder for Increased Battery Pack Security
    - Split Key (2 x 64) Stored in Secure Memory
  - Supports Field Updates
- AFE Protection
  - Programmable Current Protection
    - Overcurrent in Discharge
    - Short-Circuit Current in Charge
    - Short-Circuit Current in Discharge
- N-FET High-Side Protection FET Drive
- Support for Four LEDs
- Thermistor inputs for NTC
- Compact 32-Pin QFN Package (RHB)

2 Applications

- Notebooks, Ultrabooks, Netbooks, Tablets, UMPCs
- Medical and Test Equipment
- Portable Instrumentation

3 Description

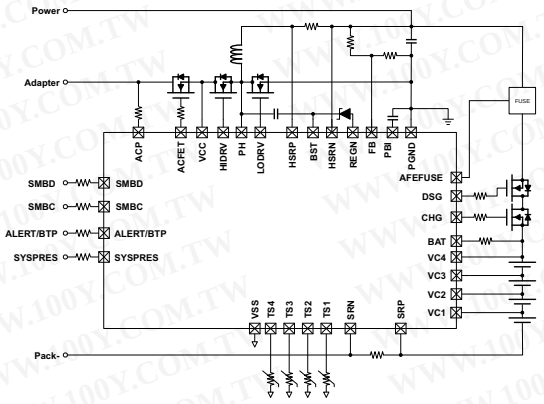
The Texas Instruments bq40z60 device is a Battery Pack Manager that integrates battery charging control output, gas gauging, and protection for completely autonomous operation of 2-series to 4-series cell Li-Ion and Li-Polymer battery packs. The architecture enables internal communication between the fuel gauging processor and battery charger controller to optimize the charging profile based on the external load conditions and power path source management during load transients and adaptor current limitations in the system. The charging current efficiency is scaleable for power transfer based on the external components, such as the NFETs, inductor, and sensing resistor.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq40z60	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Description (continued)

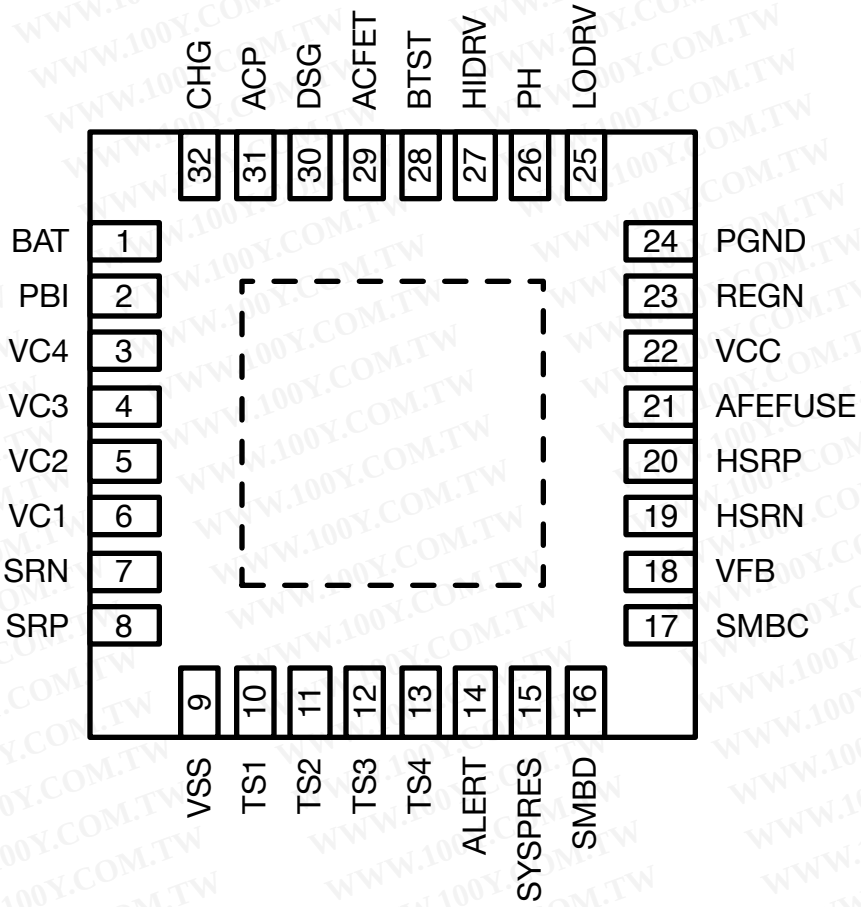
The device provides an array of battery and system safety functions, including overcurrent in discharge, short circuit in charge, and short circuit in discharge protection for the battery, as well as FET protection for the N-CH FETs, internal AFE watchdog, and cell disconnection detection. Through firmware, the device can provide a larger array of protection features including overvoltage, undervoltage, overtemperature, and more.

6 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial Release

7 Pin Configuration and Functions

QFN Package (RHB)
32 Pins



Pin Functions

NAME	NUMBER	TYPE(1)	DESCRIPTION
BAT	1	P	Battery input pin. Primary power supply
PBI	2	P	Power supply backup input pin
VC4	3	IA	Sense voltage input pin for the most positive cell, balance current input for the most positive cell, and battery stack measurement input
VC3	4	IA	Sense voltage input pin for the third most positive cell, balance current input for the third most positive cell, and return balance current for the most positive cell
VC2	5	IA	Sense voltage input pin for the second most positive cell, balance current input for the second most positive cell, and return balance current for the most positive cell
VC1	6	IA	Sense voltage input pin for the least positive cell, balance current input for the least positive cell, and return balance current for the second most positive cell
SRN	7	IA	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor.
SRP	8	IA	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor.
VSS	9	P	Device ground
TS1	10	IA	Thermistor input for temperature sensor channel 1 (hardware pin RC0)

(1) P = Power Connection, O = Digital Output, IA = Analog Input, I = Digital Input, I/OD = Digital Input/Output

Pin Functions (continued)

NAME	NUMBER	TYPE(1)	DESCRIPTION
TS2	11	IA	Thermistor input for temperature sensor channel 2
TS3	12	IA	Thermistor input for temperature sensor channel 3
TS4	13	IA	Thermistor input for temperature sensor channel 4
ALERT	14	I/O	Alert output to host (open drain)
SYSPRES	15	I/O	System presence indicator with internal weak pull up
SMBD	16	I/OD	SMBus data pin
SMBC	17	I/OD	SMBus clock pin
VFB	18	IA	Feedback sense input for charger control loop
HSRN	19	IA	High sense resistor negative node input
HSRP	20	IA	High sense resistor positive node input
AFEFUSE	21	O	Fuse drive output pin
VCC	22	P	Power supply input
REGN	23	O	Charger FET gate drive regulator
PGND	24	P	Power ground
LODRV	25	O	Low side charging FET gate control output
PH	26	I/O	Charger phase signal input
HIDRV	27	O	High side charging FET gate control output
BTST	28	IA	High side bootstrap capacitor input
ACFET	29	O	AC FET gate control output
DSG	30	O	N-CH FET drive output pin
ACP	31	IA	Adapter input pin
CHG	32	O	N-CH FET drive output pin

8 Specifications

8.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
Supply voltage range, V_{Supply}	BAT, VCC, PBI	–0.3		30	V
	REGN	–0.3		7	V
Input voltage range, V_{IN}	ACP, SMBC, SMBD, ALERT, SYSPRES	–0.3		30	V
	TS1, TS2, TS3, TS4	–0.3		V_{REG} + 0.3	V
	SRP, SRN	–0.3		0.3	V
	HSRP, HSRN	–0.3		30	V
	PH	–0.3		32	V
	VFB	–0.3		16	V
	VC4	VC3 – 0.3		VC3 + 8.5 V, or VSS + 30	V
	VC3	VC2 – 0.3		VC2 + 8.5 V, or VSS + 30	V
	VC2	VC1 – 0.3		VC1 + 8.5 V, or VSS + 30	V
	VC1	VSS – 0.3		VSS + 8.5 V, or VSS + 30	V
Output voltage range, V_O	CHG, DSG	–0.3		32	V
	HIDRV, BTST, ACFET	–0.3		36	V
	LODRV	–0.3		7	V
	AFEFUSE	–0.3		30	V
Maximum VSS current, I_{SS}			50		mA
Functional Temperature, T_{FUNC}		–40		110	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Rating	HBM(1)	±2	kV
	CDM(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{Supply}	Supply voltage	BAT, VCC, PBI	2.2		26	V
		ACFET, BTST	0		35	V
		REGN	0		6.5	V
$V_{SHUTDOWN–}$	Shutdown voltage	$V_{ACP} < V_{SHUTDOWN–}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	$V_{ACP} > V_{SHUTDOWN–} + V_{HYS}$	2.05	2.25	2.45	V
V_{HYS}	Shutdown voltage hysteresis	$V_{SHUTDOWN+} – V_{SHUTDOWN–}$		250		mV

Recommended Operating Conditions (continued)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	ACP, SMBC, SMBD, ALERT, SYSPRES			26	V
		TSx			V_{REG}	
		SRP, SRN	–0 .2		0.2	
		HSRP, HSRN	–0 .5		0.5	
		PH	–2		V_{ACP}	
		VFB	0		14	
		VC4	V_{VC3}		V_{VC3} + 5	
		VC3	V_{VC2}		V_{VC2} + 5	
		VC2	V_{VC1}		V_{VC1} + 5	
		VC1	V_{VSS}		V_{VSS} + 5	
V_O	Output voltage range	CHG, DSG, AFEFUSE			26	V
		HIDRV			35	V
		LODRV	0		6.5	V
C_{PBI}	External PBI capacitor		2.2			µF
T_{OPR}	Operating temperature		–40		85	°C

8.4 Thermal Information

THERMAL METRIC(1)		RSM	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance(2)	36	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	31.5	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	8	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	7.9	
$R_{\theta JCbot}$	Junction-to-case(bottom) thermal resistance(7)	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

8.5 Supply Voltage

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Device Operating Range	Operation with charger enabled	4.0		25	V
		Operation with charger disabled	2.5		25	
V_{CC-UV}	Under voltage lock out	VCC falling	2.2		2.45	V

8.6 Supply Current

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{NORMAL}	NORMAL mode(1)	CPU = ACTIVE, HFO = ON, ADC_FILTER = ON, CC_FILTER = ON, LFO = ON, REG18 = ON, CHG = ON, DSG = ON, ADC = ON, CC = ON, Charger Enabled, No Communication		1250	1850	µA
		CPU = HALT, HFO = ON, ADC_FILTER = ON, CC_FILTER = ON, LFO = ON, REG18 = ON, CHG = ON, DSG = ON, ADC = ON, CC = ON, Charger Disabled, No Communication		310	445	
I_{SLEEP}	SLEEP mode(1)	CPU = HALT, HFO = ON, ADC_FILTER = OFF, CC_FILTER = OFF, LFO = ON, REG18 = ON, CHG = ON, DSG = ON, ADC = OFF, CC = OFF, Charger Disabled, No Communication		122	183	µA
		CPU = HALT, HFO = OFF, ADC_FILTER = OFF, CC_FILTER = OFF, LFO = ON, REG18 = ON, CHG = ON, DSG = ON, ADC = OFF, CC = OFF, Charger Disabled, No Communication		92	138	
		CPU = HALT, HFO = ON, ADC_FILTER = OFF, CC_FILTER = OFF, LFO = ON, REG18 = ON, CHG = OFF, DSG = OFF, ADC = OFF, CC = OFF, Charger Disabled, No Communication		82	128	
		CPU = HALT, HFO = OFF, ADC_FILTER = OFF, CC_FILTER = OFF, LFO = ON, REG18 = ON, CHG = OFF, DSG = OFF, ADC = OFF, CC = OFF, Charger Disabled, No Communication		52	83	
$I_{SHUTDOWN}$	SHUTDOWN mode	CPU = HALT, HFO = OFF, ADC_FILTER = OFF, CC_FILTER = OFF, LFO = OFF, REG18 = OFF, CHG = OFF, DSG = OFF, ADC = OFF, CC = OFF, Charger Disabled, No Communication		0.5	2	µA

(1) $V_{CC} \leq 20$ V when CHG = ON and DSG = ON

8.7 Power Supply Control

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{SWITCHOVER-}$	BAT to VCC switchover voltage	$V_{BAT} < V_{SWITCHOVER-}$	2.0	2.1	2.2	V
$V_{SWITCHOVER+}$	VCC to BAT switchover voltage	$V_{BAT} > V_{SWITCHOVER-} + V_{HYS}$	3.0	3.1	3.2	V
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+} - V_{SWITCHOVER-}$		1000		mV
I_{LKG}	Input Leakage current	BAT pin, BAT = 0 V, VCC = 25 V			1	µA
		VCC pin, BAT = 25 V, VCC = 0 V			1	
		BAT and VCC pins, BAT = 0 V, VCC = 0 V, PBI = 25 V			1	
R_{PD}	Internal pulldown resistance	ACP	30	40	50	kΩ

8.8 Low-Voltage General Purpose I/O (TSx)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		0.65 x V_{REG}			V
V_{IL}	Low-level input				0.35 x V_{REG}	V
V_{OH}	Output voltage high	I_{OH} = –1.0 mA	0.75 x V_{REG}			V
		I_{OH} = –10 µA				
V_{OL}	Output voltage low	I_{OL} = 1.0 mA			0.2 x V_{REG}	V

Low-Voltage General Purpose I/O (TSx) (continued)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA

8.9 High-Voltage General Purpose I/O (ALERT, SYSPRES)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		1.3			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	V_{BAT} > 5.5 V, I_{OH} = –0 µA	3.5			V
		V_{BAT} > 5.5 V, I_{OH} = –10 µA	1.8			
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_O	Output reverse resistance	Between ALERT/SYSPRES and PBI	5			kΩ

8.10 AFE Power-On Reset

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{REGIT–}$	Negative-going voltage input	V_{REG}	1.51	1.55	1.59	V
V_{HYS}	Power on reset hysteresis	$V_{REGIT+} – V_{REGIT–}$	70	100	130	mV
t_{RST}	Power on reset time		200	300	400	µs

8.11 Internal 1.8-V LDO

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REG}	Regulator voltage		1.6	1.8	2.0	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 10 mA		±0.25%		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT} = 10 mA	–0 .6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5%		1.5%	
I_{REG}	Regulator output current limit	V_{REG} = 0.9 x $V_{REG(NOM)}$, V_{IN} > 2.2 V	20			mA
I_{SC}	Regulator short-circuit current limit	V_{REG} = 0 x $V_{REG(NOM)}$	25	40	50	mA
$PSRR_{REG}$	Power supply rejection ratio	$\Delta V_{BAT}/\Delta V_{REG}$, I_{REG} = 10 mA ,V_{IN} > 2.5 V, f = 10 Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold		1.58	1.65		V

8.12 Current Wake Comparator

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{WAKE}	Wake voltage threshold	$V_{WAKE} = V_{SRP} – V_{SRN}$	±0.3	±0.625	±0.9	mV
		$V_{WAKE} = V_{SRP} – V_{SRN}$	±0.6	±1.25	±1.8	
		$V_{WAKE} = V_{SRP} – V_{SRN}$	±1.2	±2.5	±3.6	
		$V_{WAKE} = V_{SRP} – V_{SRN}$	±2.4	±5.0	±7.2	
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		°C
t_{WAKE}	Time from application of current to wake			0.25	0.5	ms
$t_{WAKE(SU)}$	Wake comparator startup time			500	1000	µs

8.13 Coulomb Counter(1)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range		–0.1		0.1	V
Full scale range		$–V_{REF1}/10$		$V_{REF1}/10$	V
Integral nonlinearity(2)	16-bit, Best fit over input voltage range		±5.2	±22.3	LSB
Offset error	16-bit, Post-calibration		±5	±10	µV
Offset error drift	15-bit + sign, Post-calibration		0.2	0.3	µV/°C
Gain error	15-bit + sign, Over input voltage range		±0.2%	±0.8%	FSR(3)
Gain error drift	15-bit + sign, Over input voltage range			150	PPM/°C
Effective input resistance		2.5			MΩ

(1) Coulomb counter electrical specifications are assured when battery charging function is disabled.
(2) 1 LSB = $V_{REF1}/(10 \times 2^N) = 1.215/(10 \times 2^{15}) = 3.71$ µV
(3) Full-scale reference

8.14 CC Digital Filter

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits

8.15 ADC(1)

Over-operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range	Internal reference (V_{REF1})	–0.2		1	V
	External reference (V_{REG})	–0.2		0.8 x V_{REG}	
Full scale range	$V_{FS} = V_{REF1}$ or V_{REG}	$–V_{FS}$		V_{FS}	V
Integral nonlinearity(2)	16-bit, Best fit, –0.1 V to 0.8 x V_{REF1}			±6.6	LSB
	16-bit, Best fit, –0.2 V to –0.1 V			±13.1	
Offset error(3)	16-bit, Post-calibration, $V_{FS} = V_{REF1}$		±67	±157	µV

(1) ADC electrical specifications are assured when battery charging function is disabled.
(2) 1 LSB = $V_{REF1}/(2^N) = 1.225/(2^{15}) = 37.4$ µV (when ADCTL[SPEED1, SPEED0] = 0, 0)
(3) For VC1–VSS, VC2–VC1, VC3–VC2, VC3–VSS, ACP–VSS, and $V_{REF1}/2$, the offset error is multiplied by (1/ADC multiplexer scaling factor (K)).

ADC(1) (continued)

Over-operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Offset error drift	16-bit, Post-calibration, $V_{FS} = V_{REF1}$		0.6	3	µV/°C
Gain error	16-bit, –0.1 V to 0.8 x V_{FS}		±0.2%	±0.8%	FSR
Gain error drift	16-bit, –0.1 V to 0.8 x V_{FS}			150	PPM/°C
Effective input resistance		8			MΩ

8.16 ADC Digital Filter

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Conversion time	ADCTL[SPEED1, SPEED0] = 0, 0		31.25		ms
	ADCTL[SPEED1, SPEED0] = 0, 1		15.63		
	ADCTL[SPEED1, SPEED0] = 1, 0		7.81		
	ADCTL[SPEED1, SPEED0] = 1, 1		1.95		
Resolution	No missing codes, ADCTL[SPEED1, SPEED0] = 0, 0	16			Bits
Effective resolution	With sign, ADCTL[SPEED1, SPEED0] = 0, 0	14	15		Bits
	With sign, ADCTL[SPEED1, SPEED0] = 0, 1	13	14		
	With sign, ADCTL[SPEED1, SPEED0] = 1, 0	11	12		
	With sign, ADCTL[SPEED1, SPEED0] = 1, 1	9	10		

8.17 ADC Multiplexer

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
K	Scaling factor	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	0.1980	0.2000	0.2020	—
		VC4–VSS, ACP–VSS	0.049	0.050	0.051	
		V_{REF2}	0.490	0.500	0.510	
		HSRN–VSS	0.049	0.050	0.051	
V_{IN}	Input voltage range	VC4–VSS, ACP–VSS	–0.2		20	V
		TSx	–0.2		0.8 x V_{REF1}	
		TSx	–0.2		0.8 x V_{REG}	
I_{LKG}	Input leakage current	VC1, VC2, VC3, VC4, cell balancing off, cell detach detection off, ADC multiplexer off			1	µA

8.18 Cell Balancing Support

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{CB}	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at 2 V < V_{DS} < 4 V			200	Ω

8.19 Cell Detach Detection

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{CD}	Internal cell detach check current	VCx > VSS + 0.8 V	30	50	70	µA

8.20 Internal Temperature Sensor

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{TEMP}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9	–2.0	–2.1	mV/°C
		$V_{TEMPP} – V_{TEMPN}$, assured by design	0.177	0.178	0.179	

8.21 NTC Thermistor Measurement Support (ADCx)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{NTC(PU)}$	Internal pullup resistance		14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$	Resistance drift over temperature		–360	–280	–200	PPM/°C

8.22 High-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–2.5%	±0.25%	2.5%	
		T_A = –40°C to 85°C, includes frequency drift	–3.5%	±0.25%	3.5%	
$t_{HFO(SU)}$	Start-up time	T_A = –20°C to 85°C, CLKCTL[HFRAMP] = 1, oscillator frequency within +/–3% of nominal			4	ms
		CLKCTL[HFRAMP] = 0, oscillator frequency within +/–3% of nominal			100	µs

8.23 Low-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{LFO}	Operating frequency			262.144		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C, includes frequency drift	–2.5	±0.25	2.5	
$f_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz

8.24 Voltage Reference 1

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.21	1.215	1.22	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

8.25 Voltage Reference 2

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

8.26 Instruction Flash

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			2	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

8.27 Data Flash

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			1	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

8.28 Current Protection Thresholds

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OCD}	OCD detection threshold voltage range	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–16.6		–100	mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–8.3		–50	
ΔV_{OCD}	OCD detection threshold voltage program step	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–5.56		mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–2.78		
V_{SCC}	SCC detection threshold voltage range	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	44.4		200	mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	22.2		100	

Current Protection Thresholds (continued)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ΔV_{SCC}	SCC detection threshold voltage program step	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		22.2		mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		11.1		
V_{SCD1}	SCD1 detection threshold voltage range	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		
V_{OFFSET}	OCD, SCC, and SCDx offset error	Post-trim	–2.5		2.5	mV
V_{SCALE}	OCD, SCC, and SCDx scale error	No trim	–10%		10%	
		Post-trim	–5%		5%	

8.29 N-CH FET Drive (CHG, DSG)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Output voltage ratio	$Ratio_{DSG} = (V_{DSG} – V_{BAT})/V_{BAT}$, 2.2 V < V_{BAT} < 4.07 V, 10 MΩ between HSRN and DSG	2.133	2.333	2.533	—
		$Ratio_{CHG} = (V_{CHG} – V_{BAT})/V_{BAT}$, 2.2 V < V_{BAT} < 4.07 V, 10 MΩ between BAT and CHG	2.133	2.333	2.533	
		$Ratio_{ACFET} = (V_{ACFET} – V_{BAT})/V_{BAT}$, 2.2 V < V_{BAT} < 4.07 V, 10 MΩ between ACP and ACFET	2.133	2.333	2.533	
$V_{(FETON)}$	Output voltage, CHG and DSG on	$V_{DSG(ON)} = V_{DSG} – V_{BAT}$, V_{BAT} ≥ 4.07 V, 10 MΩ between V_{HSRN} and DSG, V_{BAT} = 18 V	9.0	9.5	10	V
		$V_{CHG(ON)} = V_{CHG} – V_{BAT}$, V_{BAT} ≥ 4.07 V, 10 MΩ between BAT and CHG, V_{BAT} = 18 V	9.0	9.5	10	
	ACFET	$V_{ACFET(ON)} = V_{ACFET} – V_{BAT}$, V_{BAT} ≥ 4.07 V, 10 MΩ between ACP and ACFET, V_{BAT} = 18 V	9.0	9.5	10	
$V_{(FETOFF)}$	Output voltage, CHG and DSG off	$V_{DSG(OFF)} = V_{DSG} – V_{ACP}$, 10 MΩ between HSRN and DSG	–0.4		0.4	V
		$V_{CHG(OFF)} = V_{CHG} – V_{BAT}$, 10 MΩ between BAT and CHG	–0.4		0.4	
	ACFET	$V_{ACFET(OFF)} = V_{ACFET} – V_{ACP}$, V_{BAT} ≥ 4.07 V, 10 MΩ between ACP and ACFET, V_{BAT} = 18 V	–0.4		0.4	
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG(ON)(TYP)}$, V_{ACP} ≥ 2.2 V, C_L = 4.7 nF between DSG and V_{HSRN}, 5.1 kΩ between DSG and C_L, 10 MΩ between V_{HSRN} and DSG		200	500	µs
		V_{CHG} from 0% to 35% $V_{CHG(ON)(TYP)}$, V_{ACP} ≥ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		200	500	
		V_{ACFET} from 0% to 35% $V_{ACFET(ON)(TYP)}$, V_{ACP} ≥ 2.2 V, C_L = 4.7 nF between ACFET and ACP, 5.1 kΩ between CHG and C_L, 10 MΩ between ACP and ACFET		200	500	

N-CH FET Drive (CHG, DSG) (continued)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_F	Fall time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, V_{ACP} ≥ 2.2 V, C_L = 4.7 nF between DSG and ACP, 5.1 kΩ between DSG and C_L, 10 MΩ between ACP and DSG		40	300	µs
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1 V, V_{ACP} ≥ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		40	200	
		V_{ACFET} from $V_{ACFET(ON)(TYP)}$ to 1 V, V_{ACP} ≥ 2.2 V, C_L = 4.7 nF between ACFET and ACP, 5.1 kΩ between CHG and C_L, 10 MΩ between ACP and ACFET		40	200	

8.30 FUSE Drive (AFEFUSE)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage high	V_{BAT} ≥ 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	6	7	8.65	V
		V_{BAT} < 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	V_{BAT} – 0.1		V_{BAT}	
V_{IH}	High-level input		1.5	2.0	2.5	V
$I_{AFEFUSE(PU)}$	Internal pullup current	V_{BAT} ≥ 8 V, $V_{AFEFUSE}$ = VSS		150	330	nA
$R_{AFEFUSE}$	Output impedance		2	2.6	3.2	kΩ
C_{IN}	Input capacitance			5		pF
t_{DELAY}	Fuse trip detection delay		128		256	µs
t_{RISE}	Fuse output rise time	V_{BAT} ≥ 8 V, C_L = 1 nF, V_{OH} = 0 V to 5 V		5	20	µs

8.31 Battery Charger Voltage Regulation (VFB)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{FB}	Regulation range	Based on internal DAC reference setting	0.61		1.22	V
V_{FBACC}	Voltage feedback accuracy	V_{FB} = 1.22 V	–2%		2%	
$V_{FB(STEPS)}$	Programable regulation steps			2.5		mV
R_{VFB}	Total feedback resistor divider range			500	700	kΩ

8.32 Battery Charger Current Sense (HSRP, HSRN)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN(Normal\ range)}$	Differential Input range	DAC range for current measurement	2		100	mV
V_{ACC}	Measurement accuracy	$V_{HSRP} – V_{HSRN}$ = 50 mV, R_{Sense}= 10 mΩ	–5%		5%	

8.33 Battery Charger Precharge Current Sense (HSRP, HSRN)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN(Normal\ range)}$	Differential Input range	DAC range for current measurement	2		20	mV
V_{ACC}	Measurement accuracy	$V_{HSRP} – V_{HSRN}$ = 2 mV, R_{Sense}= 10 mΩ (V_{HSRN} > 2.3 V)	–70%		70%	

8.34 AC Adapter Fault Detect (HSRN, VCC)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{HSRN – VCC}$	AC adapter input fault detect	Battery > AC adapter input (Falling)	150	225	300	mV
V_{Hys}	Recovery hysteresis	AC adapter input > Battery (Rising)	50	100	150	mV

8.35 Battery Charger Overcurrent Detection $(V)_{HSRP}$, $(V)_{HSRN}$

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{OC(max)}$	Charger overcurrent threshold	Charging current as a percentage of max sense voltage range		180	200	mV
$I_{OC(min)}$	Charger overcurrent threshold	Minimum charging overcurrent detected	45	55		mV

8.36 Battery Charger Undercurrent Detection $(V)_{HSRP}$, $(V)_{HSRN}$

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{UC(Detect)}$	Detect under current for negative inductor current	$V_{HSRP} – V_{HSRN}$ < 0 mV, for negative inductor current, V_{HSRP} > 2.3 V	1	5	16	mV
$I_{UC(Non-synch)}$	Minimum sense voltage to enter non-synchronous mode			1.7		mV

8.37 System Operation Detection $(V)_{HSRN}$

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{HSRN}	Input voltage for operation	V_{HSRN} Falling	2.05	2.15	2.25	V
V_{Hys}	Recovery hysteresis	V_{HSRN} Rising	100	150	200	mV

8.38 Battery Overvoltage Comparator (VFB)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OV(max)}$	Battery over-voltage detection	VFB > Set value (Rising)		106%		
$V_{OV(Recovery)}$	Battery over-voltage recovery	VFB < V_{OV} (Falling)		103%		

8.39 Regulator (REGN)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{LODRV}	Gate drive for low side charger FET	VCC > 10 V, I_{Load} = 0 to 60 mA	5.7	6.0	6.3	V
I_{SC}	Short circuit current limit	V_{LODRV} = 0 V	60			mA
V_{REGN}	Power good indicator	V_{REGN} Rising	3.6	3.68	3.75	V
V_{Hys}	Hysteresis	V_{REGN} Falling	240	260	280	mV

8.40 PWM High-Side Driver (HiDRV)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{ON}	Driver turn ON resistance	$V_{BTST} – V_{PH} \geq 5.5$ V		6.0	8.6	Ω
R_{OFF}	Driver turn OFF resistance	VFB < V_{OV} (Falling)		2.5	3.3	Ω
$V_{BOOTSTRAP}$	Bootstrap refresh comparator	VCC = 4 V to 6 V	2.6	2.9		V
		VCC > 6 V	3.9	4.1		V

8.41 PWM Low-Side Driver (LoDRV)

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{ON}	Driver turn ON resistance	$V_{REGN} – V_{PGND} \geq 5.5$ V	5.2		7.6	Ω
R_{OFF}	Driver turn OFF resistance	VFB < V_{OV} (Falling)	1.9		2.4	Ω

8.42 PWM Information

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{DEADTIME}$	Deadtime between FET driver output switching			30		ns
Duty cycle					99.5%	
f_{SW}	PWM switching frequency		0.8	1.0	1.1	MHz

8.43 Charger Power-Up Sequence

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DELAY}	Power-up sequence			8		ms
$t_{SS(STEPS)}$	Soft start steps			8		
$t_{SS(STEP\ TIME)}$	Soft start time			2		ms

8.44 THERMAL Shutdown Comparator

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$T_{SHUTDOWN}$			135	145	C
T_{Hys}			12		C

8.45 SMBus High Voltage I/O

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high	SMBC, SMBD, V_{REG} = 1.8 V	1.3			V
V_{IL}	Input voltage low	SMBC, SMBD, V_{REG} = 1.8 V			0.8	V
V_{OL}	Output low voltage	SMBC, SMBD, V_{REG} = 1.8 V, I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PD}	pulldown resistance		0.7	1.0	1.3	MΩ

8.46 SMBus

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4.0			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4.0			µs
$t_{HD(DATA)}$	Data hold time		300			ns
$t_{SU(DATA)}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal detect time		25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4.0		50	µs
t_R	Clock rise time	10% to 90%			1000	ns
t_F	Clock fall time	90% to 10%			300	ns
$t_{LOW(SEXT)}$	Cumulative clock low slave extend time				25	ms
$t_{LOW(MEXT)}$	Cumulative clock low master extend time				10	ms

8.47 SMBus XL

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SMBXL}	SMBus XL operating frequency	SLAVE mode	40		400	kHz

SMBus XL (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4.0			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4.0			µs
$t_{TIMEOUT}$	Error signal detect time		5		20	ms
t_{LOW}	Clock low period				20	µs
t_{HIGH}	Clock high period				20	µs

8.48 Timing Requirements

Typical values stated where T_A = 25°C and VCC = 10.8 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
CURRENT PROTECTION TIMING						
t_{OCD}	OCD detection delay time		1		31	ms
Δt_{OCD}	OCD detection delay time program step			2		ms
t_{SCC}	SCC detection delay time		0		915	µs
Δt_{SCC}	SCC detection delay time program step			61		µs
t_{SCD1}	SCD1 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		915	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		1850	
Δt_{SCD1}	SCD1 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		61		µs
		PROTECTION_CONTROL[SCDDx2] = 1		121		
t_{SCD2}	SCD2 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		458	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		915	
Δt_{SCD2}	SCD2 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		30.5		µs
		PROTECTION_CONTROL[SCDDx2] = 1		61		
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3$ mV for OCD, SCD1, and SC2, $V_{SRP} – V_{SRN} = V_T + 3$ mV for SCC			160	µs
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10%		10%	

8.49 Typical Characteristics

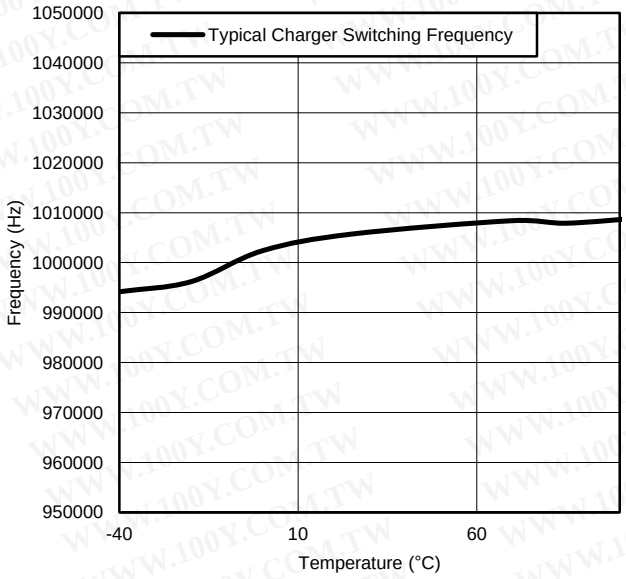


Figure 1. Charger Switching Frequency Across Temperature

9 Detailed Description

9.1 Overview

The bq40z60 is a fully integrated battery manager that employs flash-based firmware and integrated hardware protection to provide a complete solution for 2-series to 4-series cell battery stack architectures. The bq40z60 interfaces with a host system via an SBS v1.1-compliant, SMBus interface, and processes instructions and data using a state-of-the-art, ultra-low-power TI bqBMP CPU. High-performance, integrated analog peripherals allow support for a sense resistor down to 3 mΩ, battery charge control, and simultaneous current/voltage data conversion for instant power calculations.

The bq40z60 controls the cell charging profile based on user-programmed data flash parameters for charging current and voltage based on temperature and cell voltage. The gas gauge provides the cell voltage and charging information to the battery charging through an internal communication bus. The charger function is controlled based on cell voltage measurements both on individual cell and total series stack readings.

The analog front end provides this voltage-based information to the charging circuit to set the profiles pre-programmed in the data flash settings, which are useful for zero voltage and PRECHARGE mode operation. The following sections detail all of the major component blocks in the bq40z60 device.

9.2 Functional Block Diagram

Figure 2 shows the functional block diagram for the bq40z60 device.

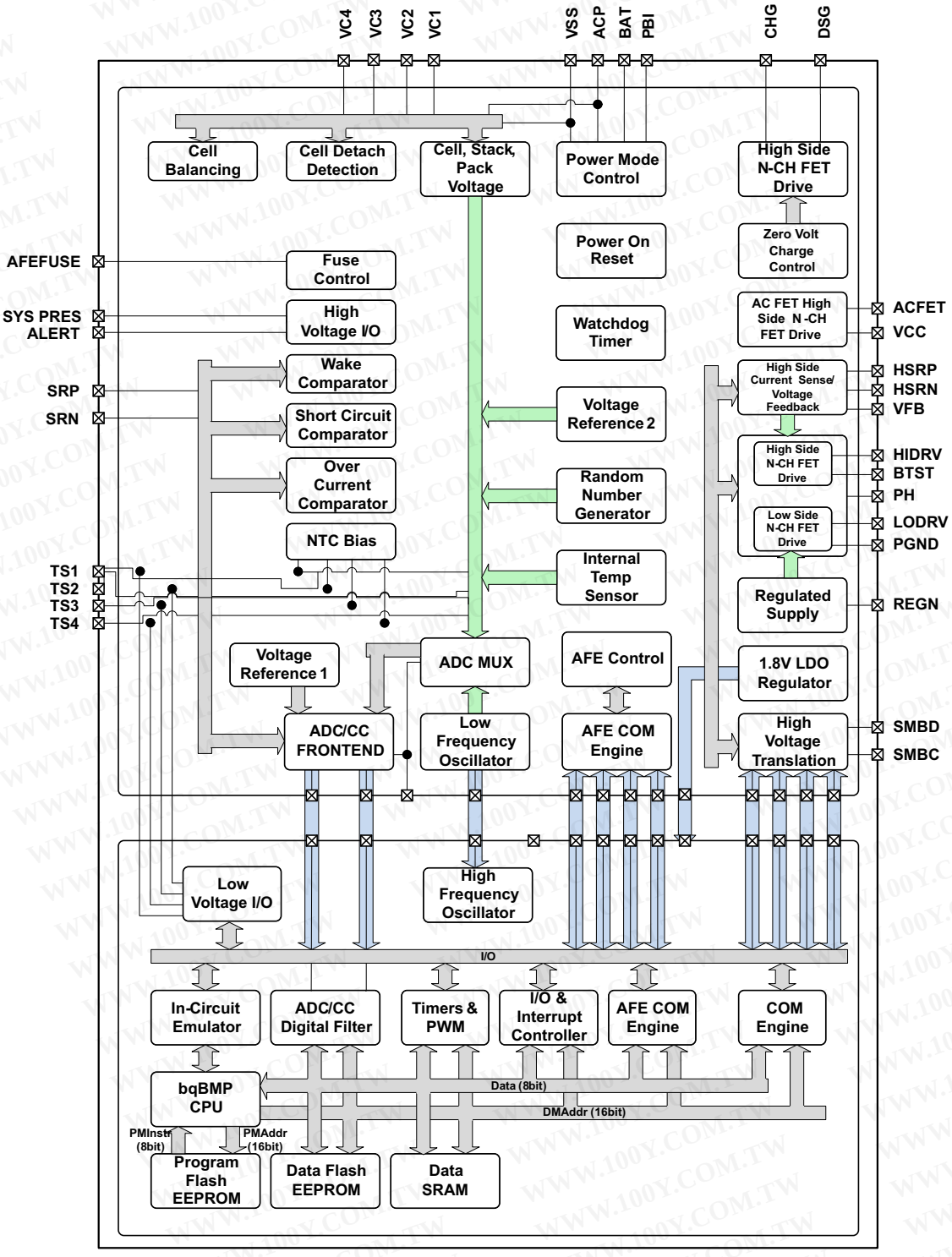


Figure 2. bq40z60 Functional Block Diagram

9.3 Feature Description

The bq40z60 consists of an integrated analog front end, charge controller, and fuel gauge. The following sections provide an overview of the device features. For additional details, refer to the *bq40z60 Technical Reference Manual* (SLUUA04).

9.3.1 Safety Features

The bq40z60 provides support for primary safety, including:

- Cell Over/Undervoltage Protection
- Charge and Discharge Overcurrent
- Short Circuit Protection
- Charge and Discharge Overtemperature

The secondary safety features of the bq40z60 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety features provide protection against:

- Safety Over/Undervoltage Permanent Failure
- Safety Overtemperature Permanent Failure
- Safety FET Overtemperature Permanent Failure
- Qmax Imbalance Permanent Failure
- Impedance Imbalance Permanent Failure
- Capacity Degradation Permanent Failure
- Cell Balancing Permanent Failure
- Fuse Failure Permanent Failure
- Voltage Imbalance at Rest Permanent Failure
- Voltage Imbalance Active Permanent Failure
- Charge/Discharge FET Permanent Failure
- Second Level Protector Permanent Failure
- Instruction Flash Checksum Permanent Failure
- Open Cell Connection Permanent Failure
- Data Flash Permanent Failure
- Open Thermistor Permanent Failure

9.3.2 Analog Front End (AFE) Details

The analog front end (AFE) consists of circuits responsible for managing internal power and interfacing to outside components for measuring current, voltage, and temperature. The bq40z60 AFE includes an active-high interrupt output connected internally to the fuel gauge to notify it of important changes in some of the AFE registers.

The bq40z60 manages its supply voltage dynamically according to operating conditions. When $V_{BAT} > V_{SWITCHOVER–} + V_{HYS}$, the AFE connects an internal switch to BAT and uses this pin to supply power to its internal 1.8-V LDO, which subsequently powers all device logic and flash operations. Once BAT decreases to $V_{BAT} < V_{SWITCHOVER–}$, the AFE disconnects its internal switch from BAT and connects another switch to VCC, allowing sourcing of power from a charger (if present). An external capacitor connected to PBI provides a momentary supply voltage to help guard against system brownouts due to transient short-circuit or overload events that pull VBAT below $V_{SWITCHOVER–}$.

Feature Description (continued)

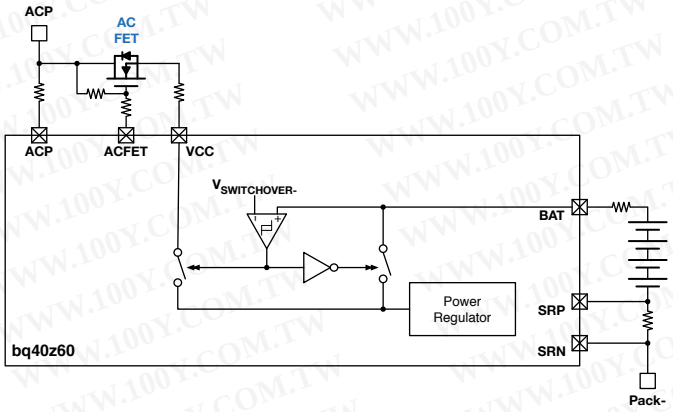


Figure 3. Internal Power Source Selection

In the event of a power-cycle, the bq40z60 AFE will hold its internal RESET output pin high for t_{RST} duration to allow its internal 1.8-V LDO and LFO to stabilize before running the analog gas gauge (AGG). The AFE enters power-on reset when the voltage at V_{REG} falls below V_{REGIT-}, and exits reset when V_{REG} rises above V_{REGIT-} + V_{HYS} for t_{RST} time. After t_{RST}, the bq40z60 AGG writes its trim values to the AFE.

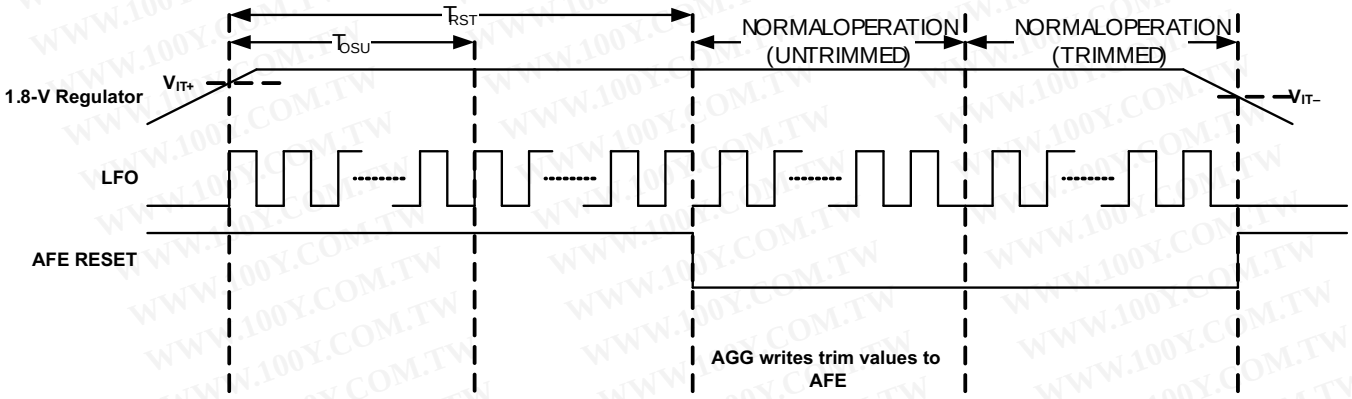


Figure 4. Power-On Reset Operation

The bq40z60 AFE includes a low frequency oscillator (LFO) running at 262.144 kHz. The AFE monitors the LFO frequency and indicates a failure via LATCH_STATUS[LFO] if the output frequency is much lower than normal.

The bq40z60 AFE provides two internal voltage references: V_{REF1}, used by the ADC and CC, and V_{REF2} used by the LDO, LFO, current wake comparator, and over- and short-current protection circuitry.

9.3.2.1 Wake Up Comparator

The internal wake comparator can be used to wake the bq40z60 from a HALT state if a configurable threshold is detected across SRP and SRN.

9.3.2.2 Cell Balancing Support

The integrated cell balancing FETs included in the bq40z60 device allow the AFE to bypass cell current around a given cell or numerous cells to effectively balance the entire battery stack. External series resistors placed between the cell connections and the VCx input pins set the balancing current magnitude. The cell balancing circuitry can be enabled or disabled via the CELL_BAL_DET[CB3, CB2, CB1] control register. Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing.

Feature Description (continued)

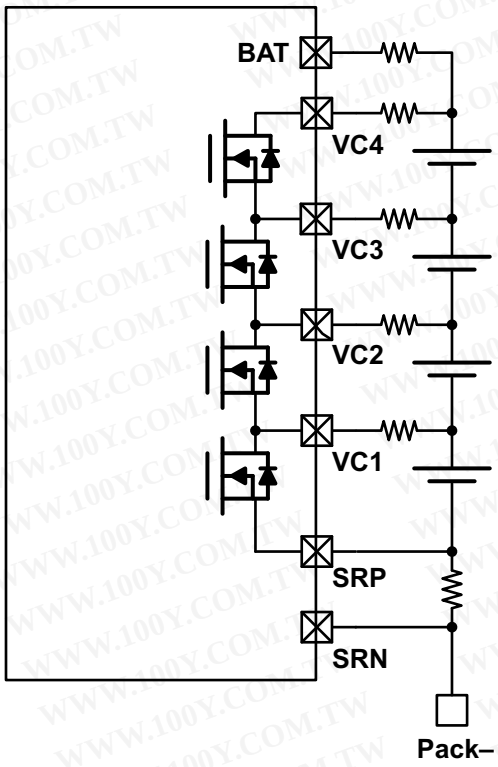


Figure 5. Cell Balancing Configuration

9.3.2.3 FET Drive

The bq40z60 controls two external N-CH MOSFETs in a back-to-back configuration for battery protection. The charge (CHG) and discharge (DSG) FETs are automatically disabled if a safety fault is detected and can also be manually turned off using AFE_CONTROL[CHGEN, DSGEN] = 0, 0. When the gate drive is disabled, an internal circuit discharges CHG to BAT and DSG to HSRN.

The AC FET (N-CH MOSFET) controls power input from the AC adaptor to the battery charging system by monitoring the voltage at the VCC pin, and turning ON the ACFET if the voltage exceeds the V_{HSRN} voltage. The following register command sets the AC FET gate drive output control, AFE_STATUS register (0x01) ACFET (Pin 2): Setting this pin to 1 allows the AC FET gate drive to be on if other conditions are satisfied.

9.3.2.4 Fuse Drive

The bq40z60 AFE has the ability to blow an external fuse in the event of a permanent failure. The fuse drive itself is supplied from the BAT input pin and its state can be monitored using the AFE_STATUS[FUSE_RAW] register. If AFE_STATUS[FUSE_RAW} = 1 for t_{DELAY} duration, then LATCH_STATUS[FUSE] is set to 1, and after an additional 500 ms, the CHG and DSG FET drive outputs will be disabled if LATCH_STATUS[FUSE] has not been cleared by then. If the AFEFUSE output is not used, it should be connected to VSS. When AFEFUSE is in the low state, it uses an internal weak pullup to enable detection of disconnection between the AFEFUSE pin and the fuse drive circuitry.

Feature Description (continued)

9.3.3 Charge Controller Details

The charge controller, under control from the fuel gauge's processor, provides autonomous control over the charging of the battery pack. The controller uses a 1-MHz buck architecture using external FETs driven by internal gate drivers. The charge voltage and current can be adjusted via data flash values to account for the temperature and voltage of the battery cells, allowing for a JEITA type charge profile. The voltage and current may also be directly written to the charge controller from an external host, allowing for a user-defined charging profile. The charger runs in Narrow Voltage DC, that is, the output voltage of the charger will only exceed the battery voltage by a small amount; by contrast, a charger that does not run in Narrow Voltage DC mode will output the adapter voltage to the system.

The charger is designed to enable the system to continue to run while the battery is charged. If the system requires more current than the charger is able to provide, the battery supplements the current to the system. The charger can support an external precharge FET, allowing the VSYS to remain above a minimum voltage needed for the system to operate.

The charger supports precharge, constant current/constant voltage, and termination, as shown below. The voltage and current thresholds for precharge and termination are controlled by data flash values. Refer to the *bq40z60 Technical Reference Manual* (SLUUA04) for more information.

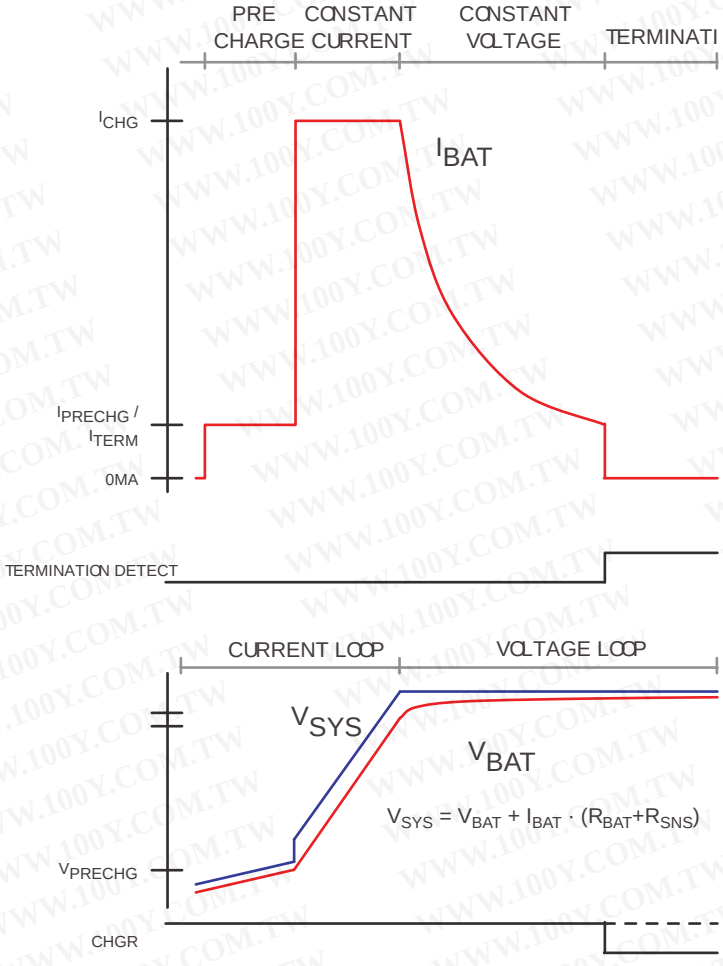


Figure 6. Normal Charge Profile

Feature Description (continued)

The charger maintains a cycle-by-cycle current limit by sensing across a resistor in series with the inductor (shown in Figure 7 as R_{CHG}). In precharge and constant voltage, the DC current is regulated by sensing the current across the sense resistor at the bottom on of the cell stack. When the charger is enabled, the initial current is set for either the Precharge or Constant Current/Constant Voltage (CC/CV) value, based on the minimum cell voltage. Once the charger enters CONSTANT CURRENT mode, the temperature and maximum cell voltage-adjusted–charging current is set, and the voltage output of the charger is automatically regulated to maintain the current across RCHG. Once the temperature-adjusted voltage is reached by the charger output, the current starts to taper.

Throughout the charge cycle, the current available from the charger is limited by the *ChargingCurrent()* value. The system draws more current, however, with the battery supplementing the difference. Once battery charging is terminated, the charger is capable of supplying all of the current defined by the ***Advanced Charge Algorithm:Maximum Current*** Register value. Refer to the *bq40z60 Technical Reference Manual* (SLUUA04) for more information.

Figure 7 shows the system power path with the adaptor current and battery current overlaid. Further information is available in Application and Implementation.

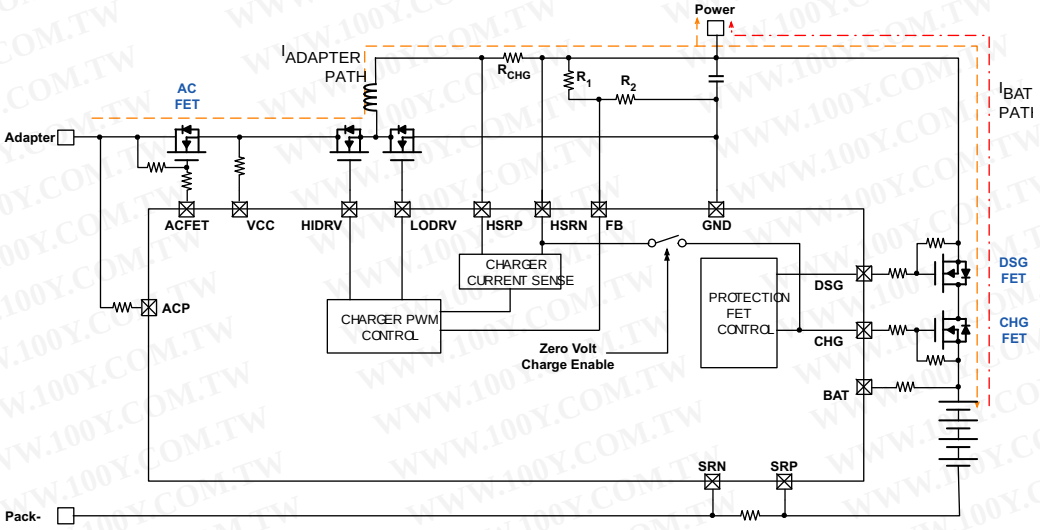


Figure 7. Power Path Overview

9.3.3.1 Precharge Modes

The charge controller is designed to allow for both internal precharge control and external precharge control. The device can operate in precharge with external FETs and a current limiting resistor. (Refer to the *bq40z60 Technical Reference Manual* (SLUUA04) for more information.)

9.3.3.2 Zero-Volt Charge Support

This mode of operation is similar to PRECHARGE mode switched charging, but with the charge FET operation in the saturation region. The NVDC out is connected to the CHG gate drive output internally to allow for precharge current from the charger through the CHG FET. This current is limited based on the value of the external R_{sense} (10-mΩ resistor the lowest precharge current = 200 mA). This will increase the power dissipation of the charge FET and will require thermal heat management and protection to ensure correct operation.

9.3.3.3 Charge Termination

Once the highest cell voltage reaches the value specified in the data flash, the charger output voltage will no longer increase and the current will start to taper. Once the highest cell voltage is within the ***Charge Term Voltage*** window and the measured current is below ***Charge Term Taper Current*** for 40 s or more, the charger will terminate by disabling the CHG FET and setting the appropriate flags. (Refer to the *bq40z60 Technical Reference Manual* (SLUUA04) for more information.)

Feature Description (continued)

The system can still provide load current from the battery pack if the adaptor current cannot support the system load. The diode of the CHG FET starts to conduct as the system voltage decreases to a point where the pack voltage is greater than the system regulation voltage – V_{diode}. If the average discharge current is high, the system can turn ON the CHG FET for improved efficiency and minimized line losses during the discharge phase.

9.3.4 Fuel Gauge and Control Details

The bq40z60 uses the Impedance Track algorithm to measure and calculate the available capacity in battery cells. The bq40z60 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq40z60 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. The device also has TURBO BOOST mode support, which enables the bq40z60 to provide the necessary data for the MCU to determine what level of peak power consumption can be applied without causing a system reset or a transient battery voltage level spike to trigger termination flags. (See the *bq40z60 Technical Reference Manual* (SLUUA04) for further details.)

9.3.4.1 Battery Trip Point (BTP)

Required for WIN8 OS, the Battery Trip Point (BTP) feature indicates when the RSOC of a battery pack has depleted to a certain value set in a DF register. This feature allows a host to program two capacity-based thresholds that govern triggering a BTP interrupt on the BTP_INT pin, and setting or clearing the *OperationStatus[BTP_INT]* on the basis of *RemainingCapacity()*.

An internal weak pullup is applied when the BTP feature is active. Depending on the system design, an external pullup may be required to put on the BTP_INT pin. See High-Voltage General Purpose I/O (ALERT, SYSPRES) for details.

9.3.4.2 Lifetime Data Logging Features

The bq40z60 offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and Minimum Cell Voltages
- Maximum Delta Cell Voltage
- Maximum Charge Current
- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum Delta Cell Temperature
- Maximum and Minimum Internal Sensor Temperature
- Maximum FET Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
- Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
- Number of Shutdown Events
- Cell Balancing Time for Each Cell
  (This data is updated every 2 hours if a difference is detected.)
- Total FW Runtime and Time Spent in Each Temperature Range
  (This data is updated every 2 hours if a difference is detected.)

9.3.5 Authentication

The bq40z60 supports authentication by the host using SHA-1. More information about the algorithm can be found in the *bq40z60 Technical Reference Manual* (SLUUA04).

Feature Description (continued)

9.3.6 LED Display

The bq40z60 can drive a 4-segment LED display for remaining capacity indication and/or a permanent fail (PF) error code indication.

9.3.7 Internal Temperature Sensor

An internal temperature sensor is available on the bq40z60 to reduce the cost, power, and size of the external components necessary to measure temperature. It is available for connection to the ADC using the multiplexer, and is ideal for determining pack temperature during storage and IC temperature during normal operation.

9.3.8 External Temperature Sensor Support

Each of the TSx input pins can be enabled with an 18-kΩ (Typ.) linearization pullup resistor to support using a 10 kΩ (25°C) NTC external thermistor, such as the Semitec 103AT–2. One or more thermistors can be connected between VSS and the individual RCx pin. The analog measurement is then taken via the ADC through its input multiplexer. If a different thermistor type is required, then changes to the external support components may be required.

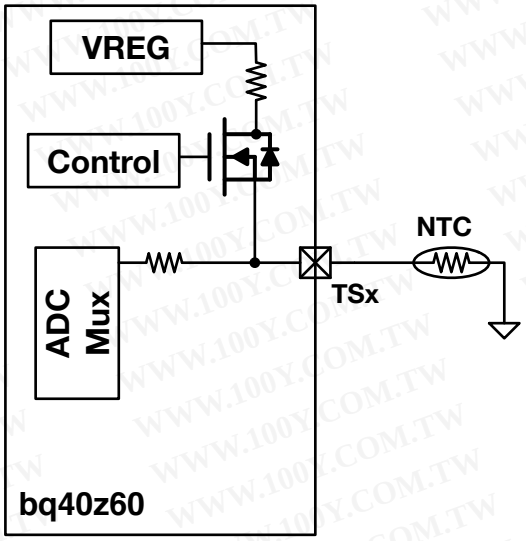


Figure 8. Thermistor Pin Configuration

9.3.9 High Frequency Oscillator

The bq40z60 includes a high frequency oscillator (HFO) running at 16.78 MHz. It is synthesized from the LFO output and scaled down to 8.388 MHz with 50% duty cycle. There is no need for external oscillator components.

9.3.10 Communications

The bq40z60 uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

9.3.10.1 SMBus On and Off State

The bq40z60 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

Feature Description (continued)

9.3.10.2 SBS Commands

The *ManufacturerAccess()* Command List shows the supported Manufacturer Access and SBS commands. See the *bq40z60 Technical Reference Manual* (SLUUA04) for further details.

Feature Description (continued)

Table 1. ManufacturerAccess() Command List

FUNCTION	MANUFACTURER ACCESS COMMAND	SBS COMMAND	ACCESS	FORMAT	DATA READ ON 0x44 OR 0x23	AVAILABLE IN SEALED MODE
DeviceType	0x0001		R	Block	Yes	Yes
FirmwareVersion	0x0002		R	Block	Yes	Yes
HardwareVersion	0x0003		R	Block	Yes	Yes
IFChecksum	0x0004		R	Block	Yes	Yes
StaticDFSignature	0x0005		R	Block	Yes	Yes
ChemID	0x0006		R	Block	Yes	Yes
StaticChemDFSignature	0x0008		R	Block	Yes	Yes
AllDFSignature	0x0009		R	Block	Yes	Yes
ShutdownMode	0x0010		W	—	—	Yes
SleepMode	0x0011		W	—	—	—
AutoCCOfset	0x0013		W	—	—	—
FuseToggle	0x001D		W	—	—	—
PrechargeFET	0x001E		W	—	—	—
ChargeFET	0x001F		W	—	—	—
DischargeFET	0x0020		W	—	—	—
Gauging	0x0021		W	—	—	—
FETControl	0x0022		W	—	—	—
LifetimeDataCollection	0x0023		W	—	—	—
PermanentFailure	0x0024		W	—	—	—
BlackBoxRecorder	0x0025		W	—	—	—
Fuse	0x0026		W	—	—	—
LifetimeDataReset	0x0028		W	—	—	—
PermanentFailureData Reset	0x0029		W	—	—	—
LifetimeDataFlush	0x002E		W	—	—	—
LifetimeDataSpeedUp Mode	0x002F		W	—	—	—
BlackBoxRecorderReset	0x002A		W	—	—	—
CalibrationMode	0x002D		W	—	—	—
SealDevice	0x0030		W	—	—	—
SecurityKeys	0x0035		R/W	Block	Yes	—
AuthenticationKey	0x0037		R/W	Block	—	—
DeviceReset	0x0041		W	—	—	—
SafetyAlert	0x0050	0x50	R	Block	Yes	Yes
SafetyStatus	0x0051	0x51	R	Block	Yes	Yes
PFAlert	0x0052	0x52	R	Block	Yes	Yes
PFStatus	0x0053	0x53	R	Block	Yes	Yes
OperationStatus	0x0054	0x54	R	Block	Yes	Yes
ChargingStatus	0x0055	0x55	R	Block	Yes	Yes
GaugingStatus	0x0056	0x56	R	Block	Yes	Yes
ManufacturingStatus	0x0057	0x57	R	Block	Yes	Yes
AFERegister	0x0058	0x58	R	Block	Yes	Yes
LifetimeDataBlock1	0x0060	0x60	R	Block	Yes	Yes
LifetimeDataBlock2	0x0061	0x61	R	Block	Yes	Yes
LifetimeDataBlock3	0x0062	0x62	R	Block	Yes	Yes
ManufacturerInfo	0x0070	0x70	R	Block	Yes	Yes
DAStatus1	0x0071	0x71	R	Block	Yes	Yes
DAStatus2	0x0072	0x72	R	Block	Yes	Yes
GaugeStatus1	0x0073	0x73	R	Block	Yes	Yes

Feature Description (continued)

Table 1. ManufacturerAccess() Command List (continued)

FUNCTION	MANUFACTURER ACCESS COMMAND	SBS COMMAND	ACCESS	FORMAT	DATA READ ON 0x44 OR 0x23	AVAILABLE IN SEALED MODE
GaugeStatus2	0x0074	0x74	R	Block	Yes	Yes
GaugeStatus3	0x0075	0x75	R	Block	Yes	Yes
StateofHealth	0x0077		R	Block	Yes	Yes
CHGR_EN	0x00C0		W	—	—	No
CVRD_ARM	0x00C1		W	—	—	Yes
ACFETEST	0x00C2		W	—	—	No
CHGONTEST	0x00C3		W	—	—	No
ROMMode	0x0F00		W	—	—	—
ExitCalibrationOutput	0xF080		R/W	Block	Yes	—
OutputCCandADCfor Calibration	0xF081		R/W	Block	Yes	—
OutputShortedCCand ADCforCalibration	0xF082		R/W	Block	Yes	—

10 Application and Implementation

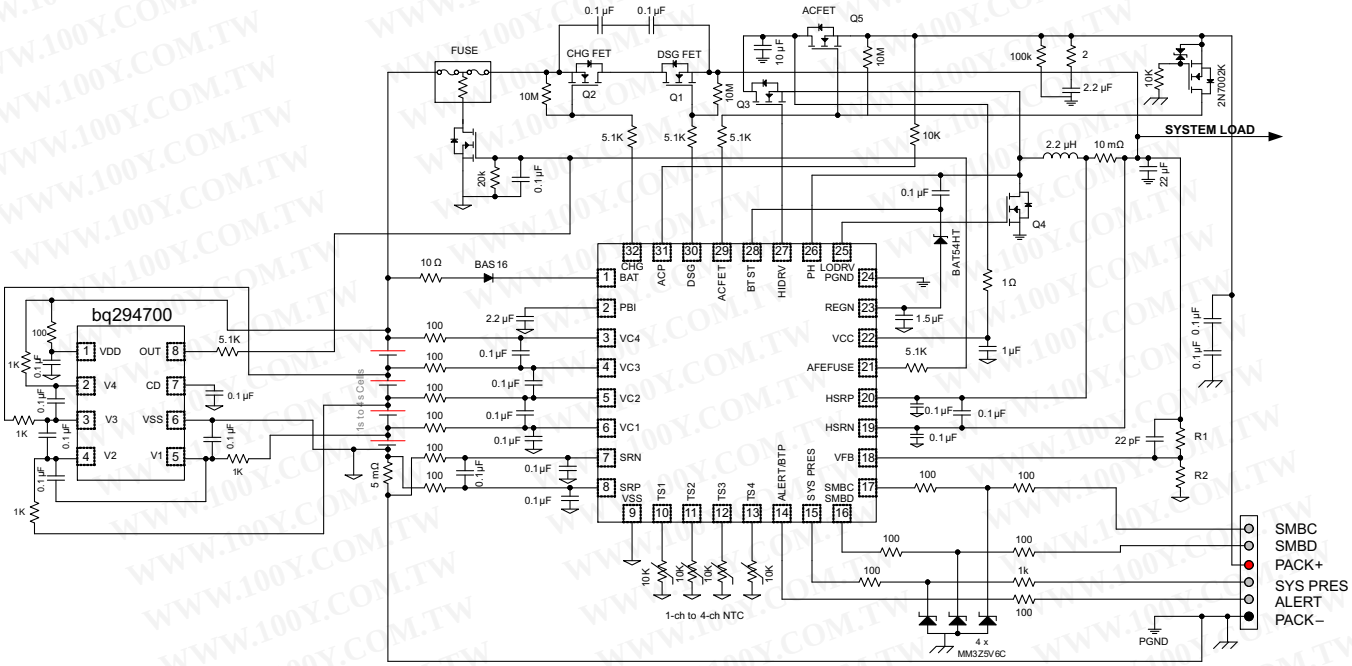
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq40z60 is a monolithic charger and gas gauge solution for multi-cell battery packs. By integrating these device together, software control can be handed off from the host microcontroller to the gas gauge controller, providing for potential energy savings that correlate to run time.

10.2 Typical Applications



Note: In 2 s to 3 s: bq2945xy is an option for second level protection.
The feedback resistor to VFB from charging output will have different values based on the number of series cells configured for the charging the pack.
4-s Cells, R1 = 332k, R2 = 26.1k
3-s Cells, R1 = 332k, R2 35.63k
2-s Cells, R1 = 332k, R2 = 56.13k
The 0.1-µF capacitors at the SRP and SRN inputs may NOT be required based on the applications, specifically, load conditions and the transition of load profiles.

Figure 9. Typical Application Schematic

NOTE

The feedback resistor to VFB from charging output will have different values based on the number of series cells configured for charging the pack.

Typical Applications (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage Range	15–22 V
3-Cell Battery Voltage Range	9 V–12.6 V
4-Cell Battery Voltage Range	12 V–16.8 V
Operating Frequency	1000 kHz

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The bq40z60 has a 1000-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (1)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_s) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{F_S \times L} \quad (2)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for a 3-cell battery pack. For 20-V adaptor voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is a 4-cell battery: The battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20%–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The bq40z60 has cycle-by-cycle charge undercurrent protection (UCP) by monitoring the charging-current sensing resistor to prevent negative inductor current. The typical UCP threshold is 5-mV falling edge corresponding to 0.5-A falling edge for a 10-mΩ charging-current sensing resistor.

10.2.2.2 Input Capacitor

The input capacitor should have enough ripple-current rating to absorb input switching ripple current. The worst-case RMS ripple current is half of the charging current when the duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst-case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated using the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (3)$$

A low-ESR ceramic capacitor such as X7R or X5R is preferred for the input-decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25-V or higher-rating capacitor is preferred for 20-V input voltage. 10-µF to 20-µF capacitance is suggested for typical of 3-A to 4-A charging current.

10.2.2.3 Output Capacitor

Output capacitor also should have enough ripple-current rating to absorb the output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (4)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{1}{8LCF_S^2}\left(V_{BAT} - \frac{V_{BAT}^2}{V_{IN}}\right) \quad (5)$$

At a certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The bq40z60 has an internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 21 kHz and 27 kHz. The preferred ceramic capacitor has a 25-V or higher rating, X7R or X5R for a 4-cell application.

10.2.2.4 Power MOSFETs Selection

Two external N-CH MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6 V of gate drive voltage. 30-V or higher voltage rating MOSFETs are preferred for 20-V input voltage, and 40 V or higher-rating MOSFETs are preferred for 20-V to 28-V input voltage.

Figure-of-merit (FOM) is usually used for selecting the proper MOSFET based on a tradeoff between the conduction loss and switching loss. For a top-side MOSFET, FOM is defined as the product of the MOSFET on-resistance, $r_{DS(on)}$, and the gate-to-drain charge, Q_{GD}. For a bottom-side MOSFET, FOM is defined as the product of the MOSFET on-resistance, $r_{DS(on)}$, and the total gate charge, Q_G.

$$FOM_{TOP} = R_{DS(ON)} \times Q_{GD} \qquad FOM_{BOTTOM} = R_{DS(ON)} \times Q \quad (6)$$

The lower the FOM value, the lower the total power loss. Usually a lower $r_{DS(on)}$ has a higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle (D = V_{OUT}/V_{IN}), charging current (I_{CHG}), the MOSFET on-resistance $t_{DS(on)}$), input voltage (V_{IN}), switching frequency (f_S), turn-on time (t_{on}), and turn-off time (t_{off}):

$$P_{TOP} = D \times I_{CHG}^2 \times R_{DS(ON)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (T_{ON} + T_{OFF}) \times F_S \quad (7)$$

The first item represents the conduction loss. Usually MOSFET $r_{DS(on)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$T_{ON} = \frac{Q_{SW}}{I_{ON}}, T_{OFF} = \frac{Q_{SW}}{I_{OFF}} \quad (8)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate-driving current, and I_{off} is the turn-off gate driving current. If the switching charge is not given in the MOSFET data sheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (9)$$

Total gate-driving current can be estimated by the REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}), and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{ON} = \frac{V_{REGN} - V_{PLT}}{R_{ON}}, I_{OFF} = \frac{V_{PLT}}{R_{OFF}} \quad (10)$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous-conduction mode:

$$P_{BOTTOM} = (1 - D) \times I_{CHG}^2 \times R_{DS(ON)} \quad (11)$$

If the HSRP–HSRN voltage decreases below 5 mV (the charger is also forced into non-synchronous mode when the average HSRP–HSRN voltage is lower than 1.7 mV), the low-side FET is turned off for the remainder of the switching cycle to prevent negative inductor current. As a result, all the freewheeling current goes through the body diode of the bottom-side MOSFET. The maximum charging current in non-synchronous mode can be up to 1.6 A (0.5 A typ) for a 10-mΩ charging-current sensing resistor, considering IC tolerance. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

MOSFET gate-driver power loss contributes to the dominant losses on the controller IC when the buck converter is switching. The combined high side and low side MOSFET gate charge, Q_{g_total}, is proportional to the power dissipation of the IC, as shown in Equation 12:

$$P_{ICLOSS\_DRIVER} = V_{IN} \cdot Q_{G\_TOTAL} \cdot F_S \quad (12)$$

Choosing FETs with a lower Q_{g_total} will reduce power loss.

10.2.2.5 Input Filter Design

During adaptor hot plug-in, the parasitic inductance and input capacitor from the adaptor cable form a second-order system. The voltage spike at the VCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an overvoltage event on the VCC pin.

There are several methods for damping or limiting the overvoltage spike during adaptor hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the overvoltage spike well below the IC maximum pin voltage rating. A high-current-capability TVS Zener diode can also limit the overvoltage level to an IC safe level. However, these two solutions may not have low cost or small size.

Figure 10 shows a cost-effective and small size solution. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the overvoltage spike is limited to a safe level. D1 is used for reverse voltage protection for the VCC pin (it can be the body diode of input ACFET). C2 is a VCC pin-decoupling capacitor and it should be placed as close as possible to the VCC pin. R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high-voltage spike. The C2 value should be less than the C1 value so R1 can be dominant over the ESR of C1 to get enough of a damping effect for hot plug-in. The R1 and R2 packages must be sized to handle inrush-current power loss according to the resistor manufacturer's datasheet. The filter component values always must be verified with the real application, and minor adjustments may be needed to fit in the real application circuit.

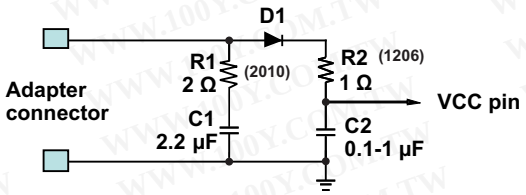
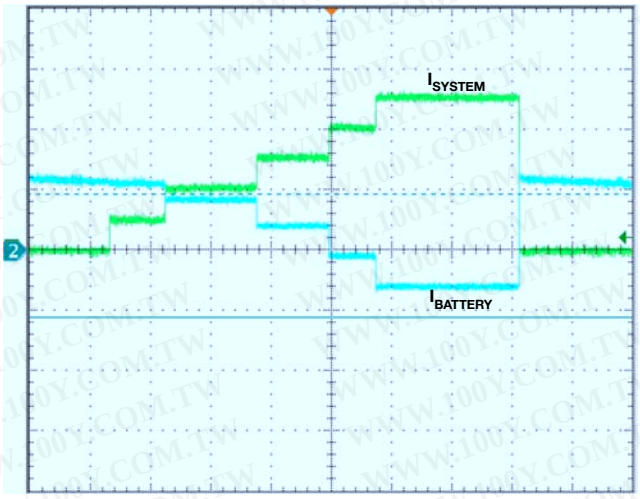


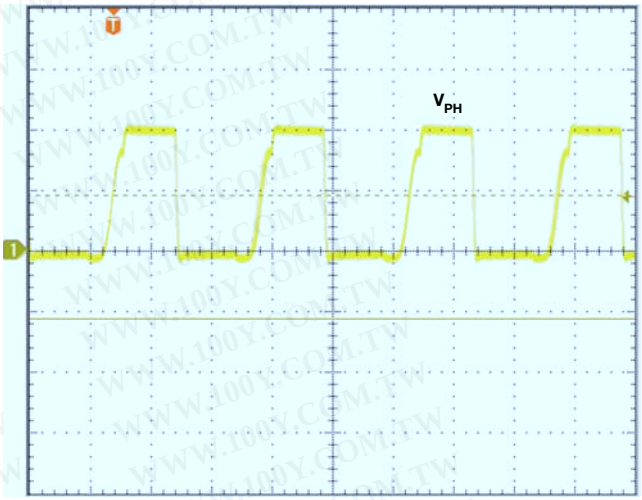
Figure 10. Input Filter

10.2.3 Application Curves



1 A/div (on both channels)
4 s/div Timescale

Figure 11. Battery Current with Load Steps



10 V/div
400 ns/div Timescale

Figure 12. Charge Controller Phase (Switch) Node Operation During Constant Current Charging

11 Power Supply Recommendations

The bq40z60 is designed to operate from a well-regulated input voltage supply range between 4.0 V and 25 V; however, with a multi-cell pack, the input voltage should be a minimum of 1 V above the maximum stack voltage. If the input supply is more than a few inches from the bq40z60, additional bulk capacitance, in the form of a 47-µF electrolytic capacitor, should be used.

12 Layout

12.1 Layout Guidelines

The following information is related to external component selection and guidelines for PCB layout.

12.1.1 PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high-frequency current-path loop (see Figure 13) is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. The following is a PCB layout priority list for proper layout. Layout of the PCB according to this specific order is essential.

1. Place the input capacitor as close as possible to the switching MOSFET supply and ground connections and use the shortest possible copper trace connection. The capacitors should be placed on the same layer as the FETs instead of using vias to connect the capacitor and the FETs. Additionally, any vias connecting the input capacitor to the adaptor node should not be placed between the capacitor and the FETs; the capacitor should have a solid copper path to the FET.
2. The IC should be placed close to the switching MOSFET gate pins to keep the gate-drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB from the switching MOSFETs.
3. Place the inductor input pin as close as possible to the switching MOSFET output pin. Minimize the copper area of this trace to lower electrical and magnetic field radiation, but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging-current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 14 for Kelvin connection for best current accuracy). Place the decoupling capacitor on these traces next to the IC.
5. Place the output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Place the sense resistor and filter components, R1, C2, and C3, as close as possible to the IC and directly adjacent to the decoupling capacitor between HSRN and HSRP.
8. Route the analog ground separately from the power ground and use a single ground connection to tie the charger power ground to the charger analog ground. Just beneath the IC, use the copper-pour for analog ground, but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground to GND. Connect analog ground and power ground together using the thermal pad as the single ground connection point. Or use a 0-Ω resistor to tie analog ground to power ground (thermal pad should tie to analog ground in this case). A star connection under the thermal pad is highly recommended.
9. It is critical that the exposed thermal pad on the back side of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC connecting to the ground plane on the other layers.
10. Place decoupling capacitors next to the IC pins and make the trace connection as short as possible.
11. Size and number of all vias should be enough for a given current path.

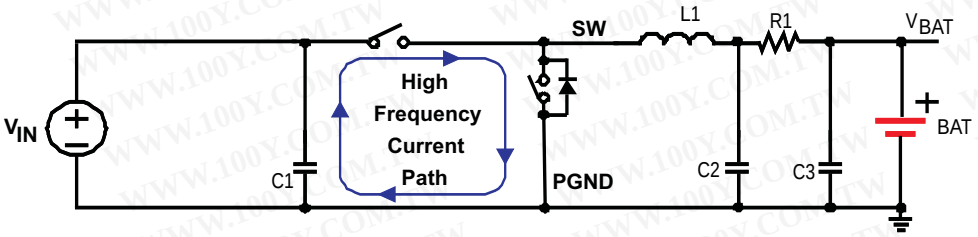


Figure 13. High-Frequency Current Path

Layout Guidelines (continued)

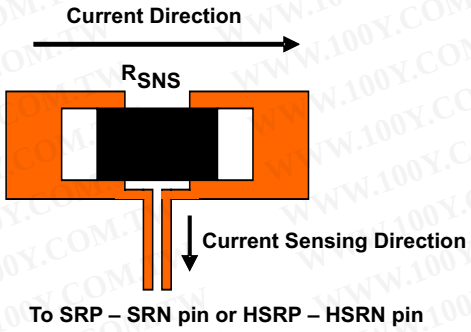


Figure 14. Sensing Resistor PCB Layout

For the recommended component placement with trace and via locations, see the *bq40z60EVM SBS 1.1 Impedance Track™ Technology Enabled Battery Management Solution Evaluation Module User's Guide* (SLUUB71) .

For the QFN information, see the *Quad Flatpack No-Lead Logic Packages Application Note* (SCBA017) and the *QFN/SON PCB Attachment Application Note* (SLUA271).

12.2 Layout Example

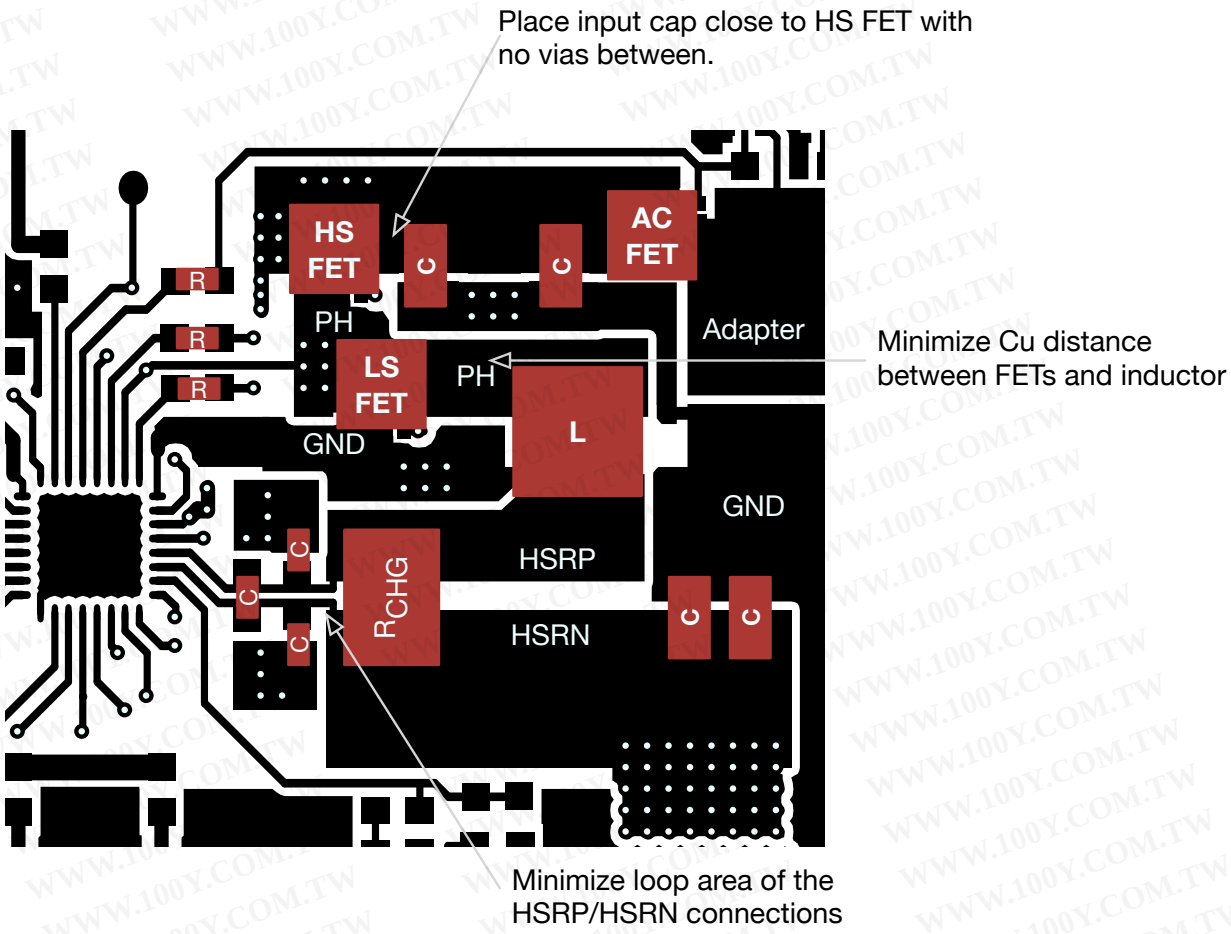


Figure 15. Board Layout Example

13 Device and Documentation Support

13.1 Related Documentation

For related documentation, see the *bq40z60 Technical Reference Manual* (SLUUA04).

13.2 Trademarks

13.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ40Z60RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z60	Samples
BQ40Z60RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z60	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

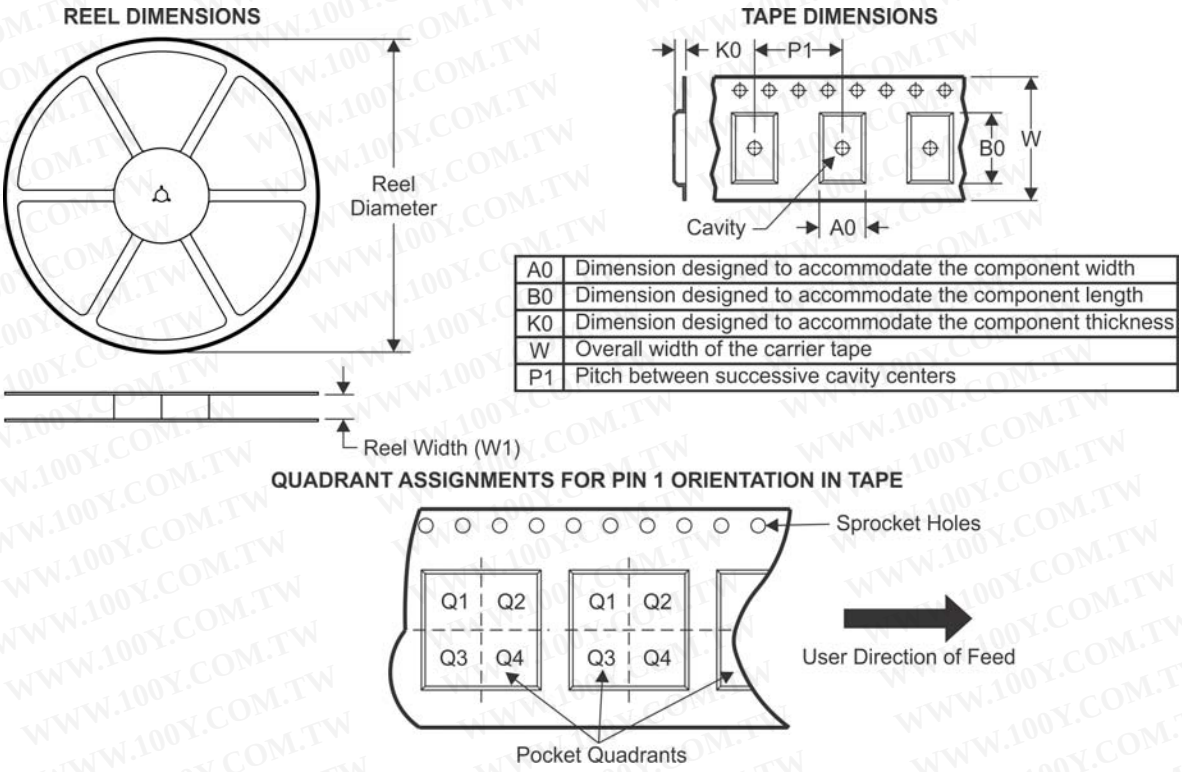
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

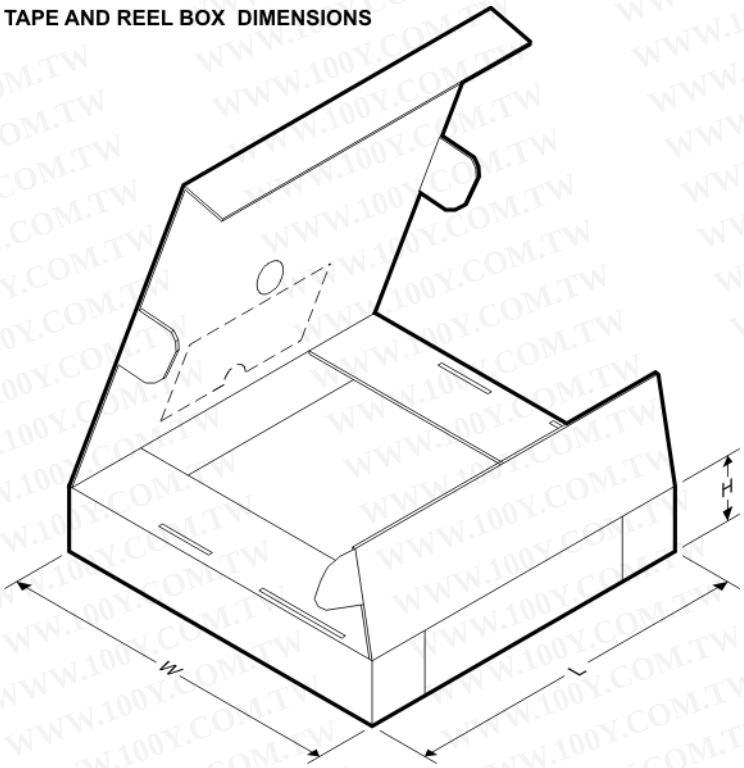


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ40Z60RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
BQ40Z60RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

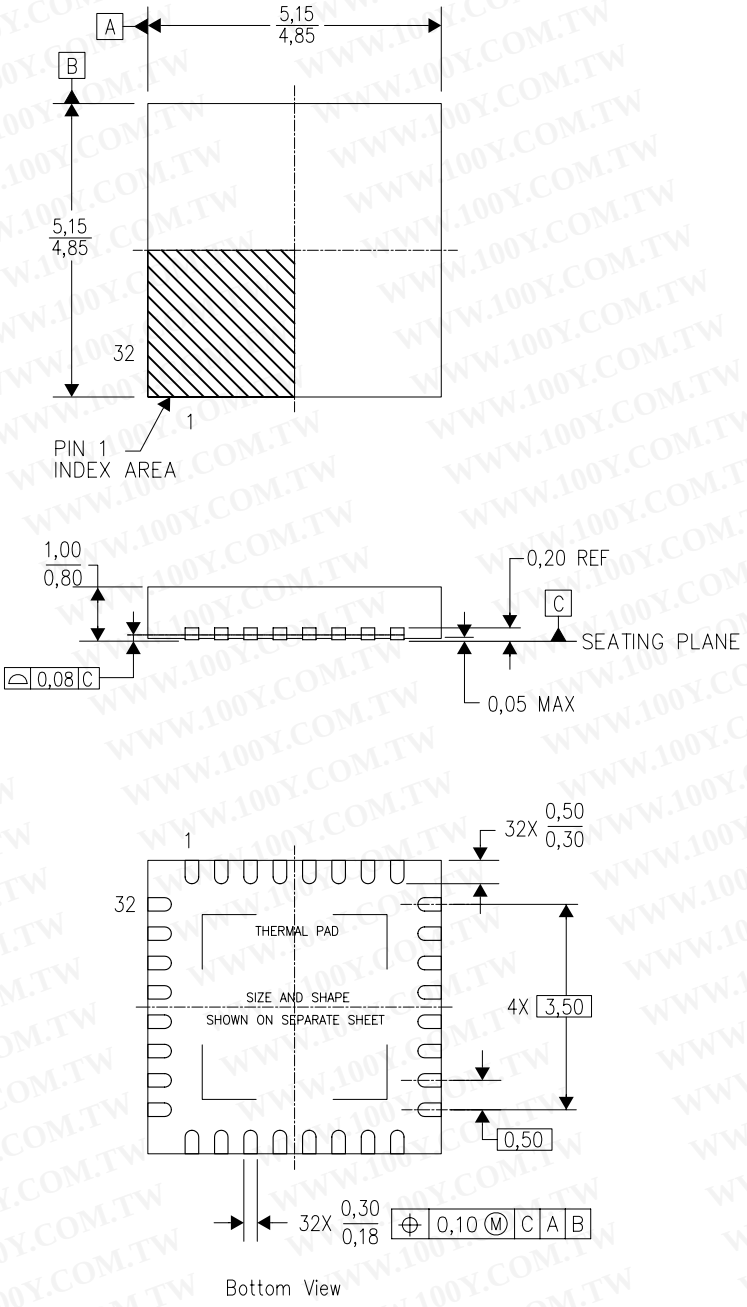
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ40Z60RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
BQ40Z60RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4204326/D 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

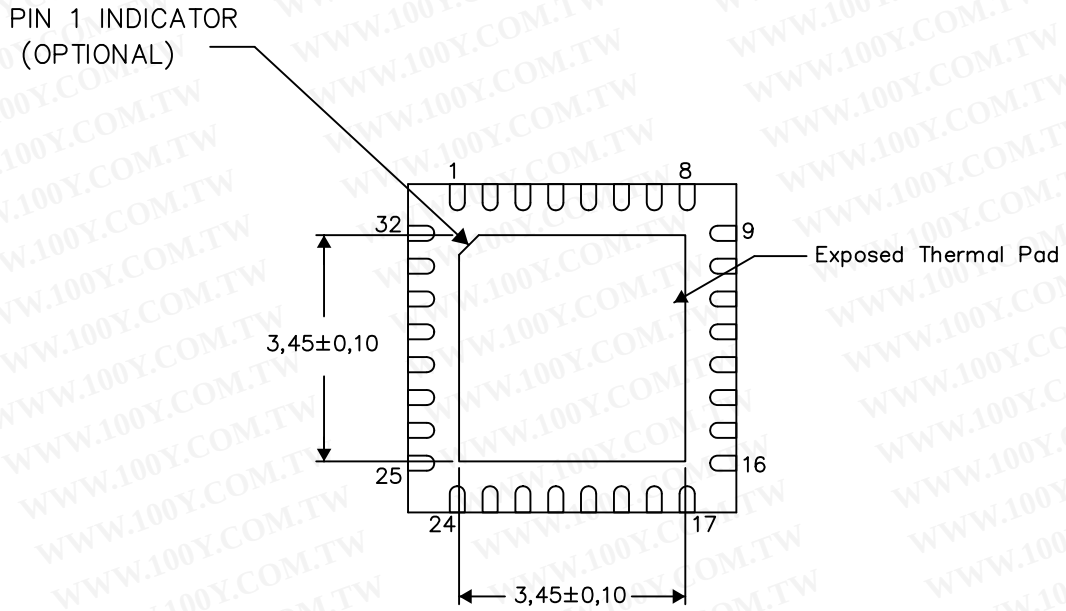
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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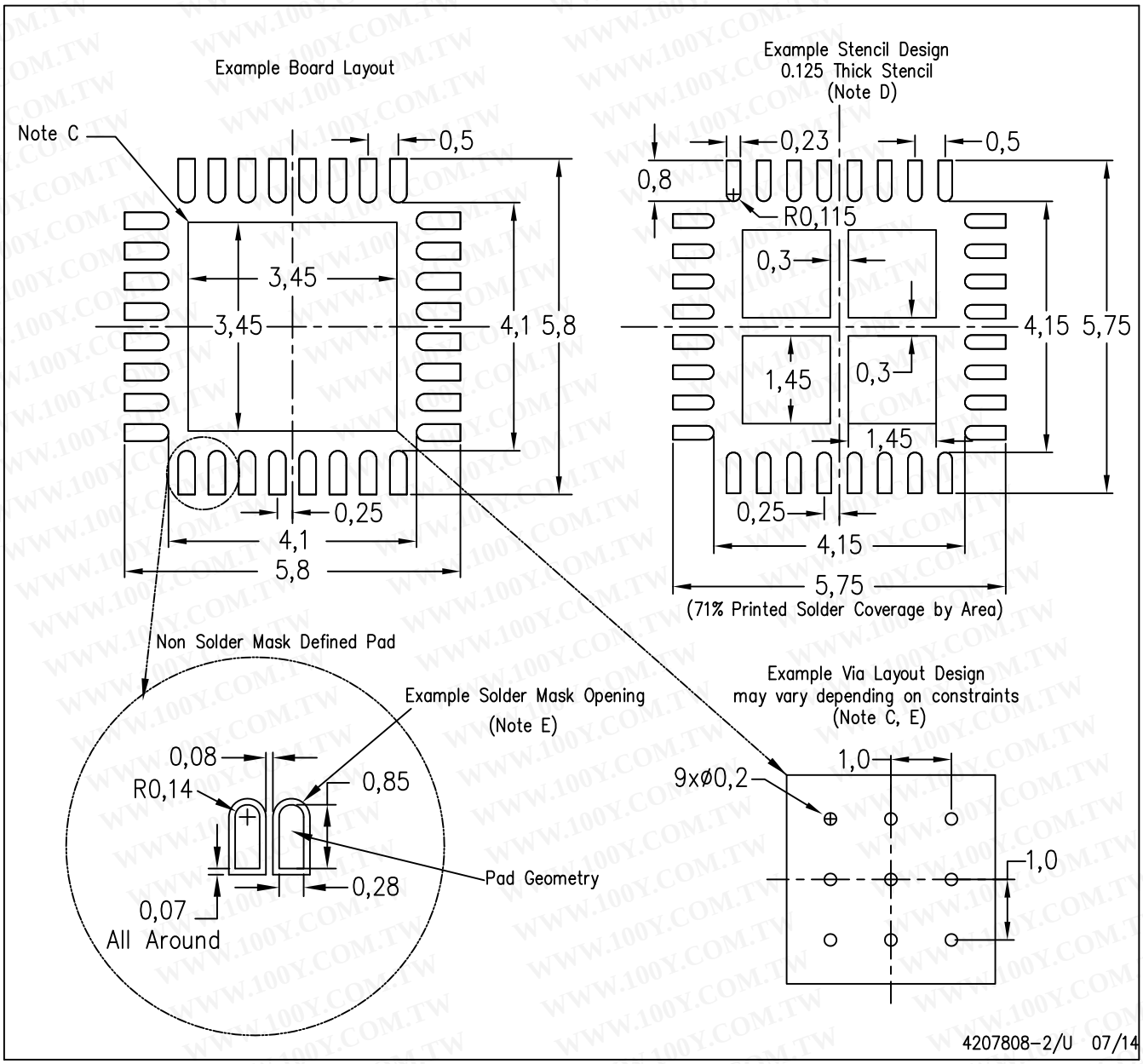
NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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