HIGH EFFICIENCY SINGLE INDUCTOR BUCK-BOOST CONVERTER WITH 4-A SWITCHES

Check for Samples: TPS63020, TPS63021

FEATURES

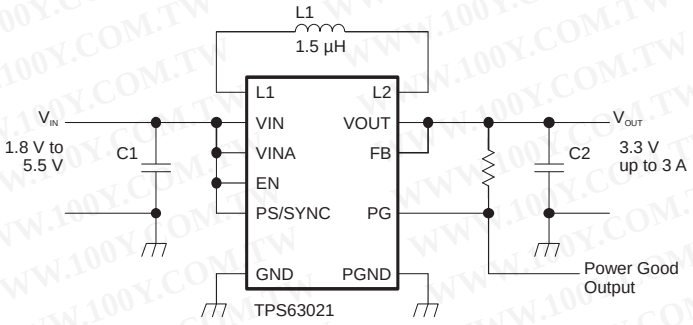
- **Up to 96% Efficiency**
- **3A Output Current at 3.3V in Step Down Mode (VIN = 3.6V to 5.5V)**
- **More than 2A Output Current at 3.3V in Boost Mode (VIN > 2.5V)**
- **Automatic Transition Between Step Down and Boost Mode**
- **Dynamic Input Current Limit**
- **Device Quiescent Current less than 50μA**
- **Input Voltage Range: 1.8V to 5.5V**
- **Fixed and Adjustable Output Voltage Options from 1.2V to 5.5V**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Forced Fixed Frequency Operation at 2.4MHz and Synchronization Possible**
- **Smart Power Good Output**
- **Load Disconnect During Shutdown**
- **Overtemperature Protection**
- **Overvoltage Protection**
- **Available in a 3 × 4-mm, QFN-14 Package**

APPLICATIONS

- **All Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products**
- **Ultra Mobile PC's and Mobile Internet Devices**
- **Digital Media Players**
- **DSC's and Camcorders**
- **Cellular Phones and Smartphones**
- **Personal Medical Products**
- **Industrial Metering Equipment**
- **High Power LED's**

DESCRIPTION

The TPS6302x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. Output currents can go as high as 3A while using a single-cell Li-Ion or Li-Polymer Battery, and discharge it down to 2.5V or lower. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save mode to maintain high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 4A. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 14-pin QFN PowerPAD™ package measuring 3 × 4 mm (DSJ).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE MARKING	PACKAGE	PART NUMBER(2)
–40°C to 85°C	Adjustable	PS63020	14-Pin QFN	TPS63020DSJ
	3.3 V	PS63021		TPS63021DSJ

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, VINA, L1, L2, VOUT, PS/SYNC, EN, FB, PG	–0.3	7	V
Temperature range	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C
ESD rating(3)	Human Body Model - (HBM)		3	kV
	Machine Model - (MM)		200	V
	Charge Device Model - (CDM)		1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS63020, TPS63021 DSJ 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	41.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance (3)	47	
θ_{JB}	Junction-to-board thermal resistance (4)	17	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter (6)	16.8	
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance (7)	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VIN, VINA	1.8		5.5	V
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

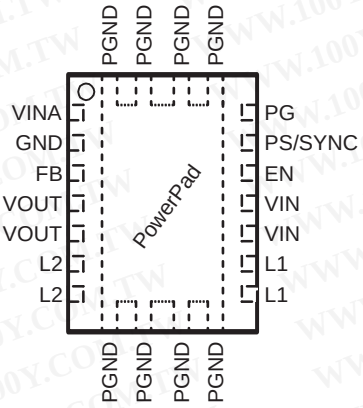
ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_I	Input voltage range			1.8		5.5	V
	Minimum input voltage for startup		0°C ≤ T_A ≤ 85°C	1.5	1.8	1.9	V
	Minimum input voltage for startup			1.5	1.8	2.0	V
V_O	TPS63020 output voltage range			1.2		5.5	V
	Minimum duty cycle in step down conversion				30%	40%	
V_{FB}	TPS63020 feedback voltage			495	500	505	mV
	TPS63021 output voltage		PS/SYNC = VIN	3.267	3.3	3.333	V
	Maximum line regulation				0.5%		
	Maximum load regulation				0.5%		
f	Oscillator frequency			2200	2400	2600	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average switch current limit		V_{IN} = V_{INA} = 3.6 V, T_A = 25°C	3500	4000	4500	mA
	High side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
	Low side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
I_q	Quiescent current	VIN and VINA	I_O = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V		25	50	µA
		VOUT			5	10	µA
	TPS63021 FB input impedance		V_{EN} = HIGH		1		MΩ
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V		0.1	1	µA
CONTROL STAGE							
UVLO	Under voltage lockout threshold		V_{INA} voltage decreasing	1.4	1.5	1.6	V
	Under voltage lockout hysteresis				200		mV
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped to GND or VINA		0.01	0.1	µA
	PG output low voltage		V_{OUT} = 3.3 V, I_{PGL} = 10 µA		0.04	0.4	V
	PG output leakage current				0.01	0.1	µA
	Output overvoltage protection			5.5		7	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

PIN ASSIGNMENTS

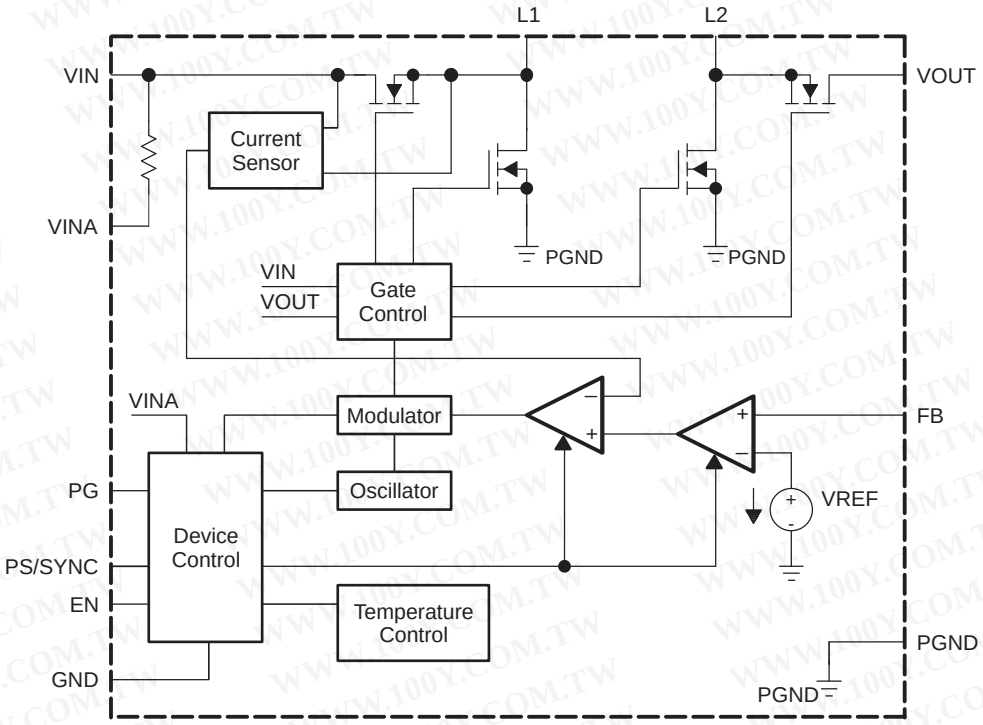
DSJ PACKAGE
(TOP VIEW)



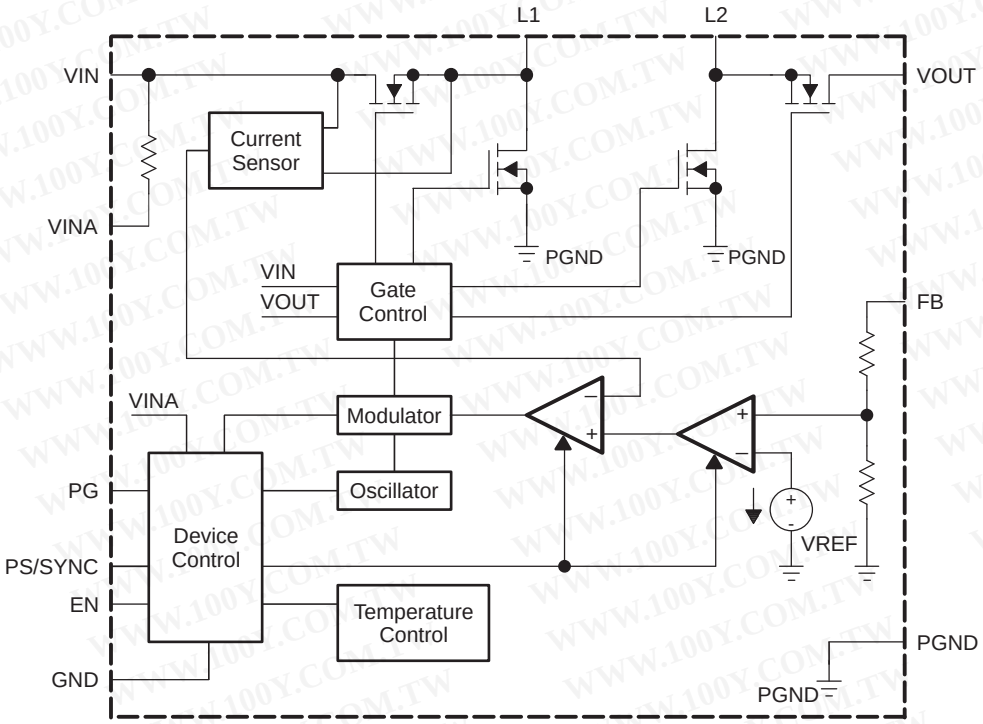
Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
EN	12	I	Enable input (1 enabled, 0 disabled) , must not be left open
FB	3	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	2		Control / logic ground
L1	8, 9	I	Connection for Inductor
L2	6, 7	I	Connection for Inductor
PS/SYNC	13	I	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization), must not be left open
PG	14	O	Output power good (1 good, 0 failure; open drain)
PGND	PowerPAD™		Power ground
VIN	10, 11	I	Supply voltage for power stage
VOUT	4, 5	O	Buck-boost converter output
VINA	1	I	Supply voltage for control stage
PowerPAD™			Must be connected to PGND. Must be soldered to achieve appropriate power dissipation.

FUNCTIONAL BLOCK DIAGRAM (TPS63020)



FUNCTIONAL BLOCK DIAGRAM (TPS63021)



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

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Efficiency	vs Output current (TPS63020, Power Save Enabled, V_{OUT} = 2.5 V / V_{OUT} = 4.5 V)	3
	vs Output current (TPS63020, Power Save Disabled, V_{OUT} = 2.5V / V_{OUT} = 4.5V)	4
	vs Output current (TPS63021, Power Save Enabled, V_{OUT} = 3.3V)	5
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	vs Input voltage (TPS63020, Power Save Enabled, V_{OUT} = 2.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	7
	vs Input voltage (TPS63020, Power Save Enabled, V_{OUT} = 4.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	8
	vs Input voltage (TPS63020, Power Save Disabled, V_{OUT} = 2.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	9
	vs Input voltage (TPS63020, Power Save Disabled, V_{OUT} = 4.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	10
	vs Input voltage (TPS63021, Power Save Enabled, V_{OUT} = 3.3V, I_{OUT} = {10; 500; 1000; 2000 mA})	11
	vs Input voltage (TPS63021, Power Save Disabled, V_{OUT} = 3.3V, I_{OUT} = {10; 500; 1000; 2000 mA})	12
Output voltage	vs Output current (TPS63020, V_{OUT} = 2.5 V)	13
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	Startup after enable (TPS63021, V_{OUT} = 3.3V, V_{IN} = 4.2V, I_{OUT} = 1500mA)	20

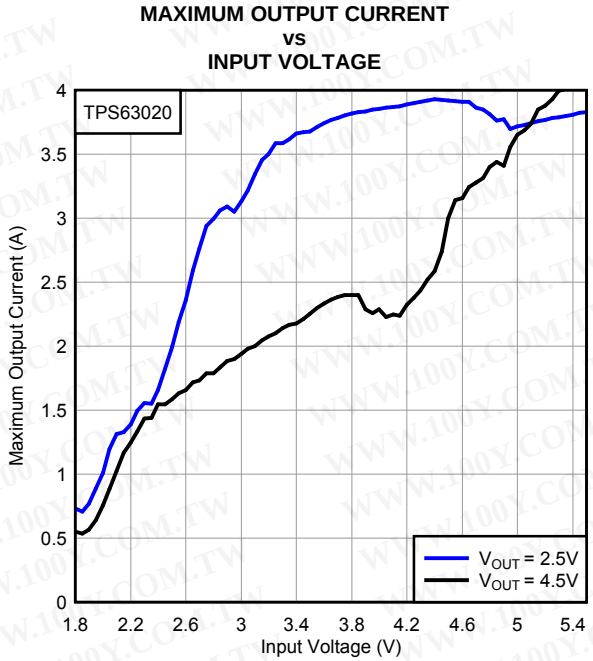


Figure 1.

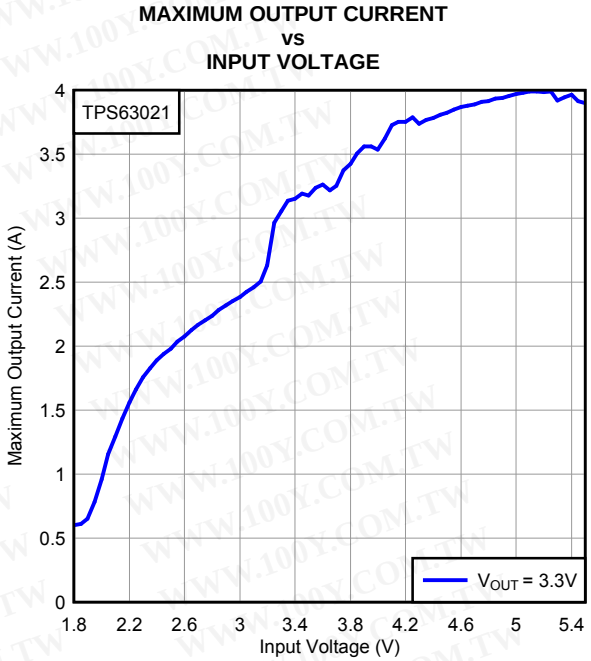
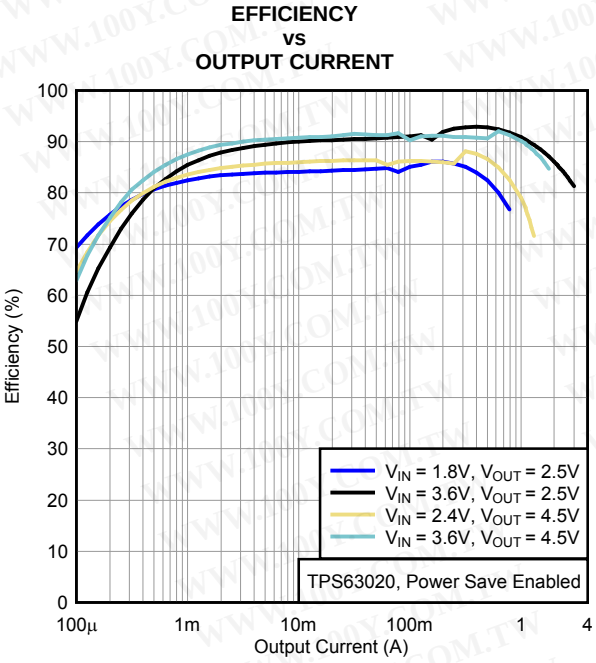


Figure 2.



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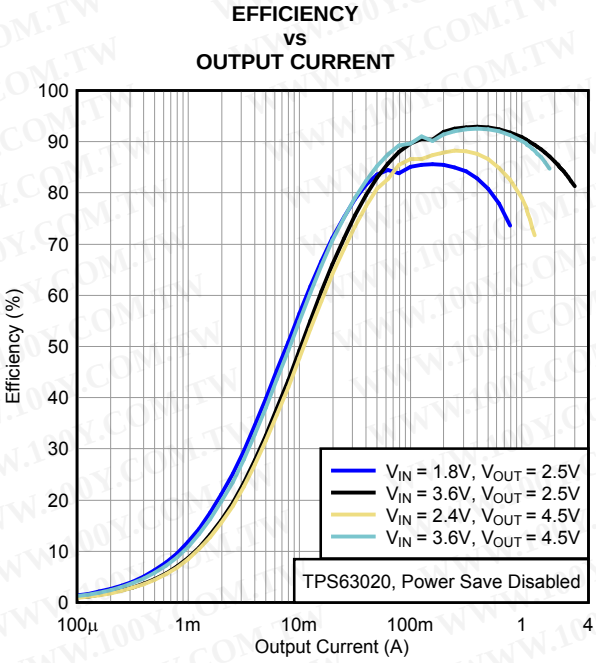

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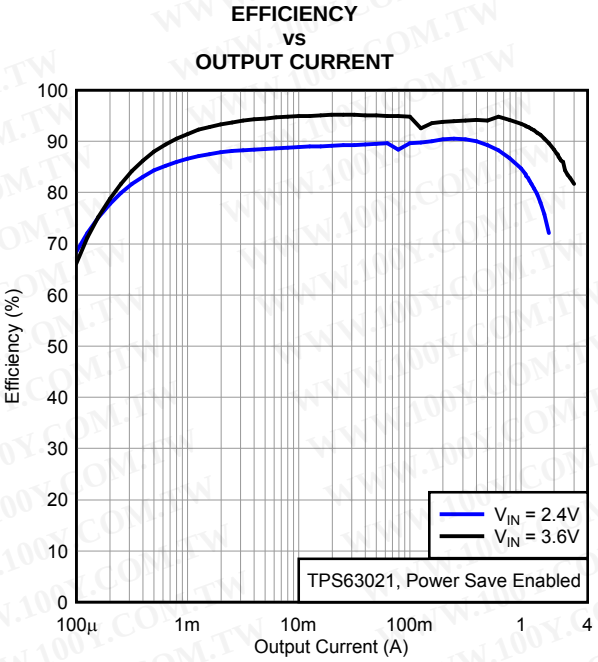

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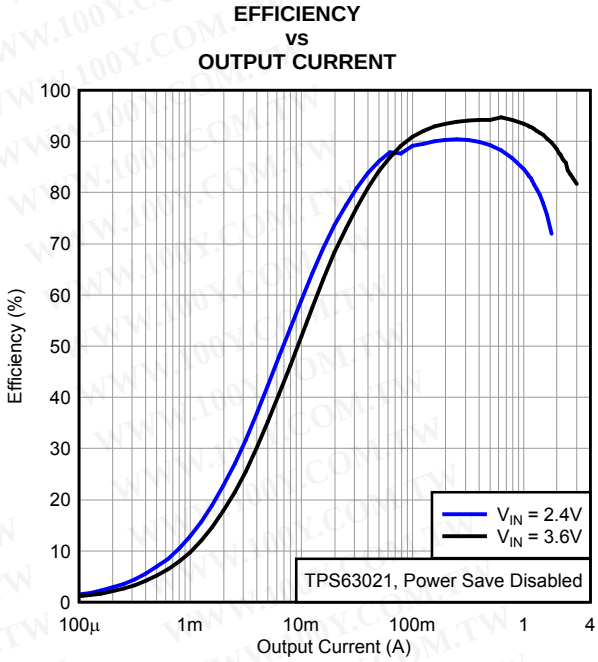

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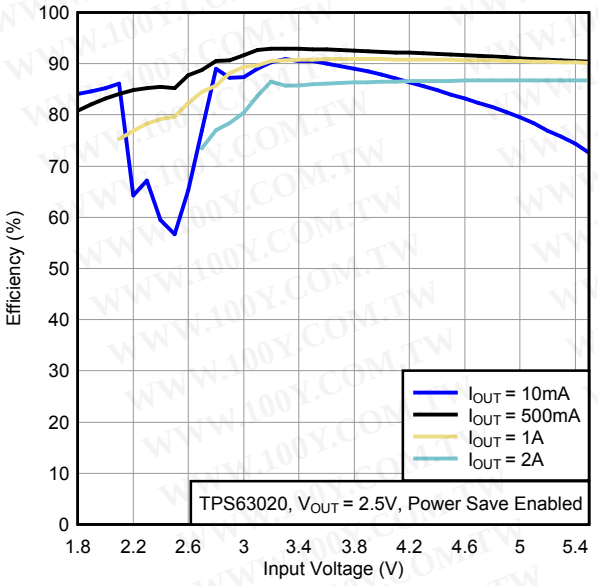

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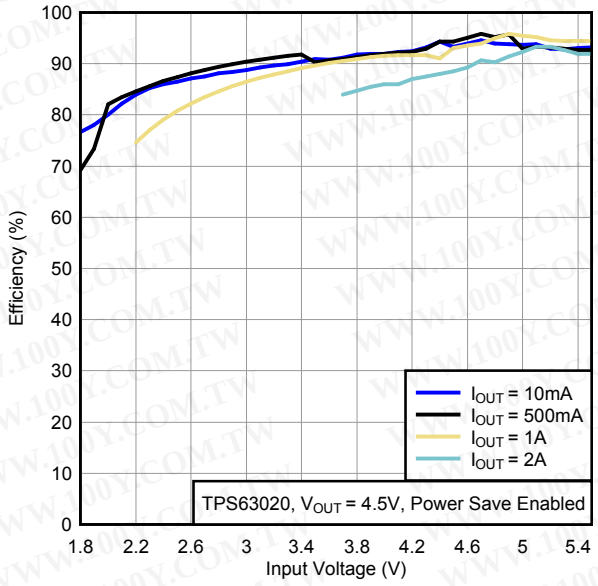

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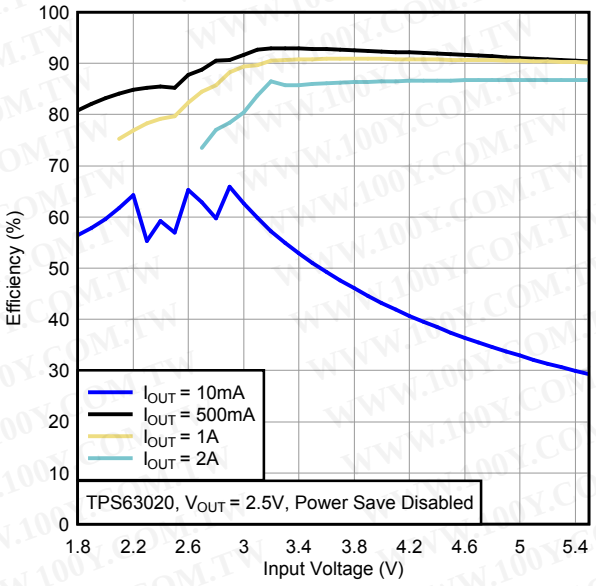


Figure 9.

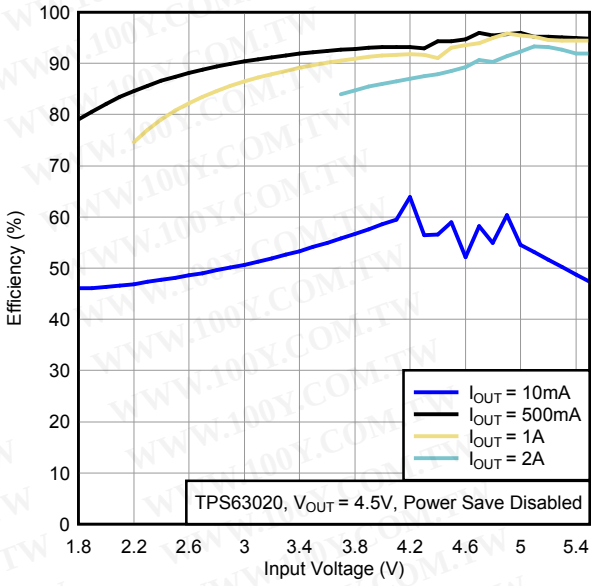
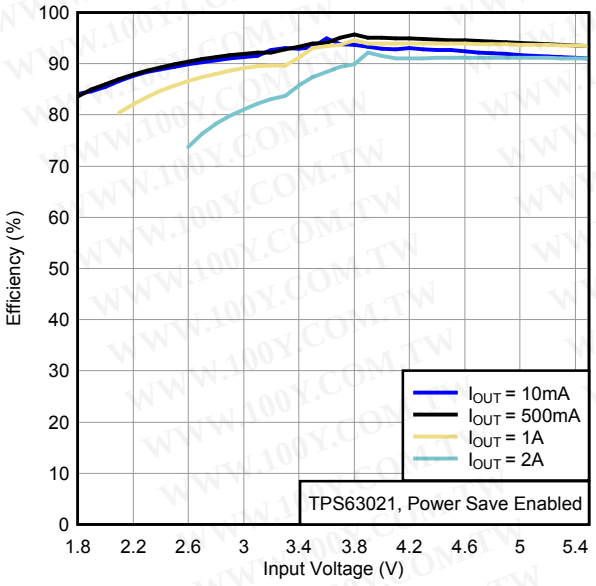


Figure 10.



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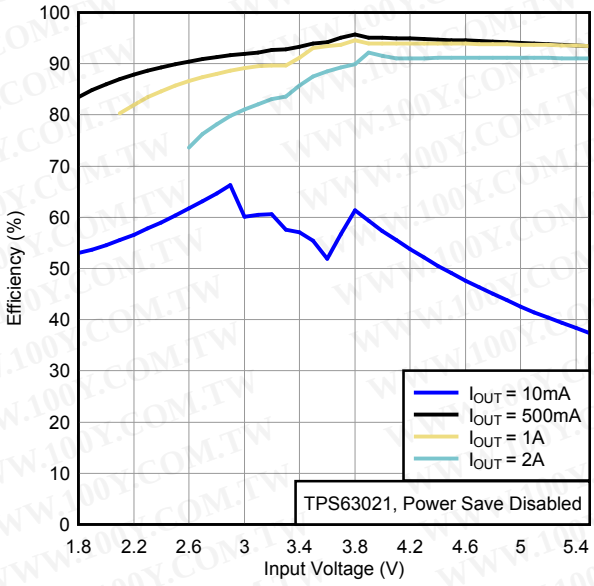

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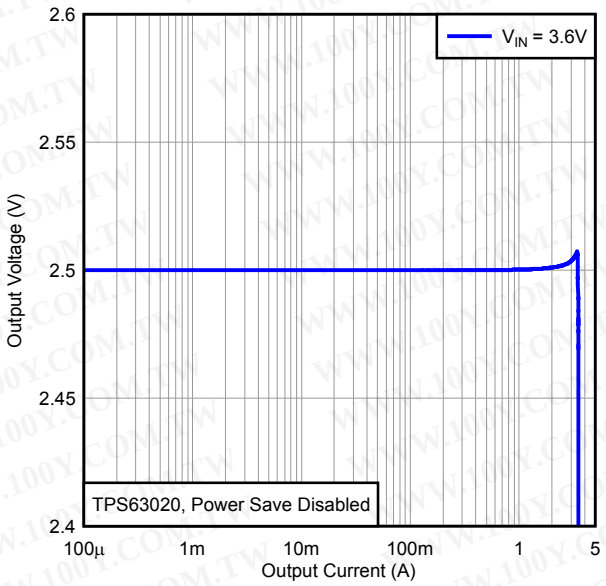
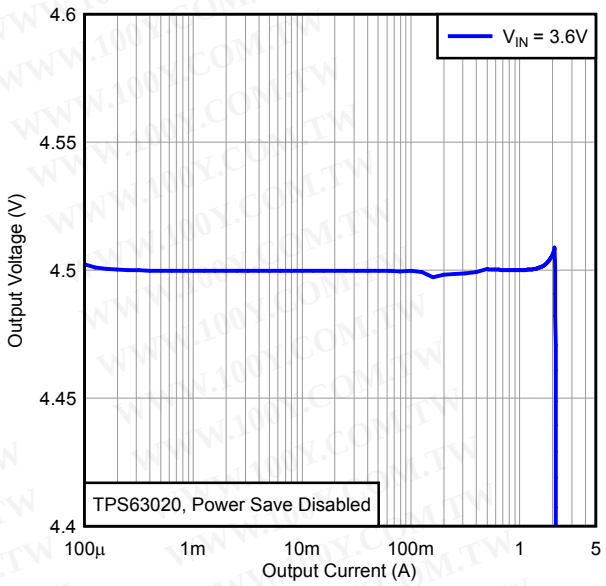


Figure 13.



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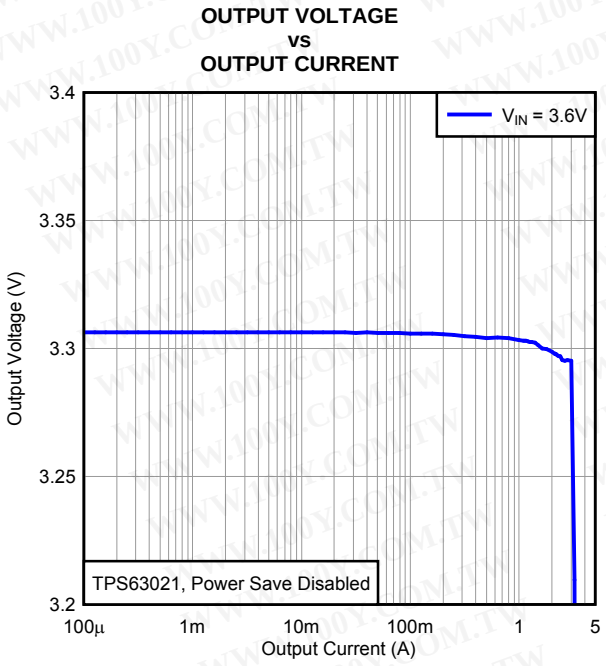

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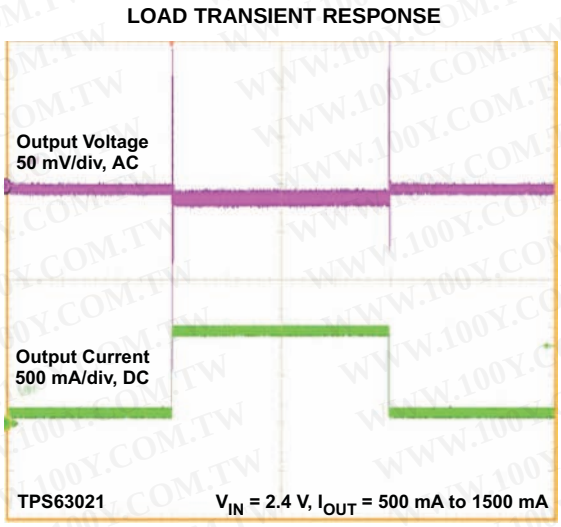
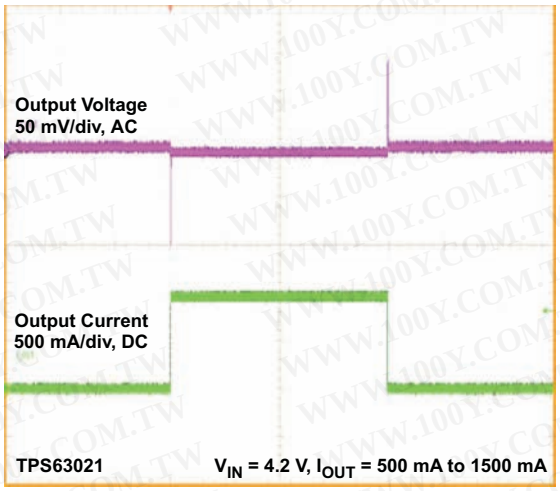


Figure 16.

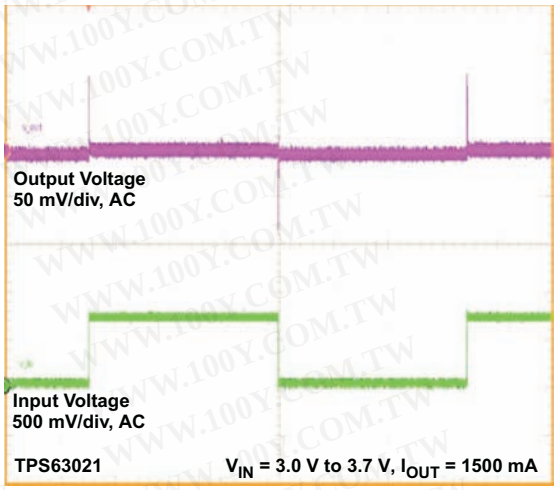
LOAD TRANSIENT RESPONSE



Time 2 ms/div

Figure 17.

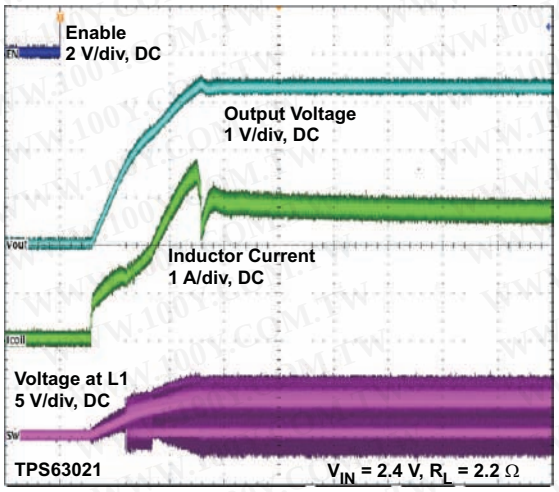
LINE TRANSIENT RESPONSE



Time 2 ms/div

Figure 18.

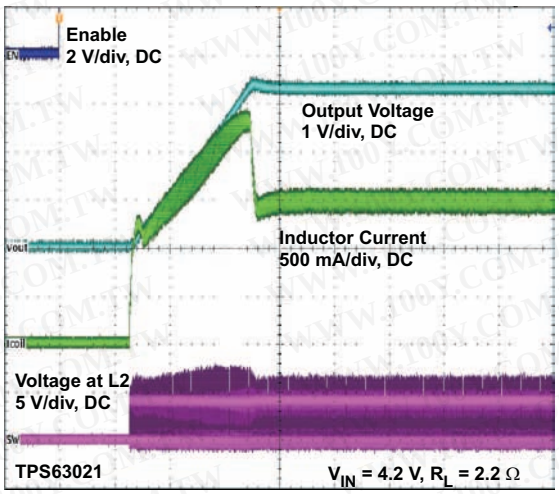
STARTUP AFTER ENABLE



Time 100 μs/div

Figure 19.

STARTUP AFTER ENABLE



Time 40 μs/div

Figure 20.

PARAMETER MEASUREMENT INFORMATION

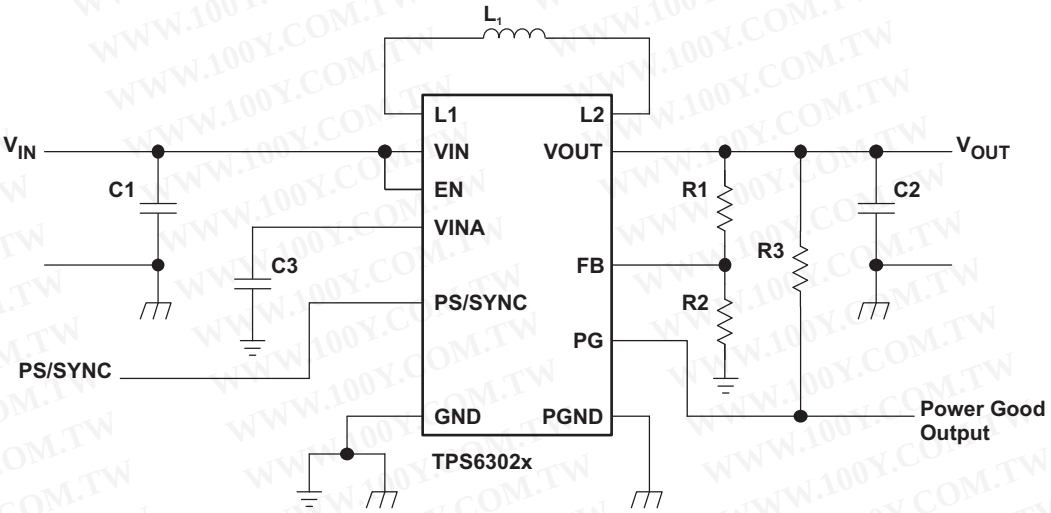


Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63020 or TPS63021	Texas Instruments
L1	1.5 µH, 4 mm x 4 mm x 2 mm	XFL4020-152ML, Coilcraft
C1	2 × 10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME84D, Murata
C2	3 × 10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME84D, Murata
C3	0.1 µF, X7R ceramic	
R1	Depending on the output voltage at TPS63020, 0 Ω at TPS63021	
R2	Depending on the output voltage at TPS63020, not used at TPS63021	
R3	1 MΩ	

DETAILED DESCRIPTION

CONTROLLER CIRCUIT

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The controller circuit also senses the average input current. With this, maximum input power can be controlled to achieve a safe and stable operation under all possible conditions. To protect the device from overheating, an internal temperature sensor is implemented.

Synchronous Operation

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion across all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter.

Buck-Boost Operation

To regulate the output voltage properly at all possible input voltage conditions, the device automatically switches from step down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. Switching losses are kept low by using only one active and one passive switch. For the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

Power Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. To enable power save, PS/SYNC must be set low. Power save mode is used to improve efficiency at light load. If power save mode is enabled, the converter stops operating if the average inductor current goes lower than about 100 mA and the output voltage is at or above its nominal value. If the output voltage decreases below its nominal value, the device ramps up the output voltage again by starting operation using an average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter again stops operating once the conditions for stopping operation are met again.

The power save mode can be disabled with a high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency. Synchronization is done by a PLL, so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

Dynamic Current Limit

To protect the device and the application, the average inductor current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the electrical characteristics table. If the supply voltage at VIN drops below 2.3V, the current limit is reduced. This can happen when the input power source becomes weak. Increasing output impedance, when the batteries are almost discharged, or an additional heavy pulse load is connected to the battery can cause the VIN voltage to drop. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at VIN. At this voltage, the device is forced into burst mode operation trying to stay active as long as possible even with a weak input power source.

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. Similar to the behavior when the input voltage at VIN drops, the current limit is reduced with temperature increasing.

Smart Power Good

The device has a built in power good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current is limited to a value below the current the voltage regulator demands for maintaining the output voltage the power good output goes low impedance. The output is open drain, so its logic function can be adjusted to any voltage level the connected logic is using, by connecting a pull up resistor to the supply voltage of the logic. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Softstart and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial value of about 500mA following the increasing output voltage. At an output voltage of about 1.2V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus, the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. If the output voltage does not increase above 1.2V, the device assumes a short circuit at the output and keeps the current limit low to protect itself and the application. At a short on the output during operation, the internal clock frequency and the current limit are also decreased accordingly. At 0 V on the output, the output current will be limited in the range of 400 mA.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VINA is lower than approximately its threshold (see electrical characteristics table). When in operation, the device automatically enters the shutdown mode if the voltage on VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops switching. As soon as the IC temperature has decreased below the programmed threshold, it starts switching again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6302x dc/dc converters are intended for systems powered by one-cell Li-Ion or Li-Polymer battery with a typical voltage between 2.3 V and 4.5 V. They can also be used in systems powered by a double or triple cell Alkaline, NiCd, or NiMH battery with a typical terminal voltage between 1.8V and 5.5V . Additionally, any other voltage source with a typical output voltage between 1.8V and 5.5V can power systems where the TPS6302x is used.

PROGRAMMING THE OUTPUT VOLTAGE

Within the TPS6302x family there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. For the adjustable output voltage versions, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. The maximum recommended value for the output voltage is 5.5V. The current through the resistor divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 500kΩ, in order to set the divider current at 1µA or higher. It is recommended to keep the value for this resistor in the range of 200kΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

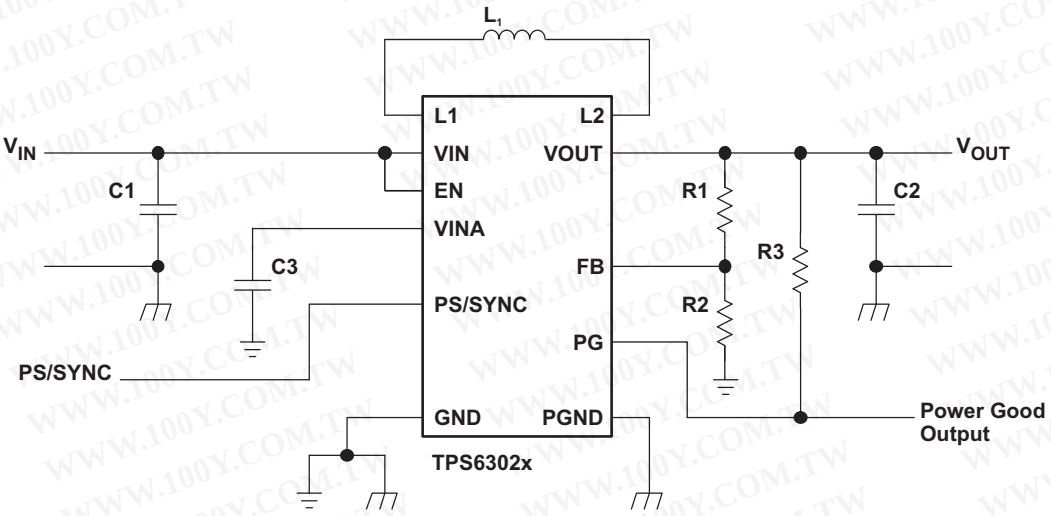


Figure 21. Typical Application Circuit for Adjustable Output Voltage Option

INDUCTOR SELECTION

To properly configure the TPS6302x devices, an inductor must be connected between pin L1 and pin L2. To estimate the inductance value, Equation 2 and Equation 3 can be used.

$$L1 = (V_{IN1} - V_{OUT}) \times 0.5 \times \frac{\mu s}{A} \quad (2)$$

$$L2 = V_{OUT} \times 0.5 \times \frac{\mu s}{A} \quad (3)$$

In Equation 2 the minimum inductance value, *L1* for step down mode operation is calculated. V_{IN1} is the

maximum input voltage. In Equation 3 the minimum inductance, *L2*, for boost mode operation is calculated. The recommended minimum inductor value is either *L1* or *L2,* whichever is higher. As an example, a suitable inductor for generating 3.3V from a Li-Ion battery with a battery voltage range from 2.5V up to 4.2V is 1.5µH. The recommended inductor value range is between 1.5µH and 4.7µH. This means that at high voltage conversion rates, higher inductor values offer better performance.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 4 shows how to calculate the peak current *I1* in step down mode operation and Equation 5 shows how to calculate the peak current *I2* in boost mode operation.

$$I1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT}(V_{IN1} - V_{OUT})}{2 \times V_{IN1} \times f \times L} \quad (4)$$

$$I2 = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN2}} + \frac{V_{IN2} \times (V_{OUT} - V_{IN2})}{2 \times V_{OUT} \times f \times L} \quad (5)$$

In both equations, *f* is the minimum switching frequency. V_{IN2} is the minimum input voltage. The critical current value for selecting the right inductor is the higher value of *I1* and *I2* . Consideration must be given to the load transients and error conditions that can cause higher inductor currents. This must be taken into account when selecting an appropriate inductor. The following inductor series from different suppliers have been used with TPS6302x converters:

Table 2. List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	XFL4020
Toko	FDV0530S

CAPACITOR SELECTION

Input Capacitor

At least a 10µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

Bypass Capacitor

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1µF is recommended. The value of this capacitor should not be higher than 0.22µF. If no capacitor is used at VINA, VINA should be connected directly to VIN.

Output Capacitor

For the output capacitor, use of small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC.

To get an estimate of the recommended minimum output capacitance, Equation 6 can be used.

$$C_{OUT} = 10 \times L \times \frac{\mu F}{\mu H} \quad (6)$$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

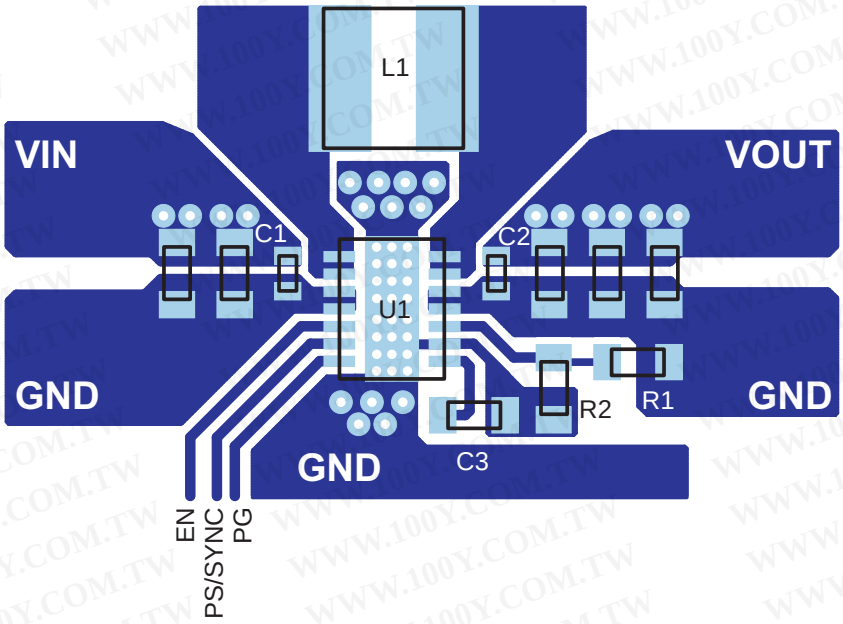


Figure 22. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and IC Package Thermal Metrics Application Note (SPRA953).

PACKAGING INFORMATION

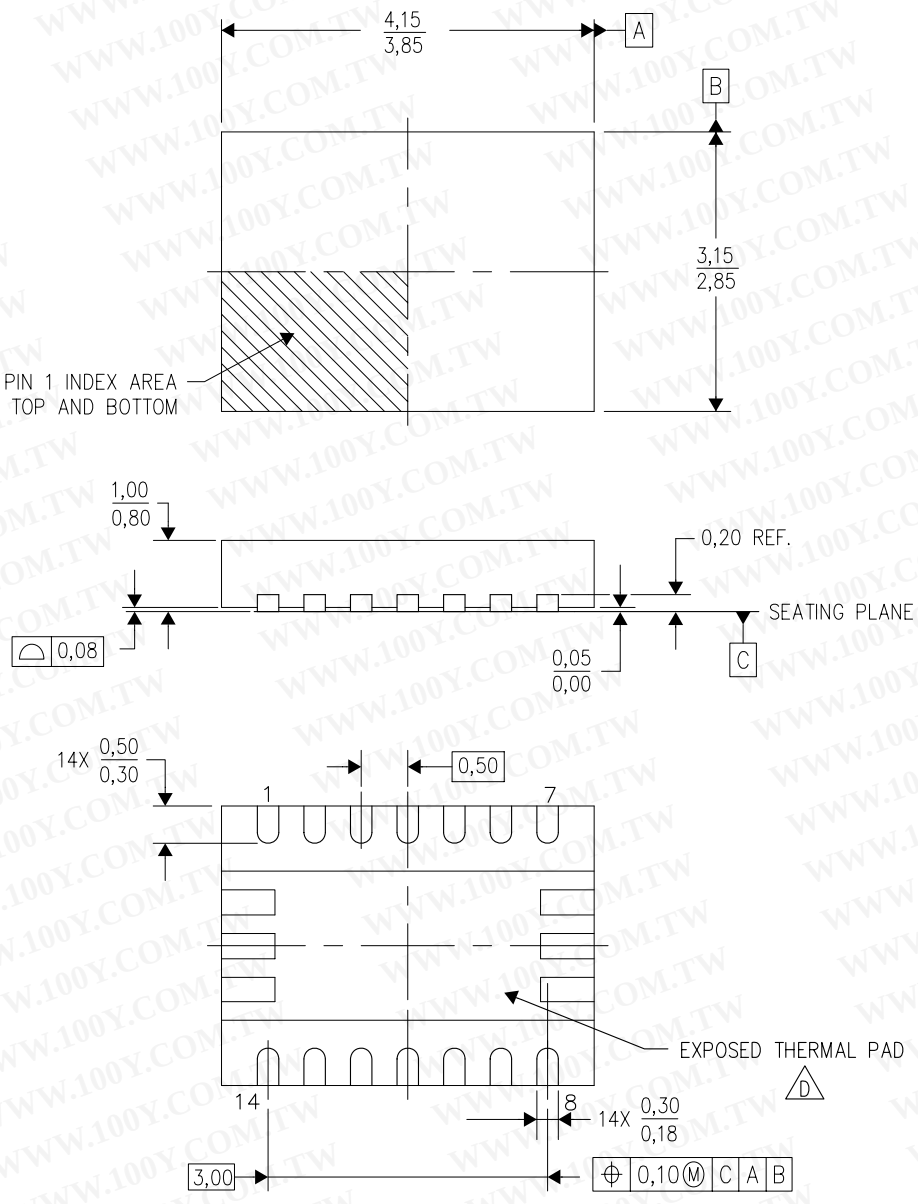
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS63020DSJR	ACTIVE	VSON	DSJ	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS63020DSJT	ACTIVE	VSON	DSJ	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS63021DSJR	ACTIVE	VSON	DSJ	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS63021DSJT	ACTIVE	VSON	DSJ	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



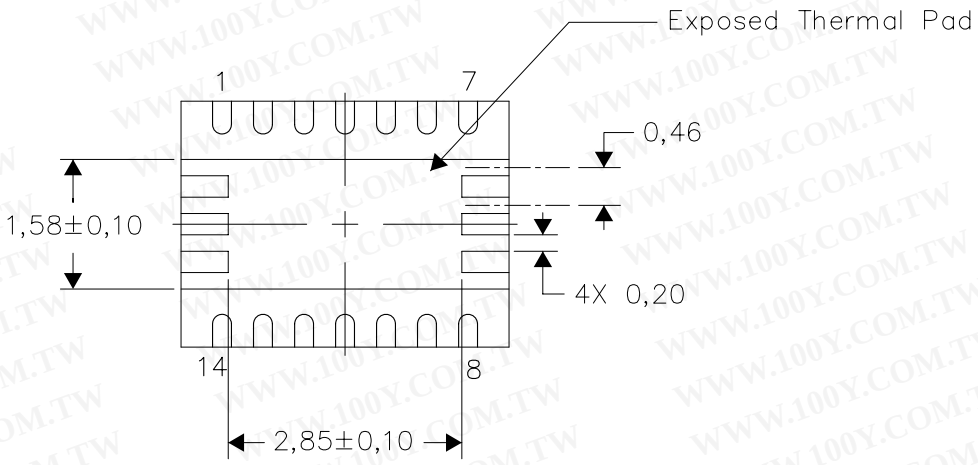
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

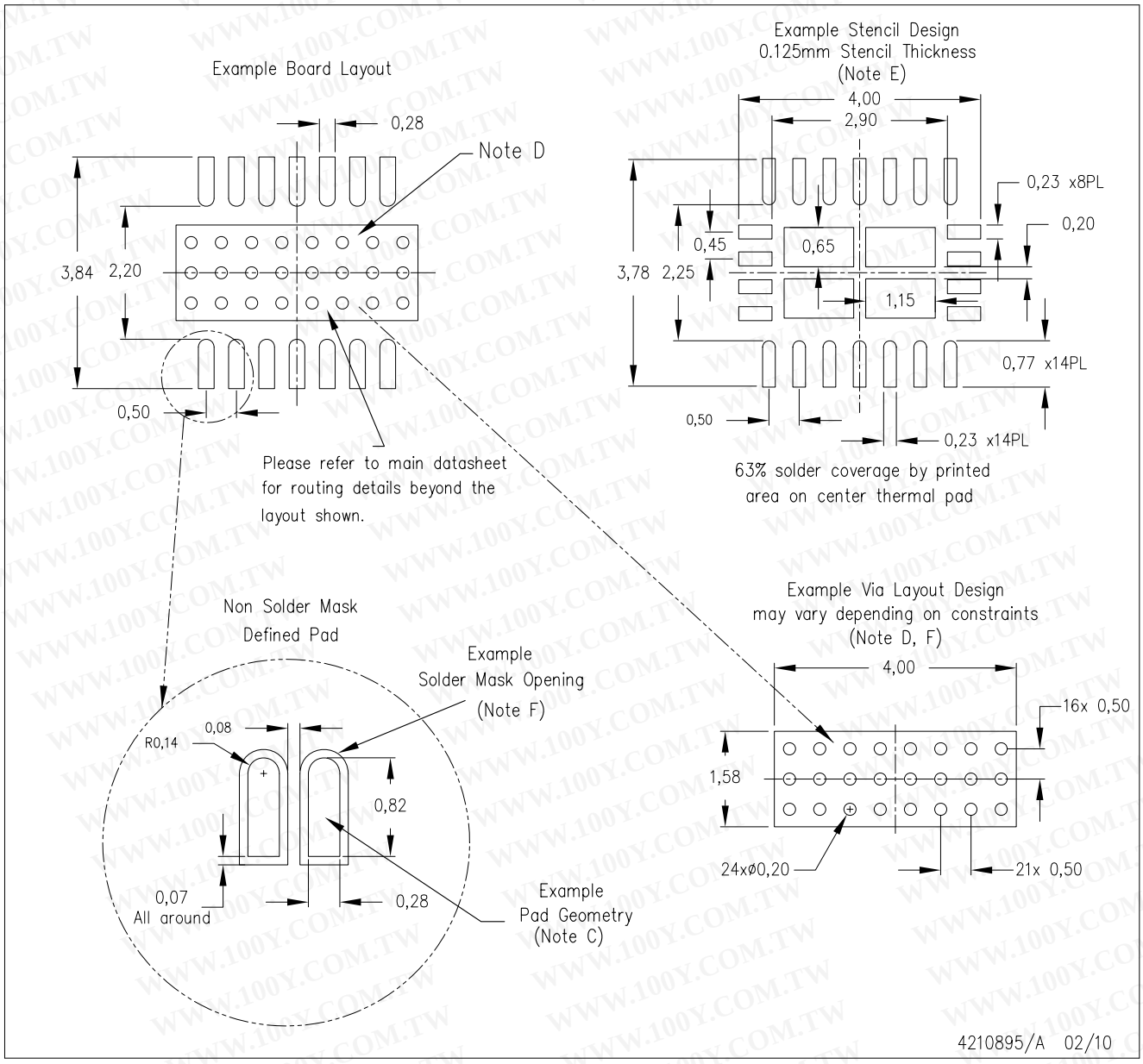


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DSJ (S-PVSON-N14) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.