

50-V Input Voltage, 50-mA, Very High Voltage LINEAR REGULATOR

 Check for Samples: [TPS7A41](#)

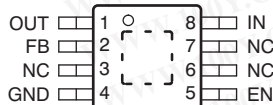
FEATURES

- **Wide Input Voltage Range: 7 V to 50 V**
- **Accuracy:**
 - **Nominal: 1%**
 - **Over Line, Load, and Temperature: 2.5%**
- **Low Quiescent Current: 25 μ A**
- **Quiescent Current at Shutdown: 4.1 μ A**
- **Maximum Output Current: 50 mA**
- **CMOS Logic-Level-Compatible Enable Pin**
- **Adjustable Output Voltage: \sim 1.175 V to 48 V**
- **Stable with Ceramic Capacitors:**
 - **Input Capacitance: \geq 1 μ F**
 - **Output Capacitance: \geq 4.7 μ F**
- **Dropout Voltage: 290 mV**
- **Built-In Current-Limit and Thermal Shutdown Protection**
- **Package: High Thermal Performance MSOP-8 PowerPAD™**
- **Operating Temperature Range: -40° C to $+125^{\circ}$ C**

APPLICATIONS

- **Microprocessors, Microcontrollers Powered by Industrial Busses with High Voltage Transients**
- **Industrial Automation**
- **Telecom Infrastructure**
- **Automotive**
- **LED Lighting**
- **Bias Power Supplies**

DGN PACKAGE
 3-mm \times 5-mm MSOP-8 PowerPAD
 (TOP VIEW)



DESCRIPTION

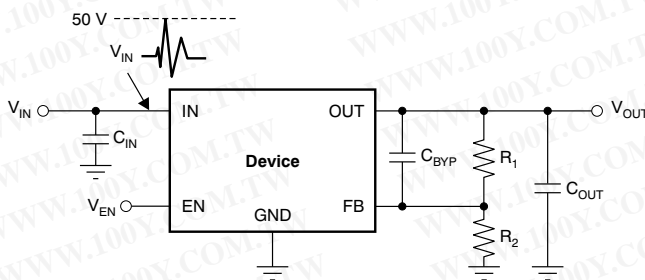
The TPS7A41 is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8), and is able to withstand continuous dc or transient input voltages of up to 50 V.

The TPS7A41 is stable with any output capacitance greater than 4.7 μ F and any input capacitance greater than 1 μ F (over temperature and tolerance). Therefore, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and a potentially small output capacitor. In addition, the TPS7A41 offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode.

The TPS7A41 has an internal thermal shutdown and current limiting to protect the system during fault conditions. The MSOP-8 packages has an operating temperature range of $T_J = -40^{\circ}$ C to $+125^{\circ}$ C.

In addition, the TPS7A41 is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only it can supply a well-regulated voltage rail, but it can also withstand and maintain regulation during very high and fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications.

Typical Application



Post DC/DC Converter Regulation for High-Performance Analog Circuitry



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT}
TPS7A4101 <i>yyy z</i>	YYY is package designator. Z is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

		VALUE		
		MIN	MAX	UNIT
Voltage	IN pin to GND pin	-0.3	+55	V
	OUT pin to GND pin	-0.3	+55	V
	OUT pin to IN pin	-55	+0.3	V
	FB pin to GND pin	-0.3	+2	V
	FB pin to IN pin	-55	+0.3	V
	EN pin to IN pin	-55	0.3	
	EN pin to GND pin	-0.3	+55	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J	-40	+125	°C
	Storage, T _{stg}	-65	+150	°C
Electrostatic discharge rating	Human body model (HBM)			2.5 kV
	Charged device model (CDM)			500 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS7A4001	UNITS
		DGN	
		8 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	55.09	°C/W
θ _{JC(top)}	Junction-to-case(top) thermal resistance	8.47	
θ _{JB}	Junction-to-board thermal resistance	—	
ψ _{JT}	Junction-to-top characterization parameter	0.36	
ψ _{JB}	Junction-to-board characterization parameter	14.6	
θ _{JC(bottom)}	Junction-to-case(bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/spra953).

DISSIPATION RATINGS

BOARD	PACKAGE	R _{θJA}	R _{θJC}	DERATING FACTOR ABOVE T _A = +25°C	T _A ≤ +25°C POWER RATING	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
High-K ⁽¹⁾	DGN	55.9°C/W	8.47°C/W	16.6mW/°C	1.83W	1.08W	0.833W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch multilayer board with 2-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

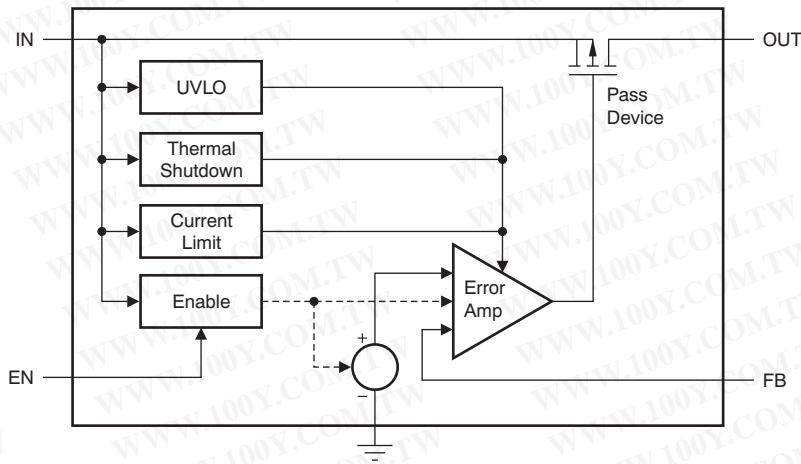
At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 2.0\text{ V}$ or $V_{IN} = 7.0\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 100\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TPS7A41			UNIT
		MIN	TYP	MAX	
V_{IN} Input voltage range		7.0		50.0	V
V_{REF} Internal reference	$T_J = +25^\circ\text{C}$, $V_{FB} = V_{REF}$, $V_{IN} = 9\text{ V}$, $I_{OUT} = 25\text{ mA}$	1.161	1.173	1.185	V
V_{OUT} Output voltage range ⁽¹⁾	$V_{IN} \geq V_{OUT(NOM)} + 2.0\text{ V}$	V_{REF}		48	V
	$T_J = +25^\circ\text{C}$, $V_{IN} = 9\text{ V}$, $I_{OUT} = 25\text{ mA}$	-1.0		+1.0	% V_{OUT}
	$V_{OUT(NOM)} + 2.0\text{ V} \leq V_{IN} \leq 24\text{ V}$ ⁽²⁾ $100\ \mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$	-2.5		+2.5	% V_{OUT}
$\Delta V_{O(\Delta VI)}$ Line regulation	$7\text{ V} \leq V_{IN} \leq 50\text{ V}$		0.03		% V_{OUT}
$\Delta V_{O(\Delta VL)}$ Load regulation	$100\ \mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$		0.31		% V_{OUT}
V_{DO} Dropout voltage	$V_{IN} = 17\text{ V}$, $V_{OUT(NOM)} = 18\text{ V}$, $I_{OUT} = 20\text{ mA}$		290		mV
	$V_{IN} = 17\text{ V}$, $V_{OUT(NOM)} = 18\text{ V}$, $I_{OUT} = 50\text{ mA}$		0.78	1.3	V
I_{LIM} Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$, $V_{IN} = 7.0\text{ V}$, $T_J \leq +85^\circ\text{C}$	51	117	200	mA
	$V_{OUT} = 90\% V_{OUT(NOM)}$, $V_{IN} = 9.0\text{ V}$	51	128	200	mA
I_{GND} Ground current	$7\text{ V} \leq V_{IN} \leq 50\text{ V}$, $I_{OUT} = 0\text{ mA}$		25	65	μA
	$I_{OUT} = 50\text{ mA}$		25		μA
I_{SHDN} Shutdown supply current	$V_{EN} = +0.4\text{ V}$		4.1	20	μA
I_{FB} Feedback current ⁽³⁾		-0.1	0.01	0.1	μA
I_{EN} Enable current	$7\text{ V} \leq V_{IN} \leq 50\text{ V}$, $V_{IN} = V_{EN}$		0.02	1.0	μA
V_{EN_HI} Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO} Enable low-level voltage		0		0.4	V
V_{NOISE} Output noise voltage	$V_{IN} = 12\text{ V}$, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT} = 10\ \mu\text{F}$, BW = 10 Hz to 100 kHz		58		μV_{RMS}
	$V_{IN} = 12\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $C_{OUT} = 10\ \mu\text{F}$, C_{BYP} ⁽⁴⁾ = 10 nF, BW = 10 Hz to 100 kHz		73		μV_{RMS}
PSRR Power-supply rejection ratio	$V_{IN} = 12\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $C_{OUT} = 10\ \mu\text{F}$, C_{BYP} ⁽⁴⁾ = 10 nF, $f = 100\text{ Hz}$		65		dB
T_{SD} Thermal shutdown temperature	Shutdown, temperature increasing		+170		$^\circ\text{C}$
	Reset, temperature decreasing		+150		$^\circ\text{C}$
T_J Operating junction temperature range		-40		+125	$^\circ\text{C}$

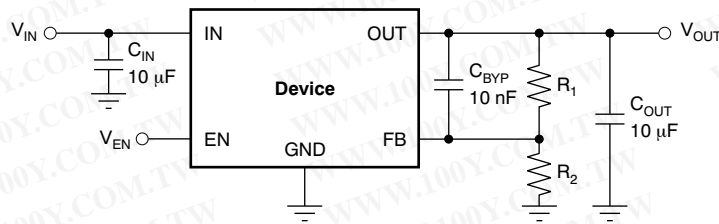
- (1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to $10\ \mu\text{A}$ is required.
- (2) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\text{ V} - V_{REF}) \times 50\text{ mA} \approx 1.14\text{ W}$). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
- (3) $I_{FB} > 0$ flows out of the device.
- (4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



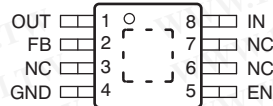
Where: $\frac{V_{OUT}}{R_1 + R_2} \geq 10 \mu A$, and

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

Example Circuit to Maximize Transient Performance

PIN CONFIGURATION

**DGN PACKAGE
MSOP-8
(TOP VIEW)**



PIN DESCRIPTIONS

TPS7A41		DESCRIPTION
NAME	NO.	
EN	5	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB	2	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
GND	4	Ground
IN	8	Input supply
NC	3, 6, 7	Not internally connected. This pin must either be left open or tied to GND.
OUT	1	Regulator output. A capacitor greater than 4.7 μF must be tied from this pin to ground to assure stability.
PowerPAD		Solder to printed circuit board (PCB) to enhance thermal performance. NOTE: The PowerPAD is internally connected to GND. Although it can be left floating, it is highly recommended to connect the PowerPAD to the GND plane.

TYPICAL CHARACTERISTICS

At $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 2.0\text{ V}$ or $V_{IN} = 9.0\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 100\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

LOAD TRANSIENT RESPONSE

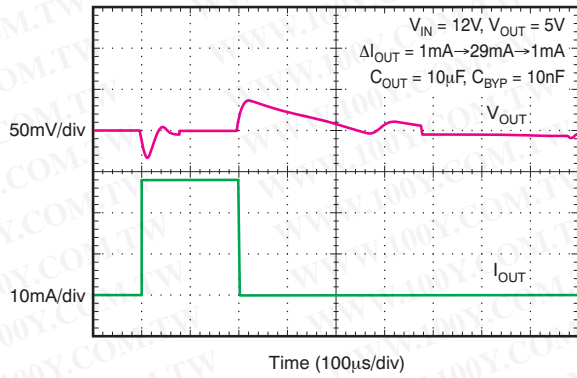


Figure 1.

LINE REGULATION

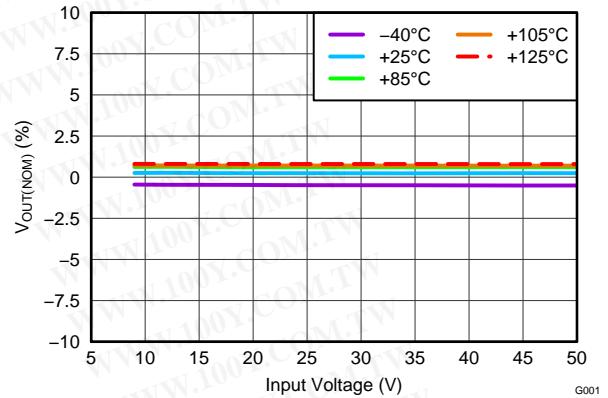


Figure 2.

FEEDBACK VOLTAGE

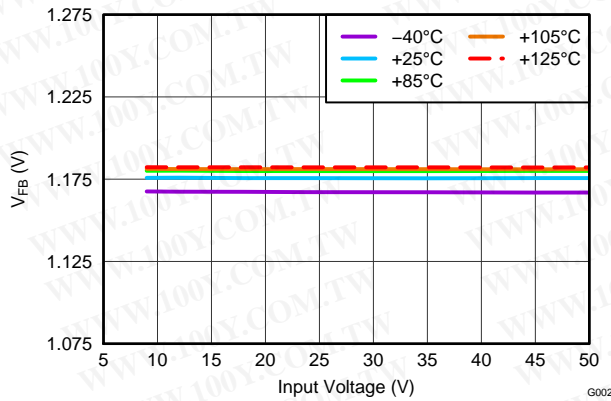


Figure 3.

QUIESCENT CURRENT vs INPUT VOLTAGE

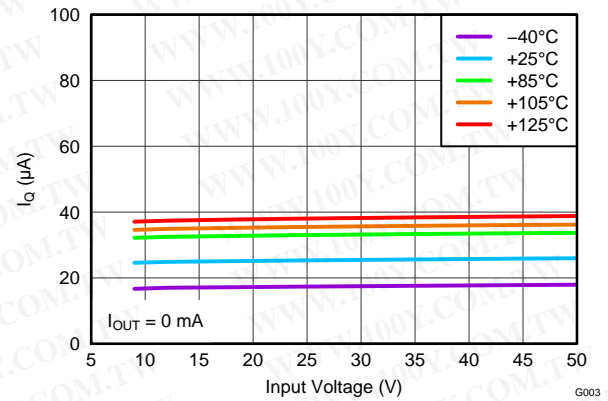


Figure 4.

FEEDBACK CURRENT

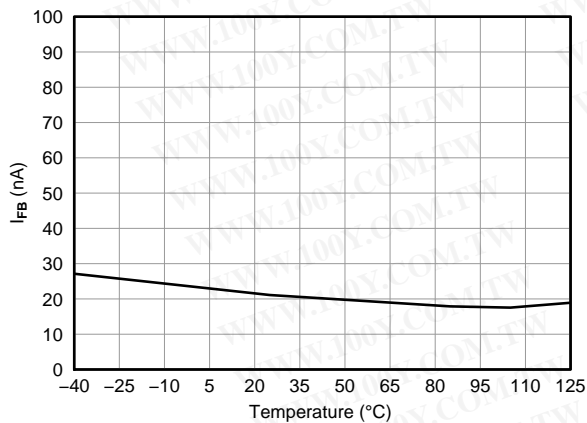


Figure 5.

GROUND CURRENT

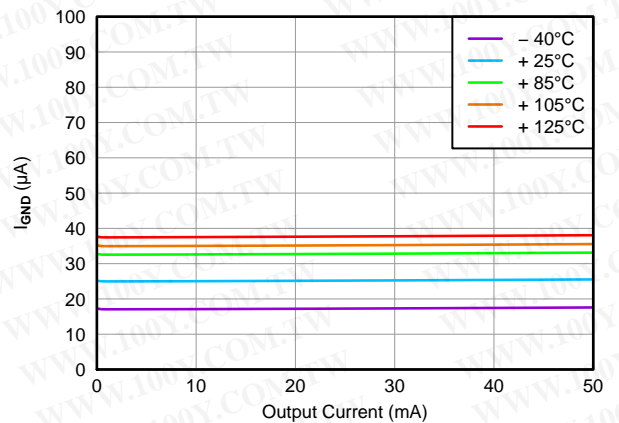


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 2.0\text{ V}$ or $V_{IN} = 9.0\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 100\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

DROPOUT VOLTAGE

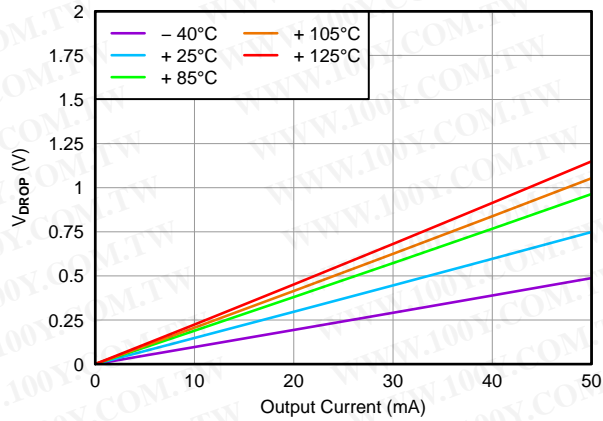


Figure 7.

ENABLE THRESHOLD VOLTAGE

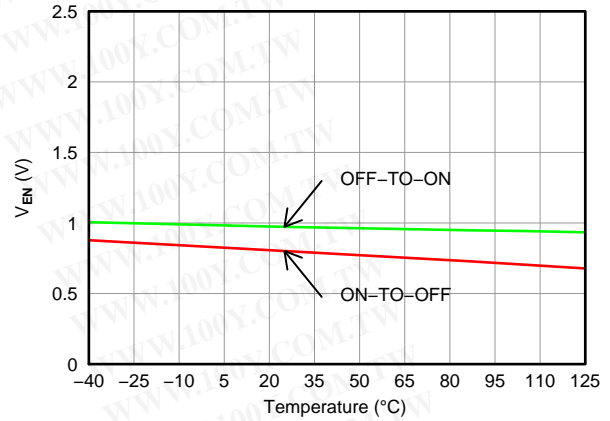


Figure 8.

OUTPUT SPECTRAL NOISE DENSITY

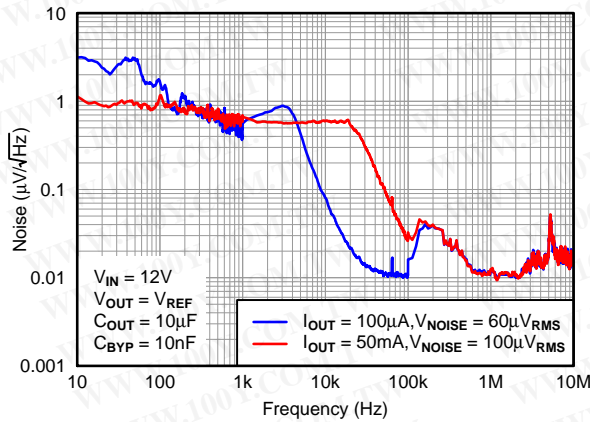


Figure 9.

CURRENT LIMIT

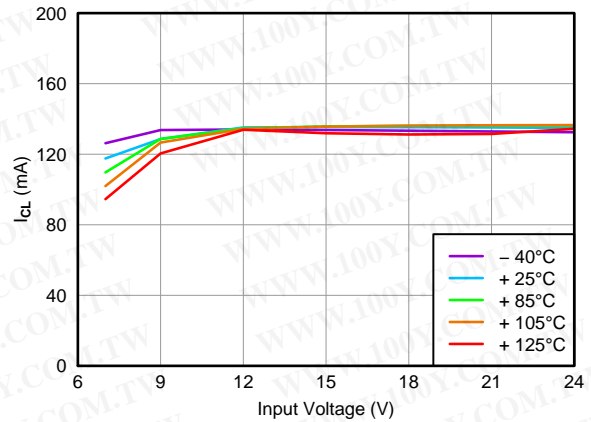


Figure 10.

POWER-SUPPLY REJECTION RATIO

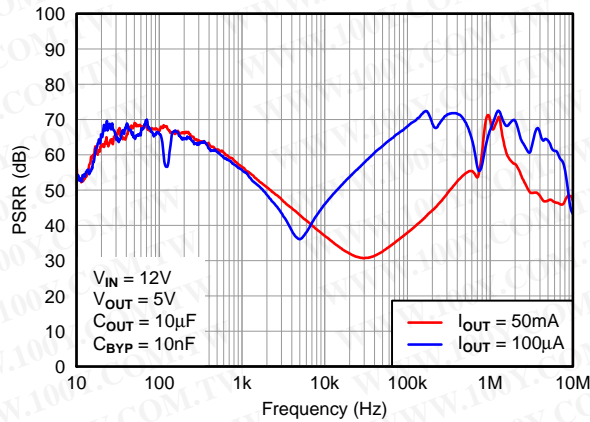


Figure 11.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A4101 belongs to a new generation of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4101 to maintain regulation during very fast high-voltage transients up to 50 V, but it also allows the TPS7A4101 to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the TPS7A4101 ground current is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance MSOP-8 PowerPAD package, make this device ideal for industrial and telecom applications.

ADJUSTABLE OPERATION

The TPS7A4101 has an output voltage range of ~1.175 V to 48 V. The nominal output voltage of the device is set by two external resistors, as shown in [Figure 12](#).

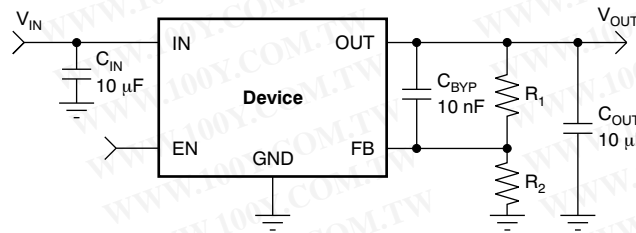


Figure 12. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in [Equation 1](#). To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 10 μ A.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 10 \mu\text{A} \quad (1)$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

ENABLE PIN OPERATION

The TPS7A4101 provides an enable pin (EN) feature that turns on the regulator when $V_{EN} > 1.5$ V.

CAPACITOR RECOMMENDATIONS

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TPS7A4101 high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 μF and input capacitance of 1 μF ; however, it is highly recommended to use 10- μF output and input capacitors to maximize ac performance.

BYPASS CAPACITOR REQUIREMENTS

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, it is highly recommended to use a 10-nF bypass capacitor to maximize ac performance (including line transient, noise and PSRR).

MAXIMUM AC PERFORMANCE

In order to maximize line transient, noise, and PSRR performance, it is recommended to include 10- μF (or higher) input and output capacitors, and a 10-nF bypass capacitor; see [Figure 12](#). The solution shown delivers minimum noise levels of 58 μV_{RMS} and power-supply rejection levels above 36 dB from 10 Hz to 10 MHz.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Note that the presence of the C_{BYP} capacitor may greatly improve the TPS7A4101 line transient response, as noted in .

APPLICATION INFORMATION

TRANSIENT VOLTAGE PROTECTION

One of the primary applications of the TPS7A4101 is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

LED ARRAY DRIVER

The TPS7A4101 can be used to drive several LED drivers connected in series, as shown in Figure 13.

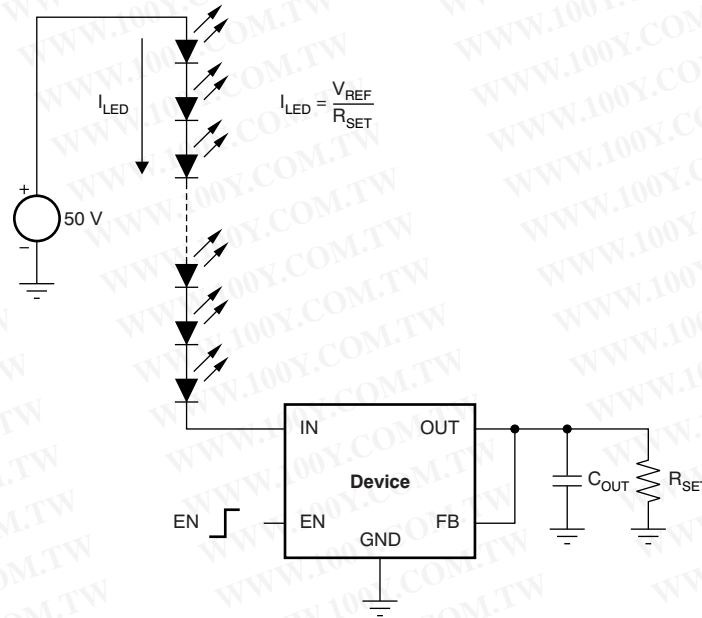


Figure 13. LED Array Driver Application

The TPS7A4101 high voltage rating makes it suitable not only for driving the intensity of an array of multiple LEDs by using a PWM signal at its EN pin, but also for controlling such an array. This PWM signal enables and disables the regulator, causing the LED light to vary its intensity.

Whenever the regulator is disabled, no current flows through the LED array. This condition means that the regulator has the same high voltage applied to the first LED in the array as is applied to the regulator input. Figure 14 illustrates the solution to this problem with the addition of the TPS7A4101 high-voltage regulator.

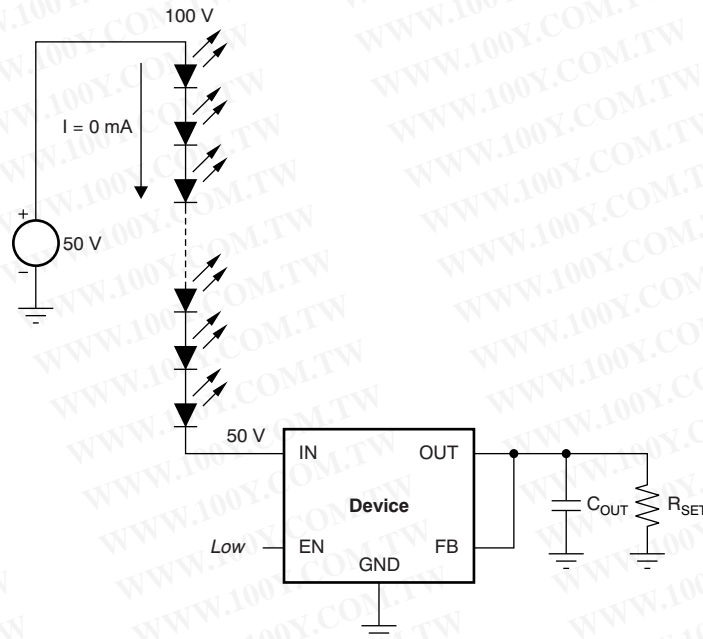


Figure 14. LED Array Driver with Regulator Disabled

LAYOUT

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A4101 are available at the end of this product data sheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A41 evaluation board, available at www.ti.com.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4101 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A4101 into thermal shutdown degrades device reliability.



POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Dissipation Ratings Table](#). Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS7A4101DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBB	
TPS7A4101DGNT	ACTIVE	MSOP- PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBB	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

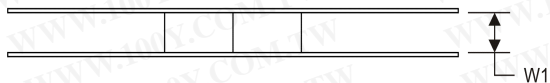
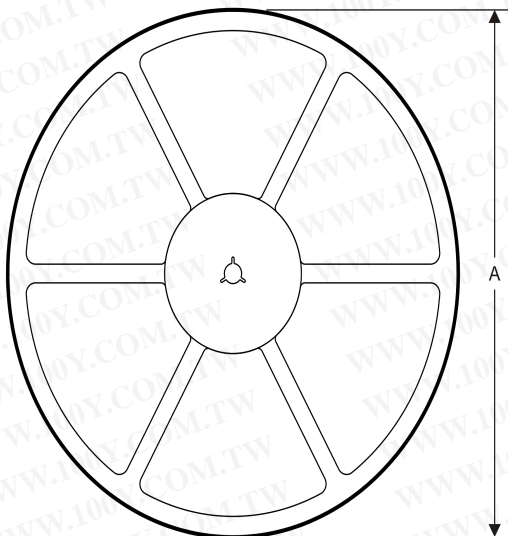
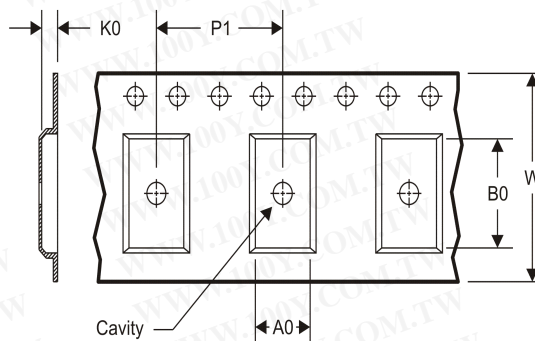
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

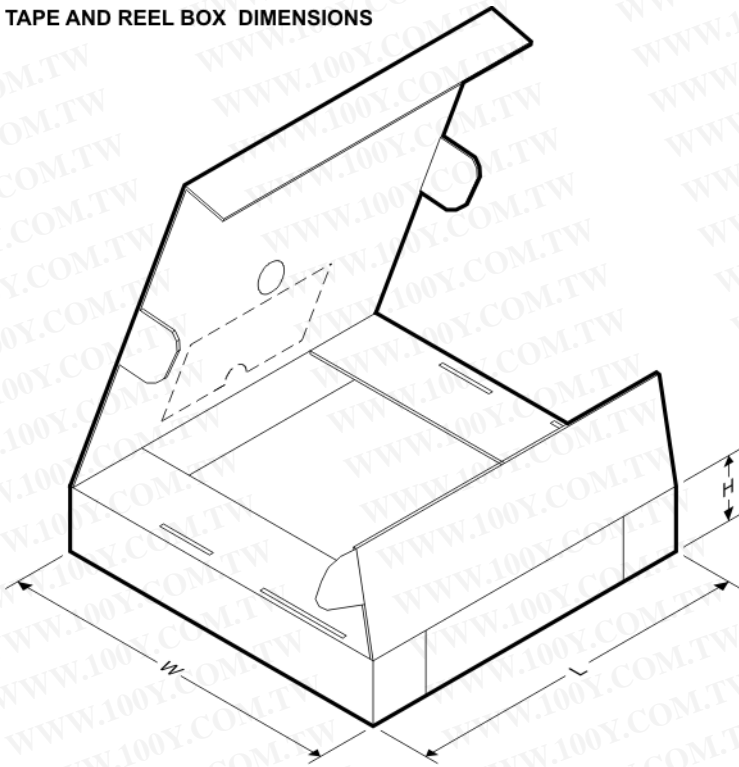
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4101DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A4101DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

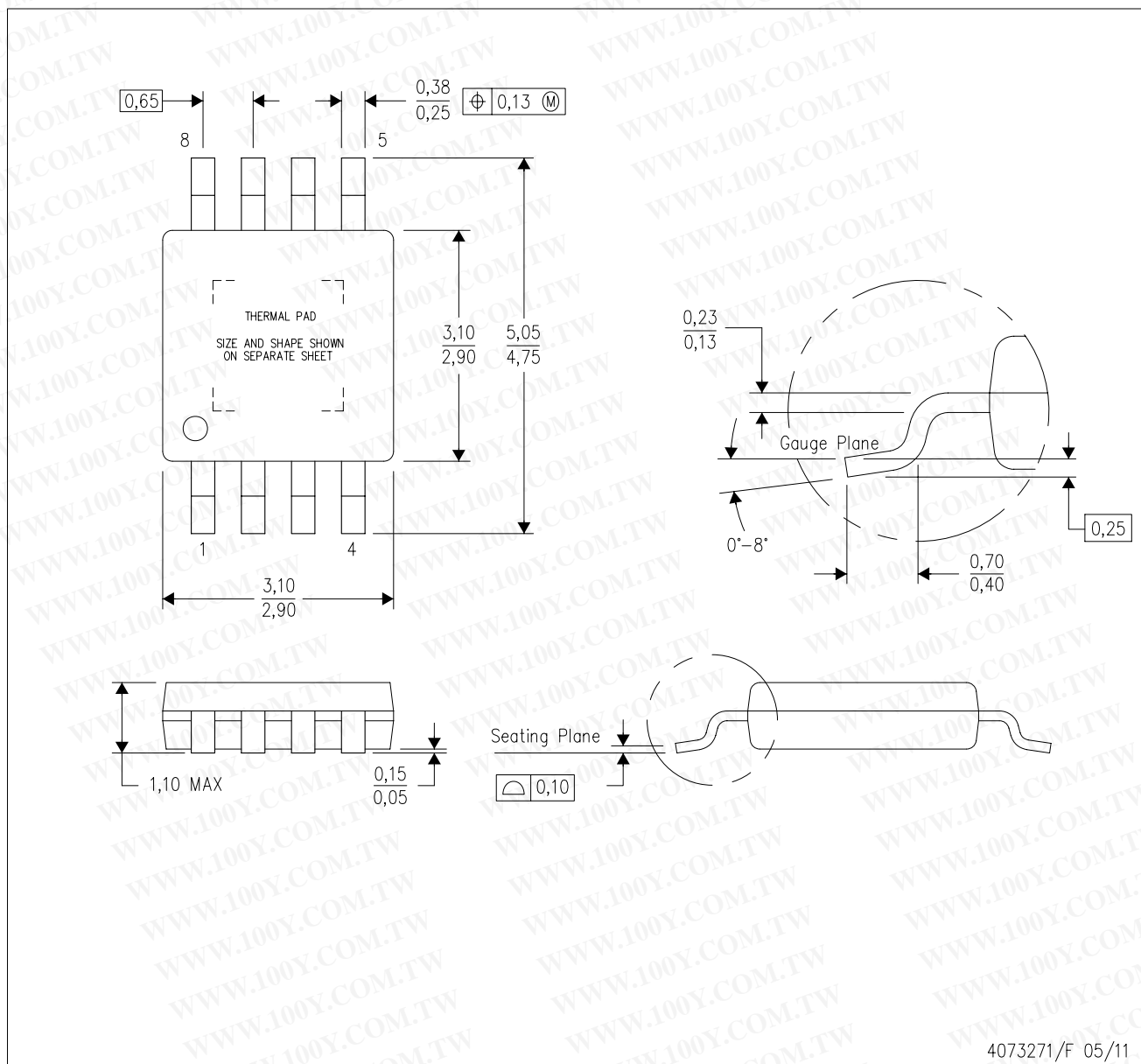
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4101DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	35.0
TPS7A4101DGNT	MSOP-PowerPAD	DGN	8	250	203.0	203.0	35.0

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DGN (S-PDSO-G8)

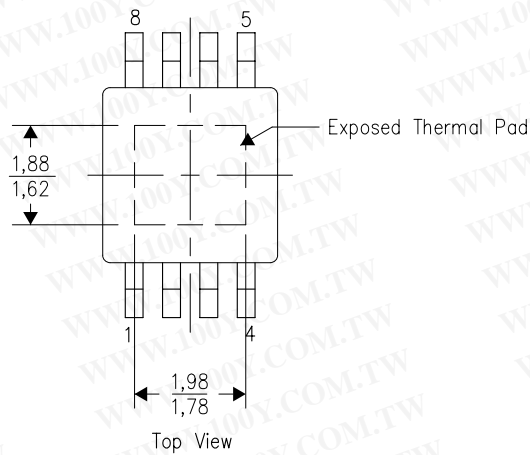
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

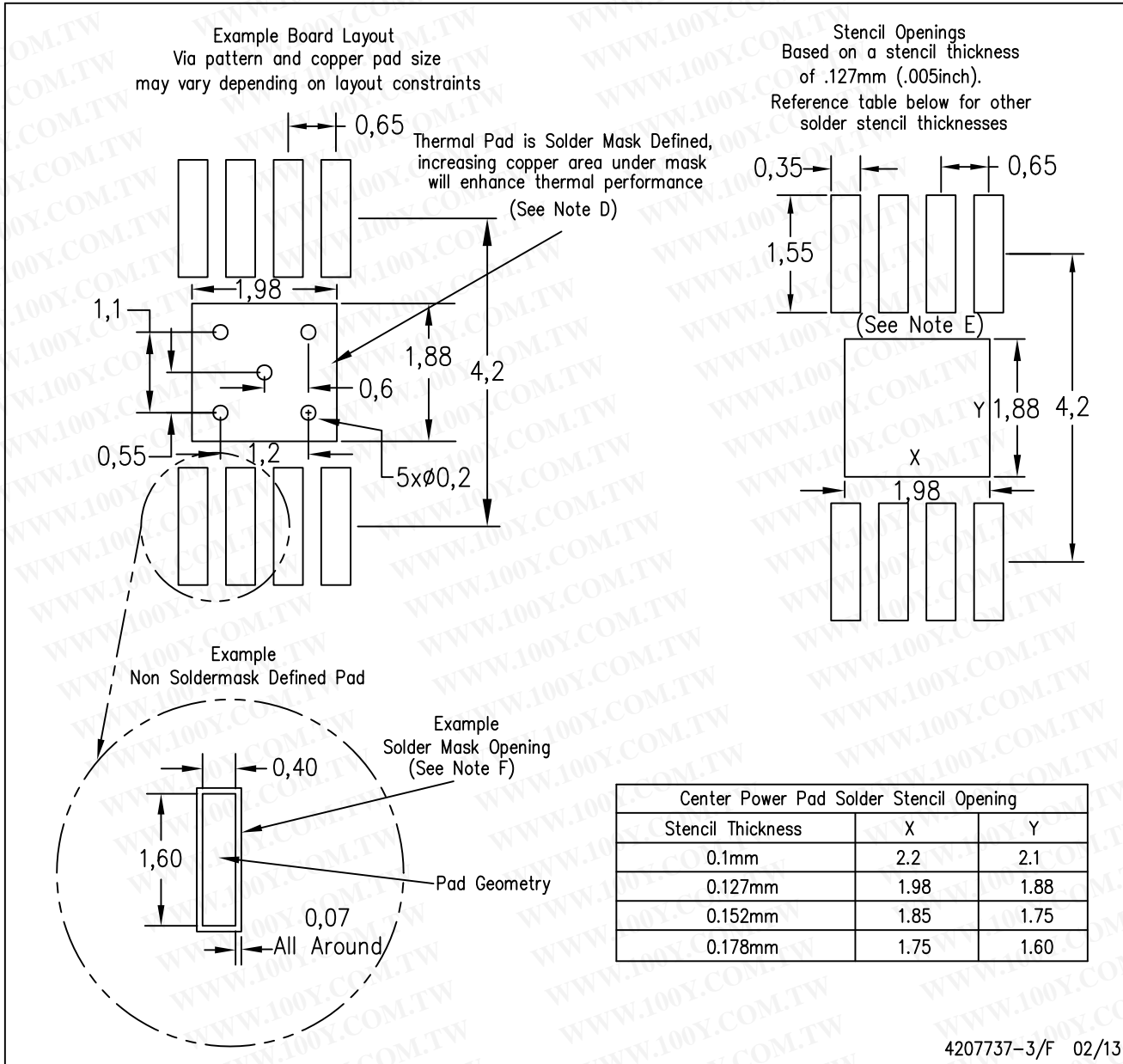
4206323-3/1 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated