



TPS7H1201HTEVM User's Guide

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1 INTRODUCTION

This user's guide describes the characteristics, operation, and use of the TPS7H1201HT evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS7H1201HT ultra-low Dropout LDO regulator. It is rated for 0.5-A ultra low-dropout (LDO) voltage regulator. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the EVM.

1.1 Related Documentation

1. TPS7H1201-HT Datasheet ([SLVSAS4](#))

2 BACKGROUND

The TPS7H1201HTEVM helps designers evaluate the operation and performance of the TPS7H1201HT ultra low drop out regulator.

Table 1. Summary of Performance

TEST CONDITIONS	OUTPUT CURRENT RANGE
$V_{IN} = 1.5\text{ V to }7\text{ V}$	Max 0.5 A

The evaluation module is designed to provide access to the features of the TPS7H1201. Some modifications can be made to this module to test performance at different input and output voltages, current and switching frequency. Please contact TI Field Applications Group for advice on these matters.

3 SAFETY

3.1 Eye Protection

Safety glasses are to be worn while performing all testing on the EVM.

3.2 General Risks

This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.

3.3 Electrostatic Discharge

ESD precautions must be followed while handling electronic assemblies.

3.4 Thermal/Shock Hazards

Precautions should be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

4 APPAREL

- Electrostatic smock
- Electrostatic gloves or finger cots
- Safety glasses
- Ground ESD wrist strap

5 EQUIPMENT

5.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 7-V at 1-A or higher is required.

5.2 Load #1

Electronic load, i.e. Chroma 63640-80-80 module along with 63600-2 DC electronic load Mainframe or Decade Resistor Box.

5.3 Meters

Four (4) Fluke 75, (equivalent or better) or two (2) equivalent voltage meters and two (2) equivalent current meters.

The current meters must be able to measure 3 A current. Note: Shunt along with DVM can be used to monitor output current.

5.4 Oscilloscope

An Tektronix Oscilloscope, i.e. DPO 7104C Current Probe Tektronix TCP202 or equivalent.

6 BOARD LAYOUT

6.1 EVM Layout Flexibility

The EVM is laid out to provide flexibility for the customer evaluation thus providing test points and or cold nose probes to monitor various critical nodes of the design as highlighted in the schematic.

Additionally, placeholder is provided thus one can add esr in series with the output capacitor (R47 in series with C39) thus making it easier to evaluate performance with increased capacitor esr.

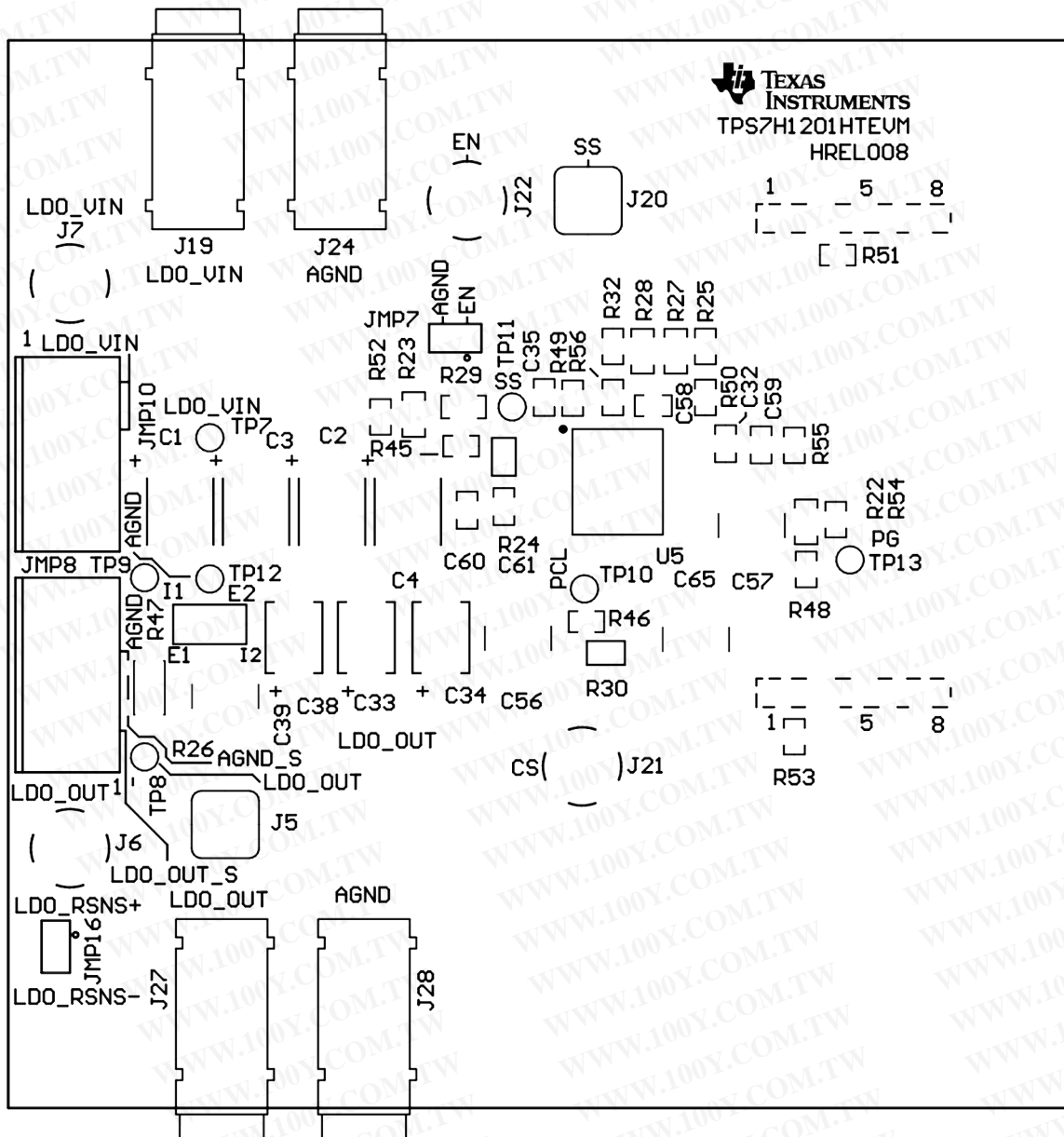


Figure 1. Component Placement (Top Side)

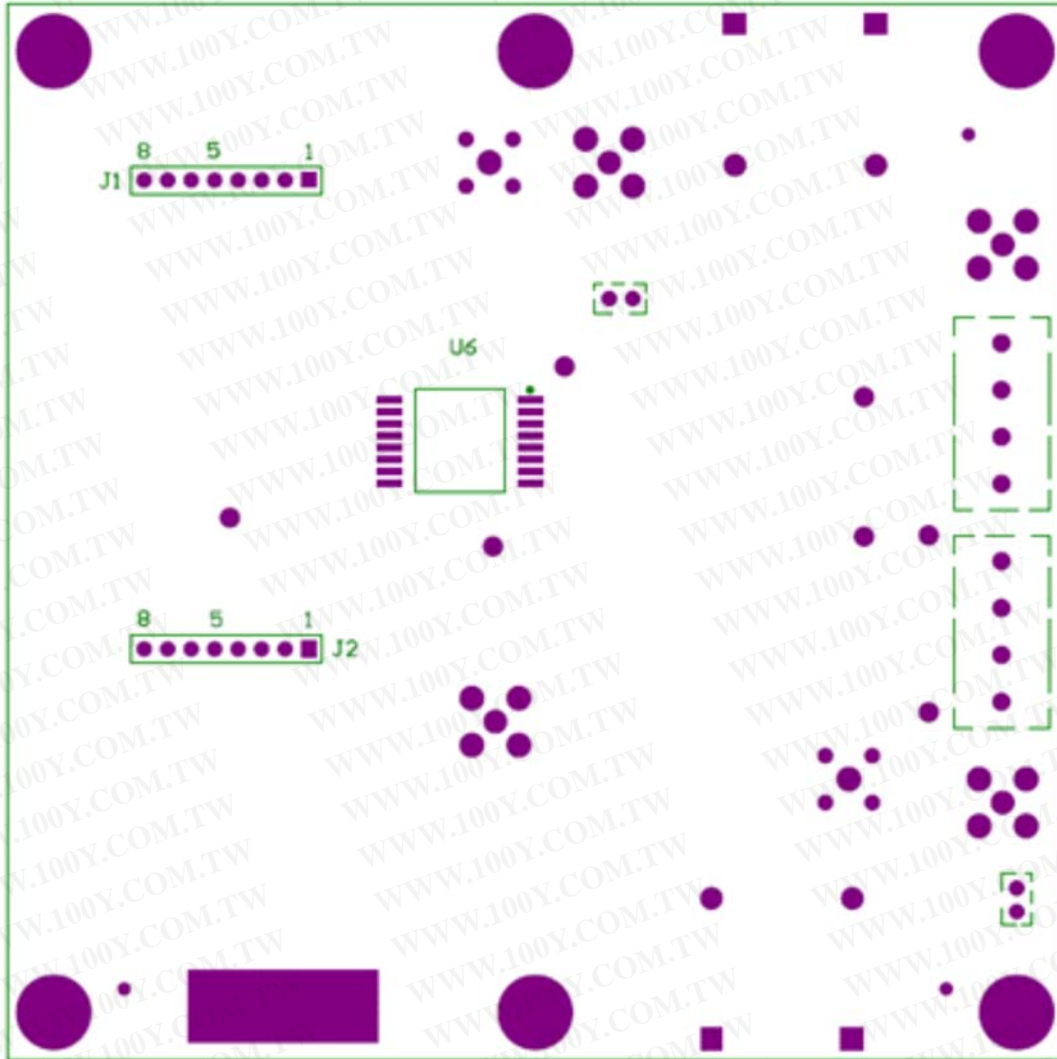


Figure 2. Component Placement (Bottom Side)

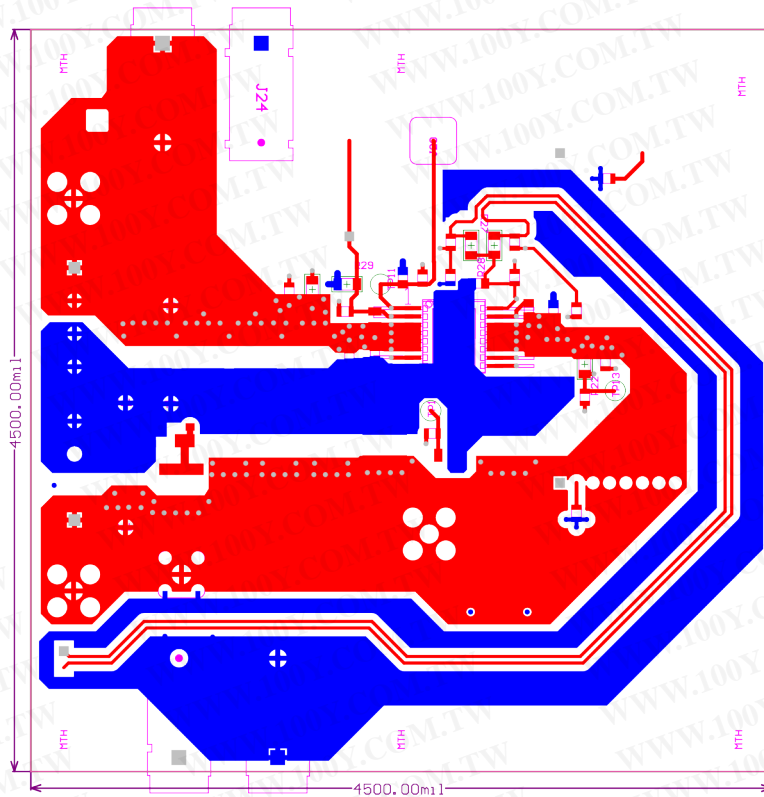


Figure 3. PCB Layout (Top Layer)

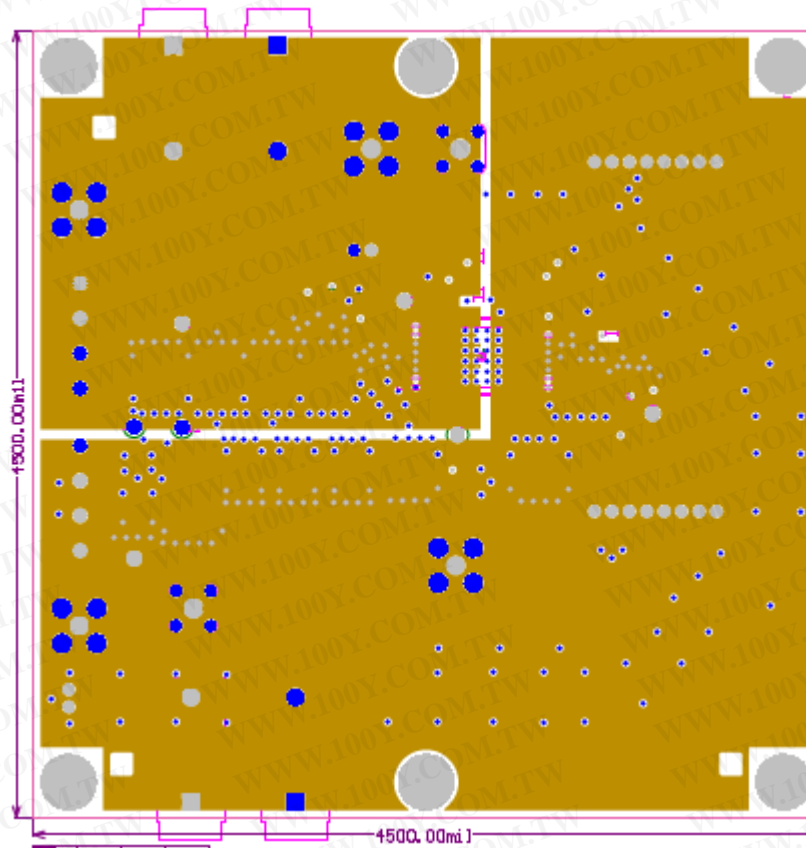


Figure 4. Board Layout - Second Layer (Mid Layer 1)

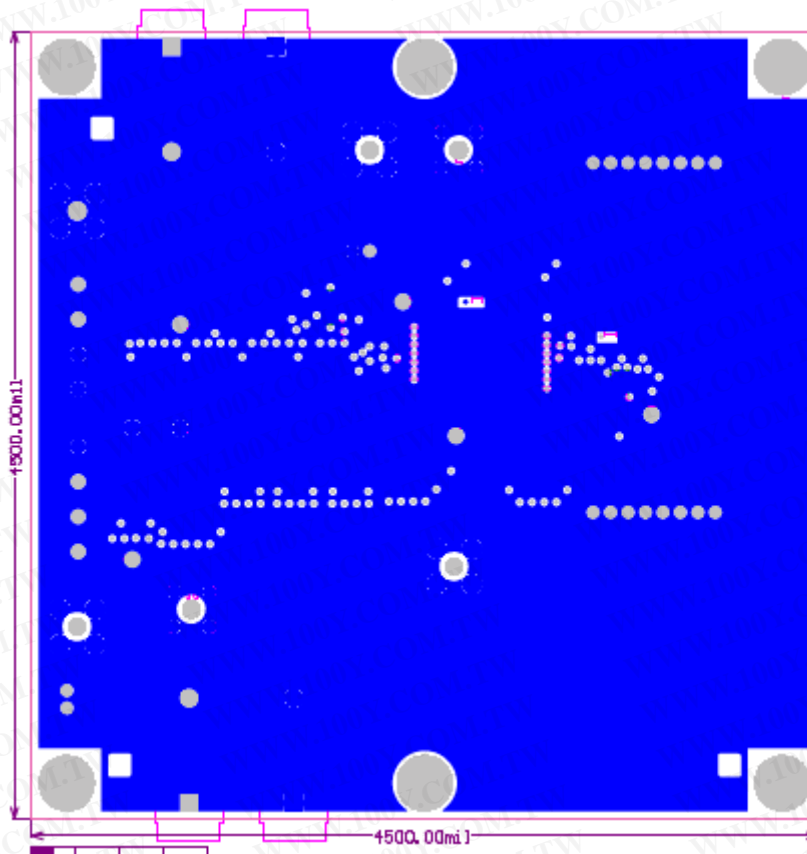


Figure 5. Board Layout - Third Layer (Mid Layer 2)

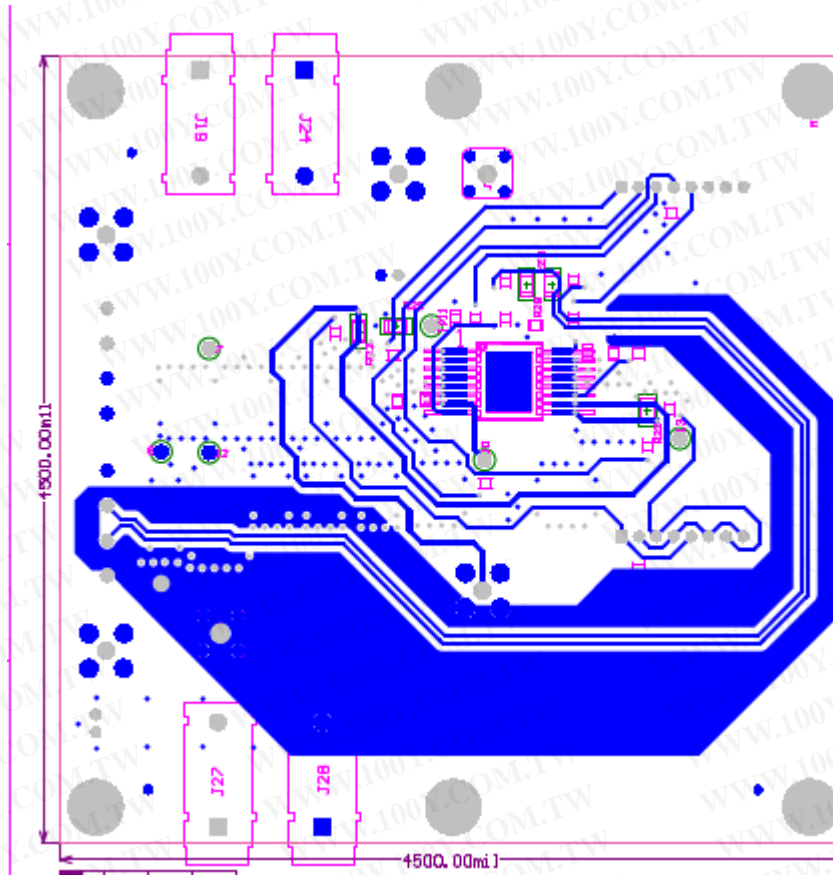


Figure 6. Board Layout - Fourth Layer (Bottom Layer)

7 BENCH TEST SETUP CONDITIONS

7.1 Headers Description and Jumper Placement

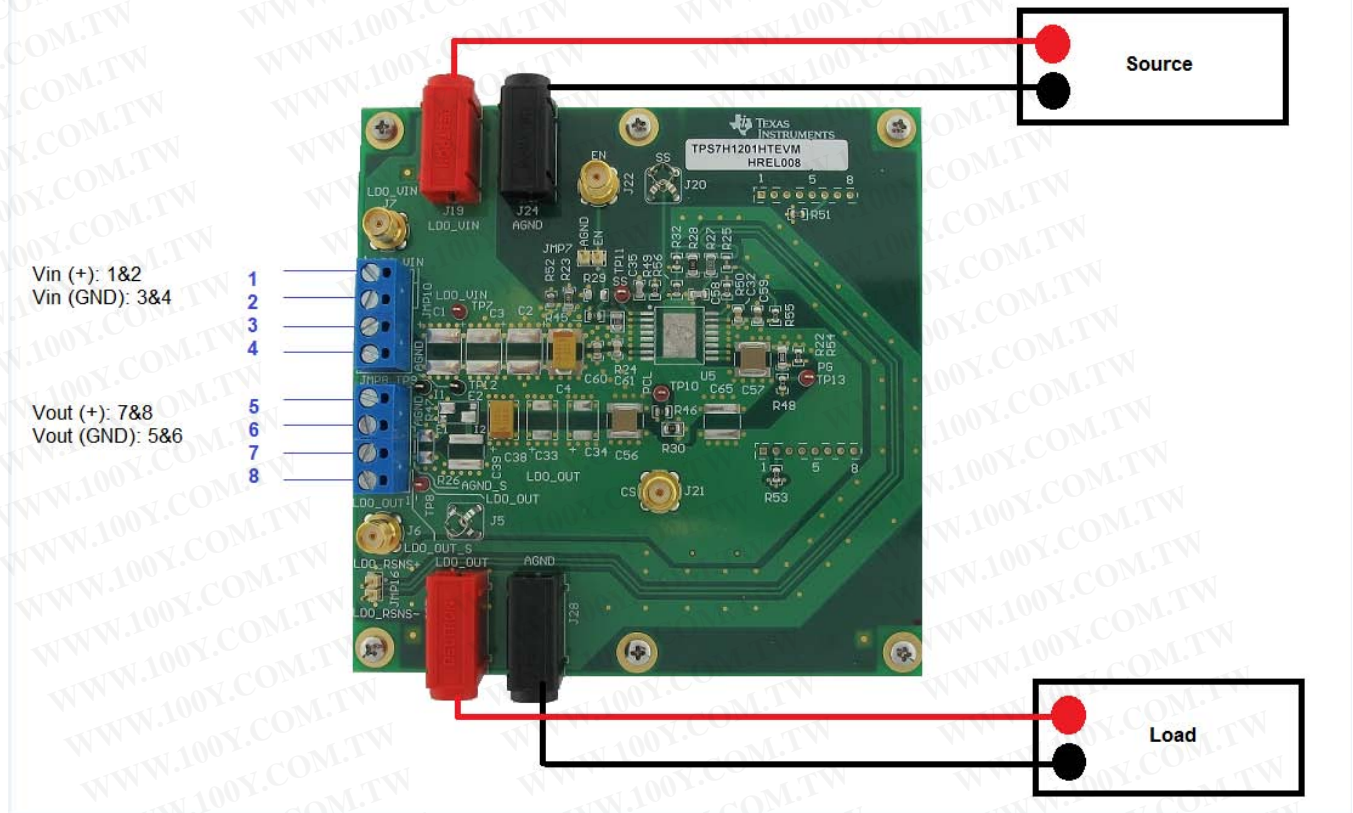


Figure 7. Headers Description and Jumper Placement

7.2 Testing

Table 2. Power Connectors

NO.	FUNCTION
J19	V _{IN} input voltage connector (see for V _{IN} range)
J24	V _{IN} input voltage connector to ground
J27	V _{OUT} output voltage connector
J28	V _{OUT} output connector to ground
J7	Vin_SMA
J22	EN_SMA
J20	SS_Probe
J5	LDO_OUT_Probe
TP8	LDO Vout measure point (+)
TP9	LDO Vout measure point (GND)
J6	LDO_OUT_SMA
TP7	LDO Vin measure point (+)
TP12	LDO Vin measure point (GND)
TP10	PCL
J21	CS_SMA
TP13	PGOOD
TP11	SS
JMP10	V _{IN} alternative connection: 1,2 (+) and 3,4 (GND)
JMP8	V _{OUT} alternative connection 3,4 (+) and 1,2 (GND)

8 POWER-UP PROCEDURE

Table 3. Test Results

	V _{OUTMIN}	V _{OUTMAX}	CURRENT LIMIT	
V _{OUT} = 1.8 V	1.76 V	1.836 V	< 0.7 A	OUTPUT SET POINT
I _{OUT} = 0.5 A	1.8166 V		0.6 A	CURRENT LIMIT

8.1 I_{OUT} and V_{OUT} Measurements

1. Make sure all power supplies in workstation are OFF.
2. Locate connectors J19 and J24.
3. Connect V_{IN}(+) to J19 and V(GND) to J24. Set it to 2.3 V.
4. Locate measure points TP7 and TP12.
5. Connect voltmeter: V_{IN}(+) to TP7 and V(GND) to TP12.
6. Locate connectors J27 and J28 and connect load here (be aware of polarities).
7. Locate measure points TP8 and TP9.
8. Connect voltmeter: V_{OUT}(+) to TP8 and V(GND) to TP9.
9. Output voltage should be per [Table 1](#). This is done by setting R27 = 19.8 kΩ and R28 = 10 kΩ.

V_{OUT} can be determined by equation highlighted below or per equation 1 in the datasheet.

$$V_{OUT} = \frac{(R_{27} + R_{28}) \cdot V_{REF}}{R_{28}} \quad (1)$$

Where V_{REF} = 0.605 V.

8.2 Output Current Limiting

A resistor value R30 connected from PCL pin to GND determines the output current limit set point based on Equation 2.

Maximum programmable current limit is 700 mA.

$$R_{pcl} = R_{30} = \frac{CSR(V_{ref})}{PCL_{cl} - 0.0216} \tag{2}$$

Where $V_{REF} = 0.605\text{ V}$, PCL_{cl} = programmable current limit (A), CSR = Current sense ratio (typical value = 51436).

CSR between I_{cs} pin and I_{OUT} can be measured as shown in Figure 8.

- Make sure all power supplies in workstation are OFF.
- Connect $V_{IN}(+)$ to J19 & $V(GND)$ to J24 and set it to 2.3 V.
- Set V_{OUT} to 1.8V. (R27 = 19.8 kΩ and R28 = 10 kΩ)
- Connect load as previously instructed, set it to zero.
- Increase I_{load} (steps of 0.100 A are suggested) until V_{load} starts to drop.
- Current limit trip point < 0.7 A.

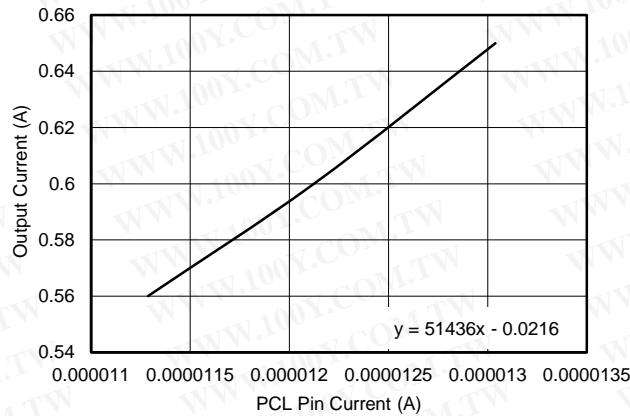


Figure 8. I_{OUT} (A) vs I_{PCL} (A)

8.3 High Side Current Sense

Monitoring the voltage at the CS pin will indicate voltage proportional to the output current. Figure 9 shows typical curve V_{CS} vs I_{OUT} for $V_{in} = 2.28\text{ V}$ and $R23 = 3.65\text{ k}\Omega$.

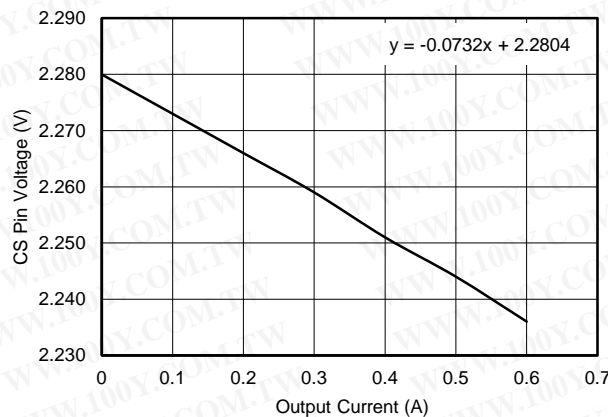


Figure 9. V_{CS} (V) vs I_{OUT} (A)

Monitoring current in CS pin (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMosFET and the current sense Mosfet as shown in Figure 10.

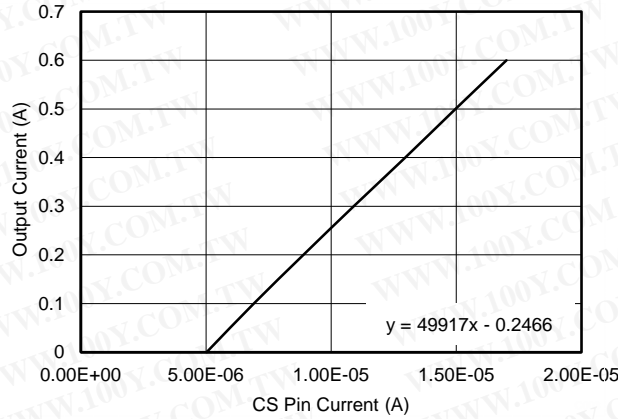


Figure 10. I_{OUT} (A) vs I_{CS} (A)

Figure 11 shows I_{OUT} vs I_{CS} when the voltage on CS pin is varied from 0.3 V to 7 V.

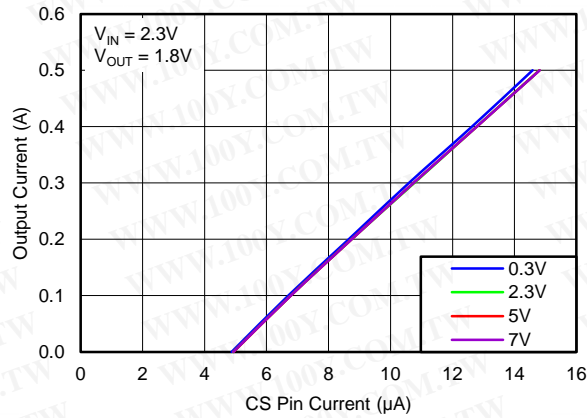


Figure 11. I_{OUT} (A) vs I_{CS} (A)

8.4 Power Good

Power good pin is an open drain connection, connect it high via pull up resistor to external voltage source. Power Good pin indicates the status of the output voltage.

8.5 Dropout Voltage

Drop out voltage (V_{do}) is the difference between the input voltage and output voltage needed to maintain regulation. V_{do} vs I_{OUT} is highlighted in Figure 12.

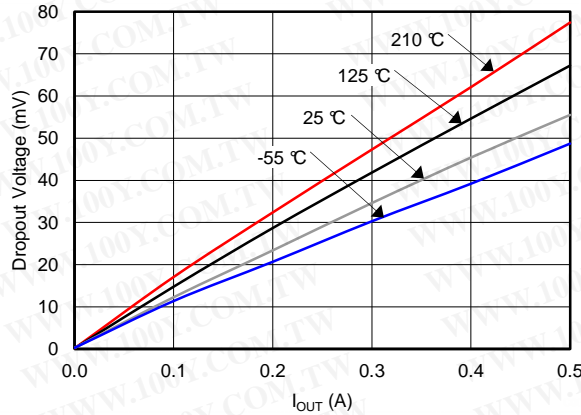


Figure 12. V_{do} vs I_{OUT}

8.6 Transient Response

Waveforms below indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Output voltage overshoot / undershoot

Channel 2 : Step load in current

Channel 3: Input voltage

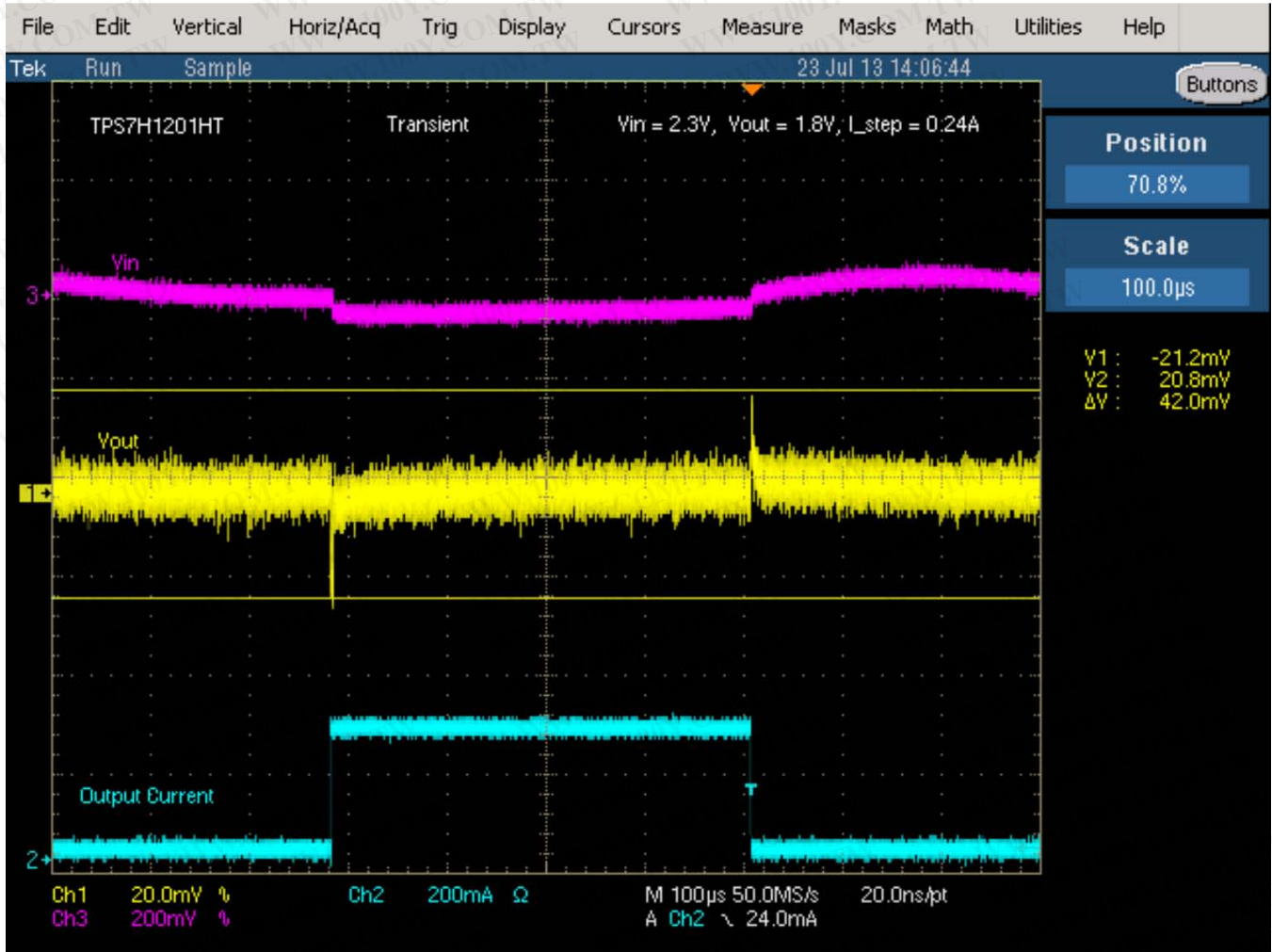


Figure 13. Load Transient Response: Step Load 0 A to 250 mA

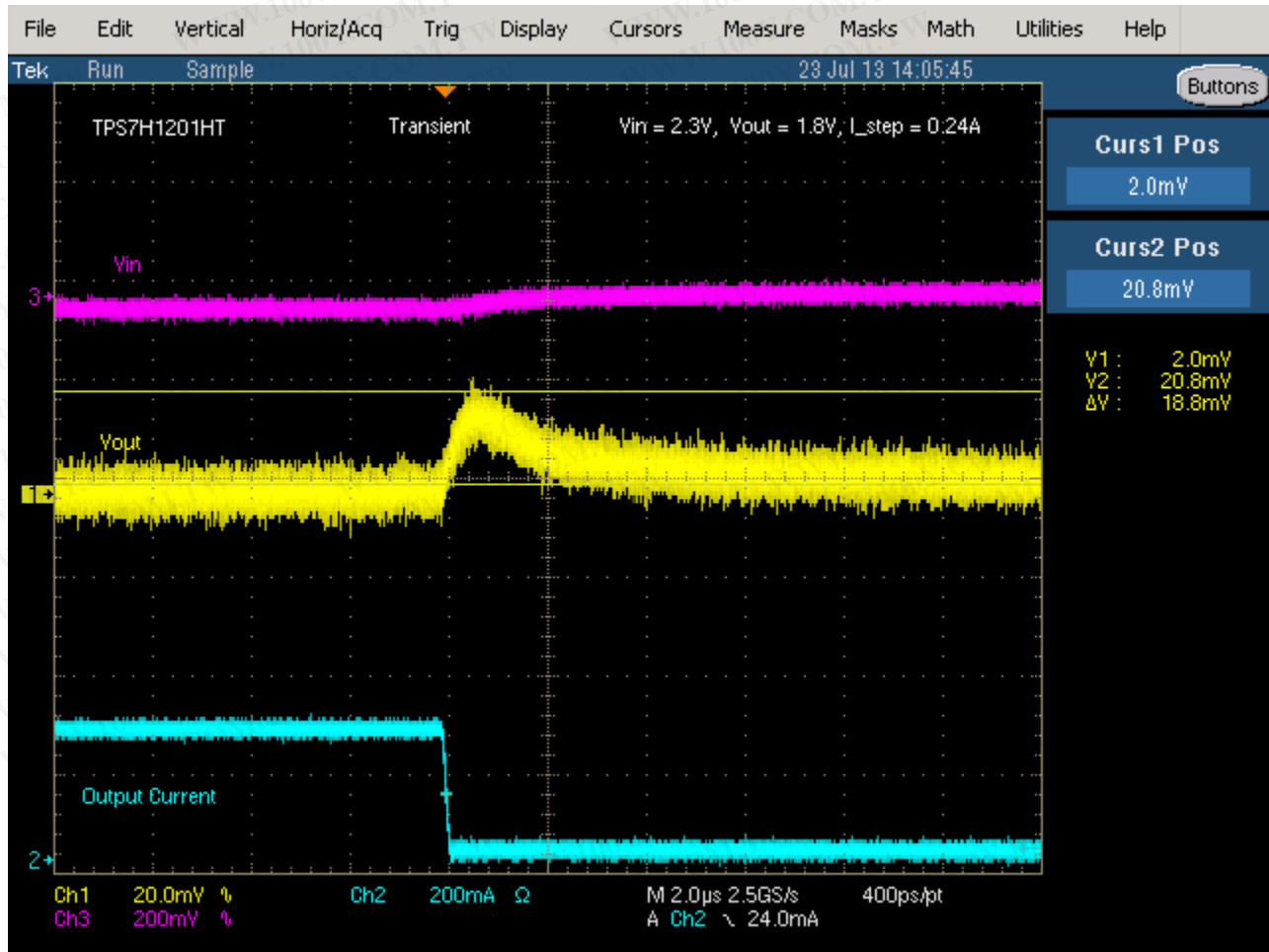


Figure 14. Expanded View Overshoot

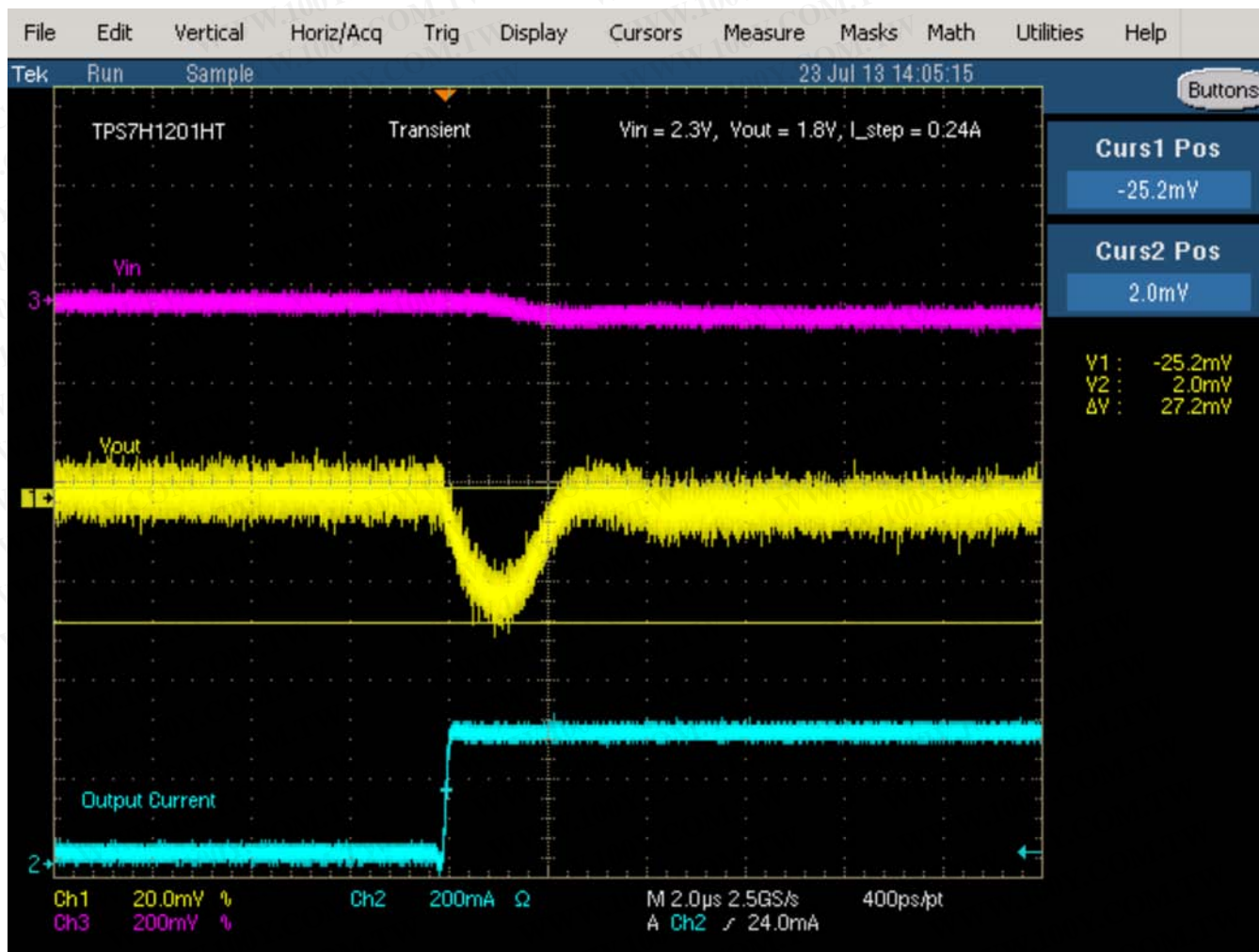


Figure 15. Expanded View Undershoot

8.7 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled.

- In parallel mode CS pin of LDO#1 must be connected to PCL pin of LDO#2 via a series resistor (41.5 kΩ) and CS pin of LDO#2 must be connected to PCL pin of LDO#1 via series resistor (41.5 kΩ).
- In parallel configuration R30 (resistor from PCL to GND) and R23 (resistor from CS pin to V_{IN}) must be left open (unpopulated).

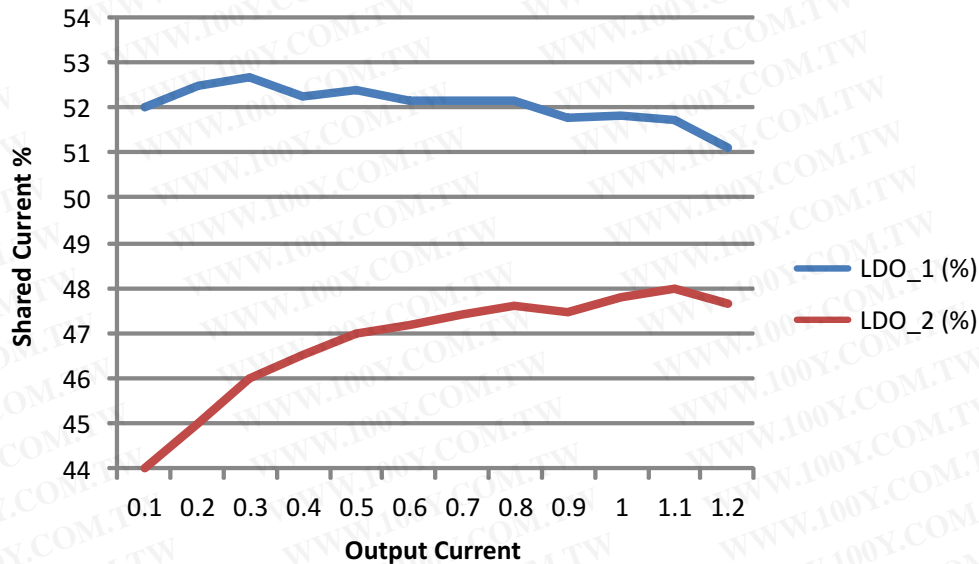


Figure 16. Current Sharing LDO_1 and LDO_2

8.8 Soft-Start

Connecting a capacitor on CS pin to GND (C₃₅) slows down the output voltage ramp rate. The soft-start capacitor will charge up to 1.2 V.

$$C_{35} = \frac{T_{ss} \cdot I_{ss}}{V_{REF}} \quad (3)$$

Where:

t_{ss} = Soft-start time

I_{ss} = 2.5 μA

V_{REF} = 0.605 V

8.9 Enable/Disable

EVM can be disabled via pulling the enable pin low via shorting JMP7-1 (Enable) to JMP7-2 (GND). Enable pin is tied high to V_{IN} via R24 (20 kΩ) resistor, thus keeping the EVM enabled.

Alternately, EVM can also be disabled via pulling SS pin (U6 pin 1) low via an external circuit comprising of 2N7002 MOSFET as shown in Figure 17. A high signal at the gate of Q100 will discharge the SS pin and disable the device.

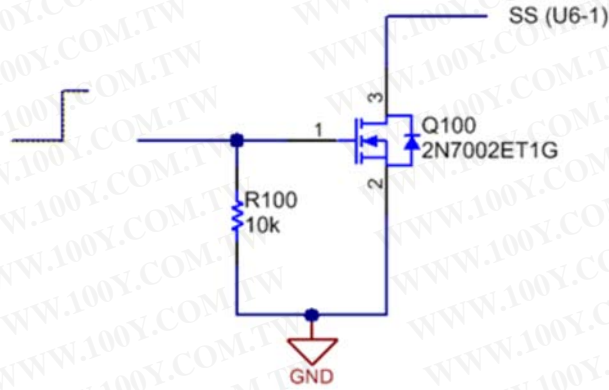


Figure 17. Disabling the LDO via Soft-Start Pin

8.10 Turn-Off

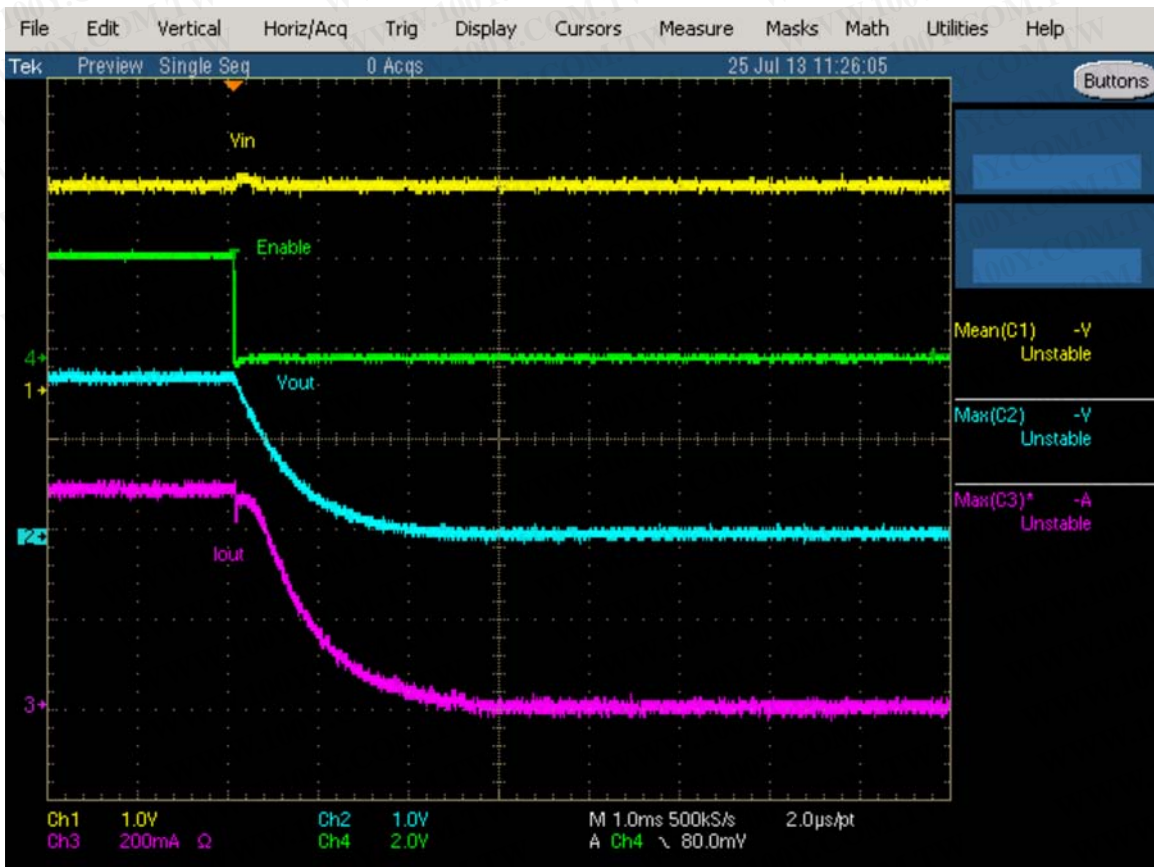


Figure 18. Turn-Off

8.11 Output Noise

Output noise is measured using HP3495A. For details on the setup see “Output Noise Measurement Setup” document. Plots below shows noise in $\mu\text{V}/\sqrt{\text{Hz}}$ vs Frequency.

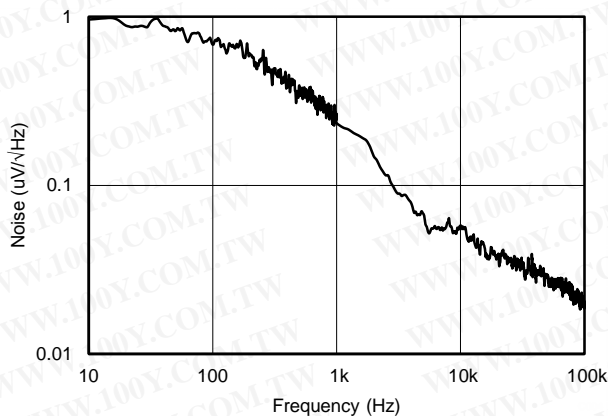


Figure 19. RMS Noise (10 Hz - 100 kHz) = 19.4113538 μVrms , $V_{\text{IN}} = 2 \text{ V}$, $V_{\text{OUT}} = 1.8 \text{ V}$ at 0 A.

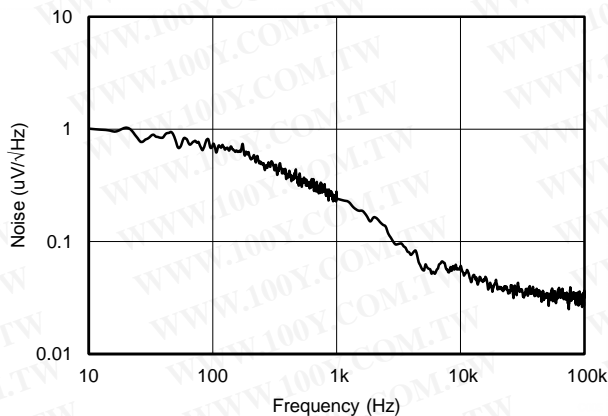


Figure 20. RMS Noise (10 Hz - 100 kHz) = 20.12 μVrms , $V_{\text{IN}} = 2 \text{ V}$, $V_{\text{OUT}} = 1.8 \text{ V}$ at 0.25 A.

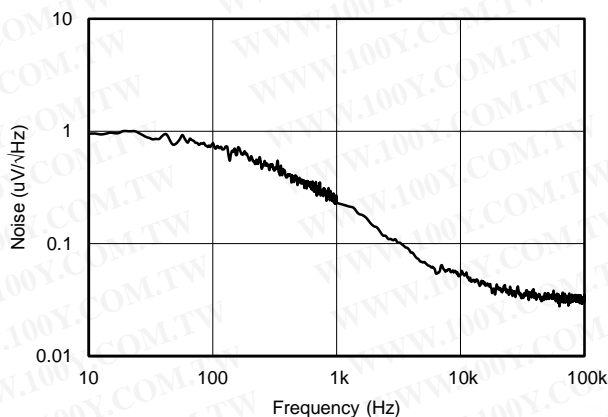


Figure 21. RMS Noise (10 Hz - 100 kHz) = 20.26 μVrms , $V_{\text{IN}} = 2 \text{ V}$, $V_{\text{OUT}} = 1.8 \text{ V}$ at 0.5 A.

9 SCHEMATIC AND BILL OF MATERIALS

The following pages contain the TPS7H1201HTEVM schematic and bill of materials.

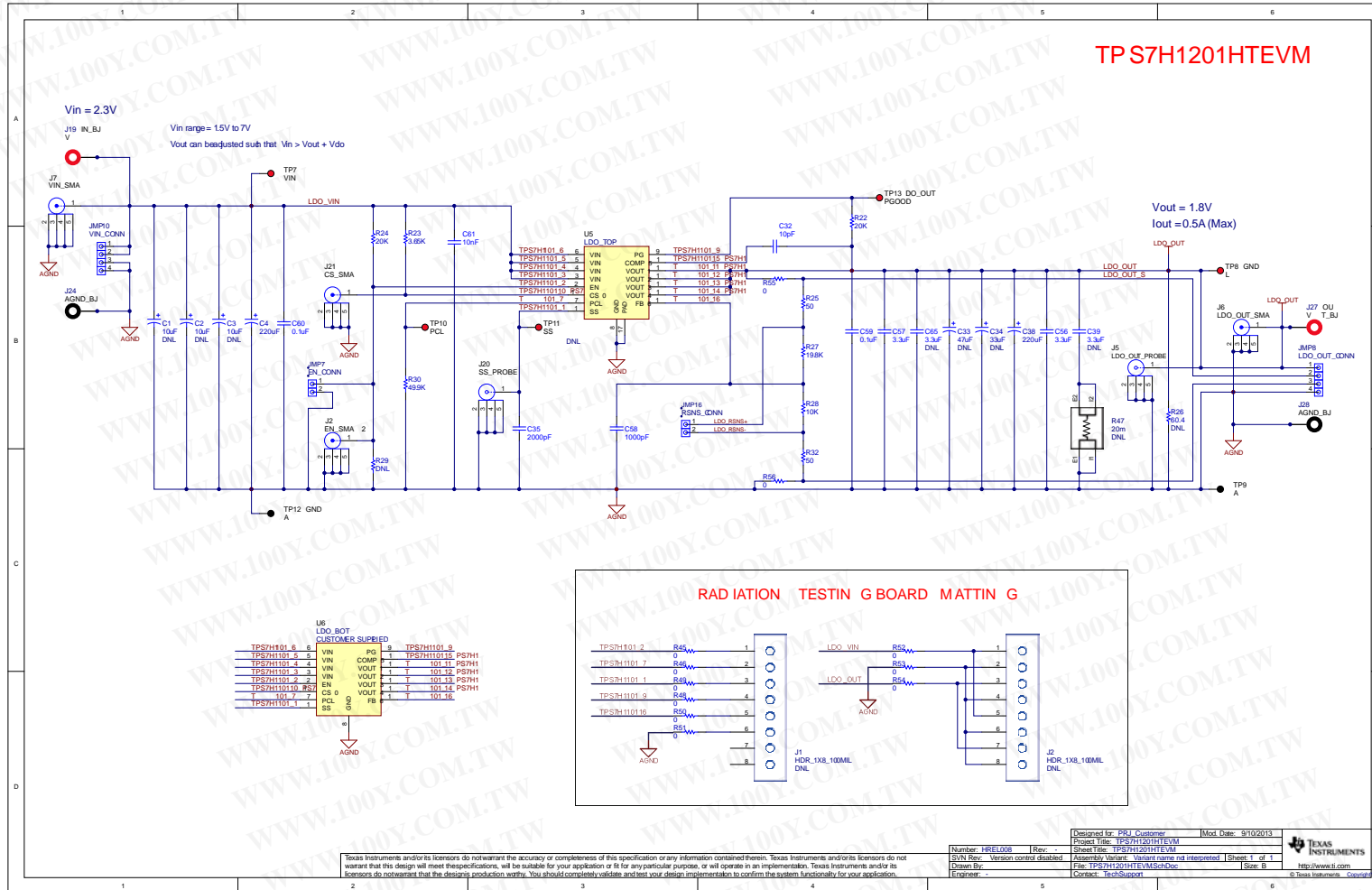


Figure 22. TPS7H1201HTEVM Schematic

Table 4. TPS7H1201HTEVM Bill of Materials

Item No.	Qty	Designator	Value	Footprint	Manufacturer	Part No.	Description
1	1	C4	220uF	7260-38	Kemet	T543X227M016ATE035	CAP TANT 220UF 16V 20% 2917
2	2	C32,C61	10nF	0805	Kemet	C0805C103K3RACTU	CAP CER 10000PF 25V 10% X7R 0805
3	1	C35	2000pF	0805	Kemet	C0805C202J3GACTU	CAP CER 2000PF 25V 5% NPO 0805
4	1	C38	220uF	7260-38	Kemet	T543X227M016ATE035	CAP TANT 220UF 16V 20% 2917
5	2	C56,C57	3.3uF	2225	MURATA	GRM55DR71H335KA01L	CAP CER 3.3UF 50V 10% X7R 2220
6	1	C58	1000pF	0805	Kemet	C0805C102J3GACTU	CAP CER 1000PF 25V 5% NPO 0805
7	2	C59,C60	0.1uF	0805	Kemet	C0805C104K3RACTU	CAP CER 0.1UF 25V 10% X7R 0805
8	1	J5			Tektronix	131-5031-00	Compact Probe Tip Circuit Board Test Points, TH
9	1	J6			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
10	1	J7			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
11	1	J19			DEM Manufacturing	571-0500	Standard Banana Jack, insulated, 10A, red
12	1	J27			DEM Manufacturing	571-0500	Standard Banana Jack, insulated, 10A, red
13	1	J20			Tektronix	131-5031-00	Compact Probe Tip Circuit Board Test Points, TH
14	1	J21			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
15	1	J22			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
16	2	J24,J28			DEM Manufacturing	571-0100	Standard Banana Jack, insulated, 10A, black
17	1	JMP7		HDR_1X2_TSW	Samtec	TSW-102-07-G-S	CONN HEADER 2POS .100 SGL GOLD"
18	1	JMP8		HDR_1X4_39544	Molex	39544-3004	CONN TERMINAL BLOCK 4POS 5.08MM
19	1	JMP10		HDR_1X4_39544	Molex	39544-3004	CONN TERMINAL BLOCK 4POS 5.08MM
20	1	JMP16		HDR_1X2_TSW	Samtec	TSW-102-07-G-S	CONN HEADER 2POS .100 SGL GOLD"
21	1	R22	20kΩ	1206	Stackpole	RNCP1206FTD20K0	RES 20K OHM 1/2W 1% 1206 SMD
22	1	R23	3.65kΩ	1206	Panasonic	ERJ-8ENF3651V	RES 3.65k, 1/4W, 1%, 100ppm/C 1206
23	1	R24	20kΩ	0805	Stackpole	RNCP0805FTD20K0	RES 20K OHM 1/4W 1% 0805 SMD
24	2	R25,R32	50Ω	0603	Panasonic	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
25	1	R27	19.8kΩ	1206	Stackpole	RNCF1206BTE19K8	RES 19.8K OHM 1/8W 0.1% 1206
26	1	R28	10kΩ	1206	Stackpole	RNCS1206BKE10K0	RES 1/8W 10K OHM 0.1% 1206
27	1	R30	49.9kΩ	0805	Stackpole	RMCF0805FT49K9	RES 49.9K OHM 1/8W 1% 0805 SMD
28	11	R45,R46,R48, R49,R50,R51, R52,R53,R54, R55,R56	0Ω	0603	Panasonic	ERJ-3GEY0R00V	RES 0.0 OHM 1/10W 0603 SMD
29	1	TP7			Keystone	5000	Test Point, TH, Miniature, Red
30	1	TP8			Keystone	5000	Test Point, TH, Miniature, Red
31	2	TP9,TP12			Keystone	5001	Test Point, TH, Miniature, Black
32	1	TP10			Keystone	5000	Test Point, TH, Miniature, Red
33	1	TP11			Keystone	5000	Test Point, TH, Miniature, Red
34	1	TP13			Keystone	5000	Test Point, TH, Miniature, Red

Table 4. TPS7H1201HTEVM Bill of Materials (continued)

Item No.	Qty	Designator	Value	Footprint	Manufacturer	Part No.	Description
35	1	U6		CFP (HKS)	Texas Instruments	TPS7H1201SHKS	IC installed as lid down at the back of the board
36	4				Keystone	2029K-ND	Standoffs
37	4				Pencom	4-40X1/4PH-PN-MS-SS	Screws for standoffs
38	1		HREL008		Any	HREL008	PCB
39	1				Brady	THT-13-457-10	Label on the EVM under TI logo = TPS7H1201HTEVM HREL008-001
40	0	C1,C2,C3	10uF	7260-38_1	Vishay	T95R106K050LSAL	CAP TANT 10UF 50V 10% 2824
41	0	C33	47uF	7260-38	Kemet	T491X476M035AT	CAP TANT 47UF 35V 20% 2917
42	0	C34	33uF	7260-38	Kemet	T491X336K035AT	CAP TANT 33UF 35V 10% 2917
43	0	C39,C65	3.3uF	2225	MURATA	GRM55DR71H335KA01L	CAP CER 3.3UF 50V 10% X7R 2220
44	0	J1,J2	HDR_1X8_1 00MIL	HDR_1X8_BCS	SAMTEC	BCS-108-F-S-TE	SKT 8 POS 2.54mm Solder ST Thru-Hole
45	0	R29	DNL	1206	TBD	TBD	TBD
46	0	R26	60.4Ω	2010	Rohm	MCR50JZHF60R4	RES 60.4 OHM 1/2W 1% 2010 SMD
47	0	R47	20mΩ	RES_Y14870R020 00B0R	VISHAY	Y14870R02000B0R	Current sensing chip resistor, 20m OHM, 0.1%
48	0	U5		CFP (HKR)	Texas Instruments	TPS7H1201SHKR	IC installed as lid up at the top of the board

勝特力材料 886-3-5753170
胜特力电子(上海) 86-21-34970699
胜特力电子(深圳) 86-755-83298787
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