# ADVANCED REGULATING PULSE WIDTH MODULATORS

## FEATURES

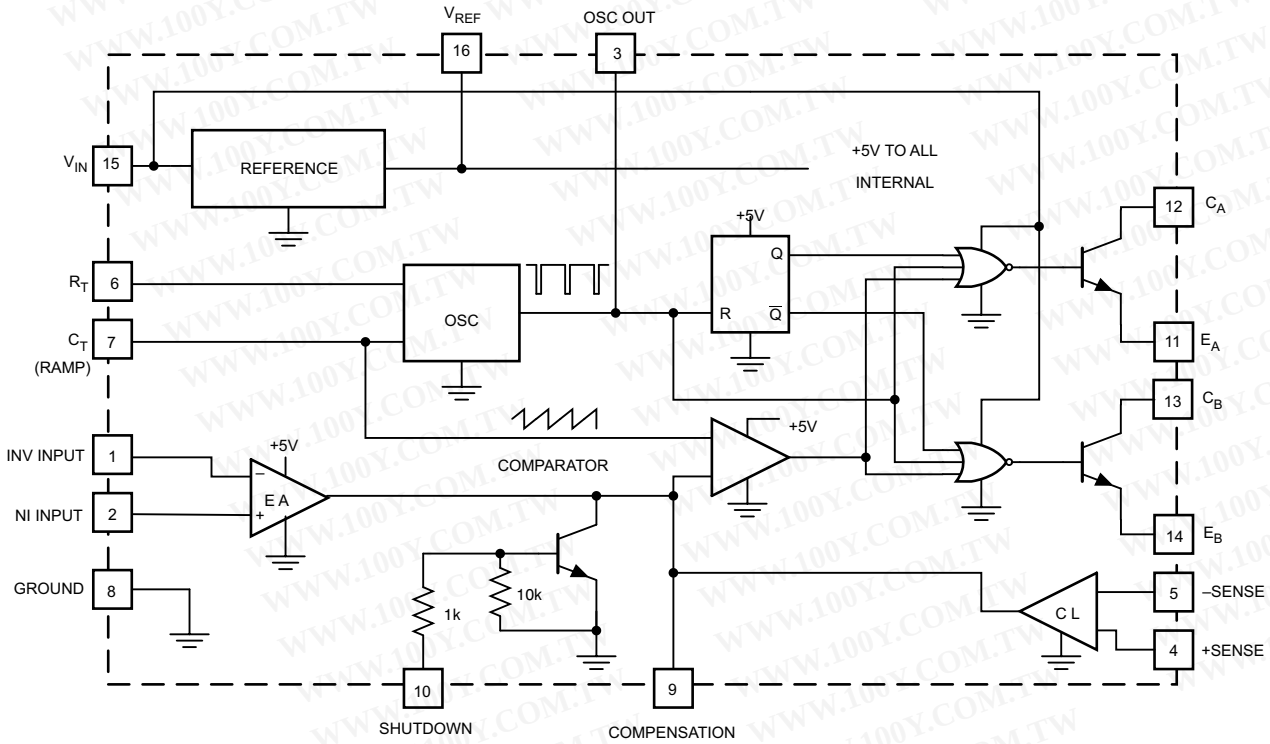
- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typical**
- **Interchangeable With SG1524, SG2524 and SG3524, Respectively**



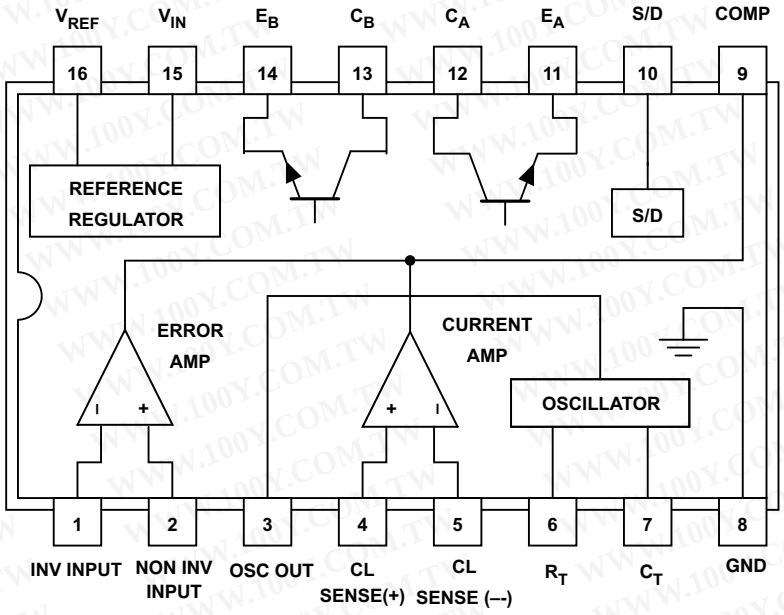
## DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of –55°C to 125°C. The UC2524 and UC3524 are designed for operation from –25°C to 85°C and 0°C to 70°C, respectively.

## BLOCK DIAGRAM



## CONNECTION DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage(1)(2) | | 40 V |
| | Collector output current | | 100 mA |
| | Reference output current | | 50 mA |
| | Current through $C_T$ terminalg | | –50 mA |
| | Power dissipation | $T_A$ = 25°C(3) | 1000 mW |
| | | $T_C$ = 25°C(3) | 2000 mW |
| | Operating junction temperature range | | –55°C to 150°C |
| | Storage temperature range | | –65°C to +150°C |

(1) All voltage values are with respect to the ground terminal, pin 8.
(2) The reference regulator may be bypassed for operation from a fixed 5 V supply by connecting the $V_{CC}$ and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6 V.
(3) Consult packaging section of data book for thermal limitations and considerations of package.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 8 | | 40 | V |
| | Reference output current | | 0 | | 20 | mA |
| | Current through $C_T$ terminal | | –0.03 | | –2 | mA |
| $R_T$ | Timing resistor | | 1.8 | | 100 | kΩ |
| $C_T$ | Timing capacitor | | 0.001 | | 0.1 | µF |
| | Operating ambient temperature range | UC1524 | –55 | | 125 | °C |
| | | UC2524 | –25 | | 85 | |
| | | UC3524 | 0 | | 70 | |

## ELECTRICAL CHARACTERISTICS

these specifications apply for $T_A$ = –55°C to 125°C for the UC1524, –25°C to 85°C for the UC2524, and 0°C to 70°C for the UC3524, $V_{IN}$ = 20 V, and f = 20 kHz, $T_A = T_J$, over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | UC1524/UC2524 | | | UC3524 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **REFERENCE SECTION** | | | | | | | | |
| Output voltage | | 4.8 | 5.0 | 5.2 | 4.6 | 5.0 | 5.4 | V |
| Line regulation | $V_{IN}$ = 8 V to 40 V | | 10 | 20 | | 10 | 30 | mV |
| Load regulation | $I_L$ = 0 mA to 20 mA | | 20 | 50 | | 20 | 50 | mV |
| Ripple rejection | f = 120 Hz, $T_J$ = 25°C | | 66 | | | 66 | | dB |
| Short circuit current limit | $V_{REF}$ = 0, $T_J$ = 25°C | | 100 | | | 100 | | mA |
| Temperature stability | Over operating temperature range | | 0.3% | 1% | | 0.3% | 1% | |
| Long term stability | $T_J$ = 125°C, t = 1000 Hrs | | 20 | | | 20 | | mV |
| **OSCILLATOR SECTION** | | | | | | | | |
| Maximum frequency | $C_T$ = 1 nF, $R_T$ = 2 kΩ | | 300 | | | 300 | | kHz |
| Initial accuracy | $R_T$ and $C_T$ constant | | 5% | | | 5% | | |
| Voltage stability | $V_{IN}$ = 8 V to 40 V, $T_J$ = 25°C | | | 1% | | | 1% | |
| Temperature stability | Over operating temperature range | | | 5% | | | 5% | |
| Output amplitude | Pin 3, $T_J$ = 25°C | | 3.5 | | | 3.5 | | V |
| Output pulse width | $C_T$ = 0.01 mfd, $T_J$ = 25°C | | 0.5 | | | 0.5 | | µs |
| **ERROR AMPLIFIER SECTION** | | | | | | | | |
| Input offset voltage | $V_{CM}$ = 2.5 V | | 0.5 | 5 | | 2 | 10 | mV |
| Input bias current | $V_{CM}$ = 2.5 V | | 2 | 10 | | 2 | 10 | µA |
| Open loop voltage gain | | 72 | 80 | | 60 | 80 | | dB |
| Common mode voltage | $T_J$ = 25°C | 1.8 | | 3.4 | 1.8 | | 3.4 | V |
| Common mode rejection ratio | $T_J$ = 25°C | | 70 | | | 70 | | dB |
| Small signal bandwidth | $A_V$ = 0 dB, $T_J$ = 25°C | | 3 | | | 3 | | MHz |
| Output voltage | $T_J$ = 25°C | 0.5 | | 3.8 | 0.5 | | 3.8 | V |
| **COMPARATOR SECTION** | | | | | | | | |
| Duty-cycle | % Each output on | 0% | | 45% | 0% | | 45% | |
| Input threshold | Zero duty-cycle | | 1 | | | 1 | | V |
| | Maximum duty-cycle | | 3.5 | | | 3.5 | | |
| Input bias current | | | 1 | | | 1 | | µA |
| **CURRENT LIMITING SECTION** | | | | | | | | |
| Sense voltage | Pin 9 = 2 V with error amplifier set for maximum out, $T_J$ = 25°C | 190 | 200 | 210 | 180 | 200 | 220 | mV |
| Sense voltage T.C. | | | 0.2 | | | 0.2 | | mV/°C |
| Common mode voltage | $T_J$ = –55°C to 85°C for the –1 V to 1 V limit | –1 | | 1 | –1 | | 1 | V |
| | $T_J$ = 25°C | –0.3 | | 1 | | | | |
| **OUTPUT SECTION (EACH OUTPUT)** | | | | | | | | |
| Collector-emitter voltage | | 40 | | | 40 | | | V |
| Collector leakage current | $V_{CE}$ = 40 V | | 0.1 | 50 | | 0.1 | 50 | µ A |
| Saturation voltage | $I_C$ = 50 mA | | 1 | 2 | | 1 | 2 | V |
| Emitter output voltage | $V_{IN}$ = 20 V | 17 | 18 | | 17 | 18 | | V |
| Rise Time | $R_C$ = 2 kΩ, $T_J$ = 25°C | | 0.2 | | | 0.2 | | µs |
| Fall Time | $R_C$ = 2 kΩ, $T_J$ = 25°C | | 0.1 | | | 0.1 | | µs |
| Total standby current (Note) | $V_{IN}$ = 40 V | | 8 | 10 | | 8 | 10 | mA |

## PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor ($R_T$), and one timing capacitor ($C_T$), $R_T$ establishes a constant charging current for $C_T$. This results in a linear voltage ramp at $C_T$, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5 V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at $C_T$. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor ($Q_1$ or $Q_2$) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the valve of $C_T$. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

## TYPICAL CHARACTERISTICS

**OPEN-LOOP VOLTRAGE AMPLIFICATION OF ERROR AMPLIFIER vs FREQUENCY**

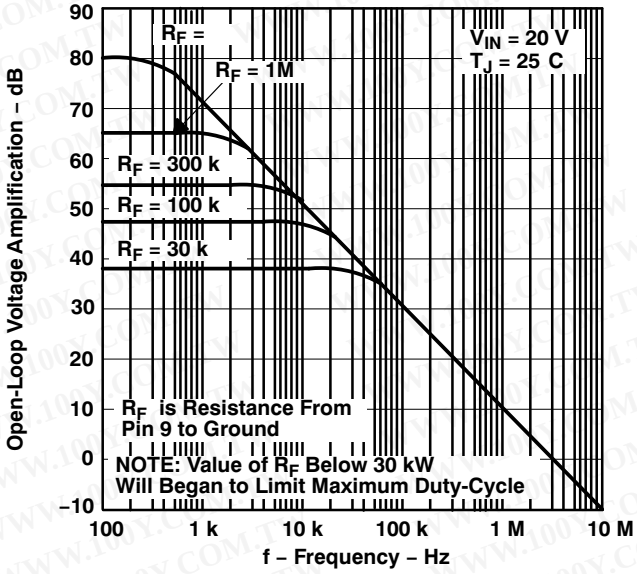



Figure 1.

**OSCILLATOR FREQUENCY vs TIMING COMPONENTS**

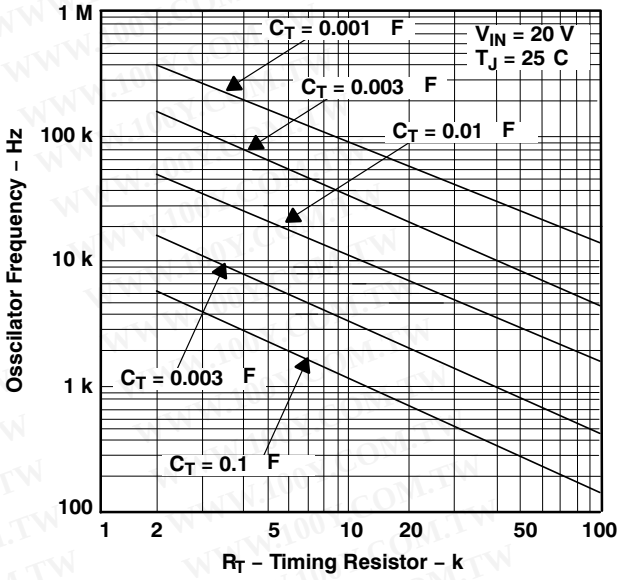



Figure 2.

**OUTPUT DEAD TIME vs TIMING CAPACITANCE VALUE**

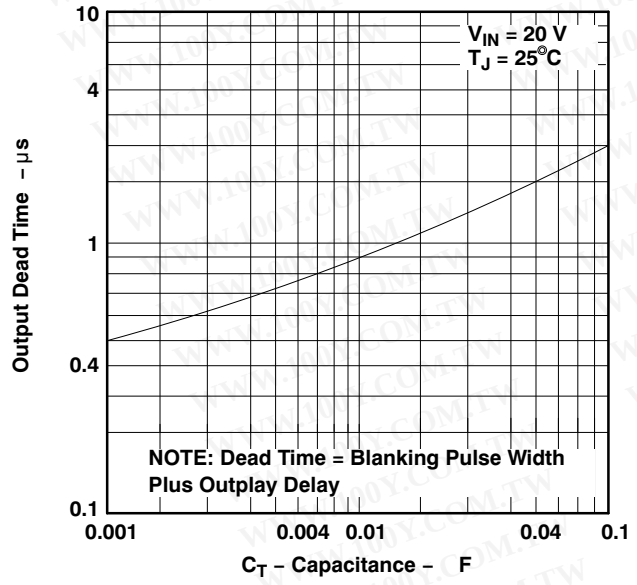



Figure 3.

**OUTPUT SATURATION VOLTAGE vs LOAD CURRENT**

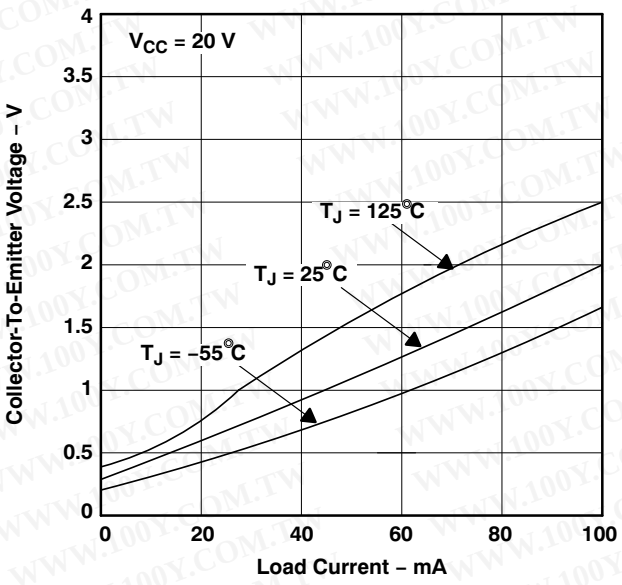



Figure 4.

## APPLICATION INFORMATION

### OSCILLATOR

The oscillator controls the frequency of the UC1524 and is programmed by $R_T$ and $C_T$ according to the approximate formula:

$$f \quad \frac{1.18}{R_T C_T} \qquad (1)$$

where

$R_T$ is in kΩ
$C_T$ is in µF
f is in kHz

Practical values of $C_T$ fall between 1 nF and 100 nF. Practical values of $R_T$ fall between 1.8 kΩ and 100 kΩ. This results in a frequency range typically from 120 Hz to 500 kHz.

### BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of $C_T$. If small values of $C_T$ are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in Figure 5.

### SYNCHRONOUS OPERATIONS

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration $R_T$ $C_T$ must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all $C_T$ terminals connected to single timing capacitor, and the timing resistor connected to a single $R_T$, terminal.

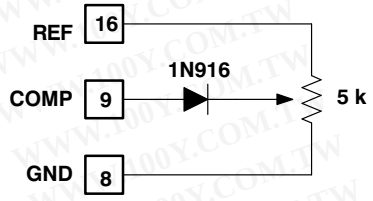



**Figure 5. Error Amplifier Clamp**

The other $R_T$ terminals can be left open or shorted to $V_{REF}$. Minimum lead lengths should be used between the $C_T$ terminals.

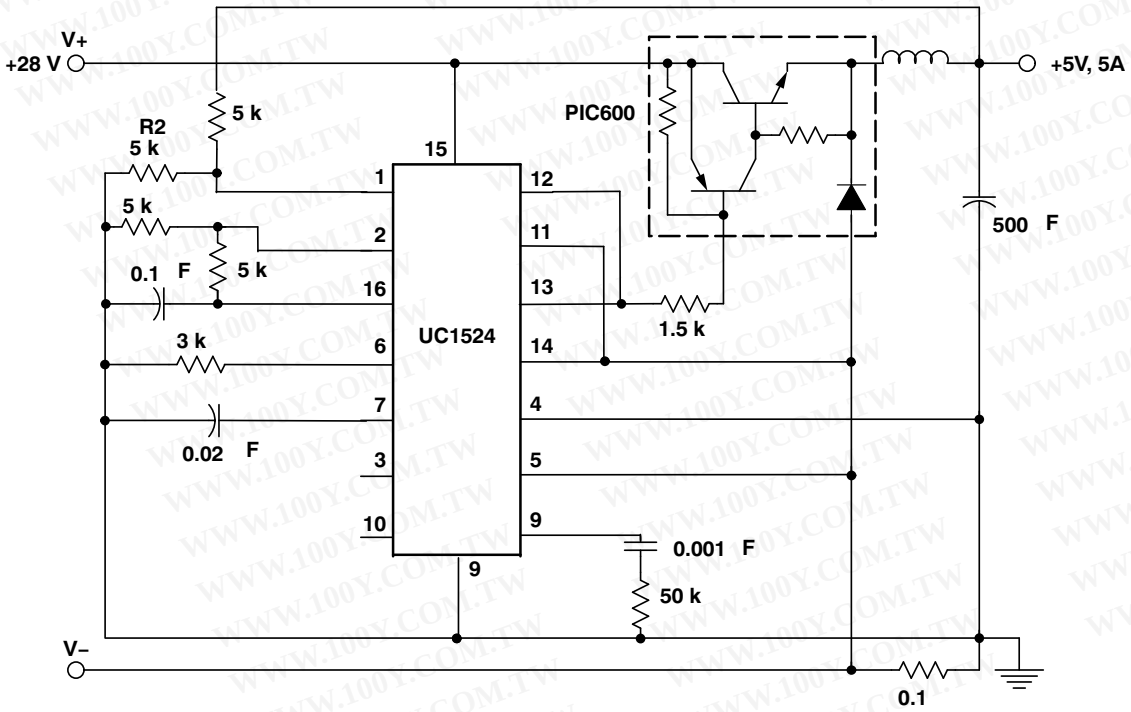



**Figure 6. Single-Ended LC Switching Regulator Circuit**

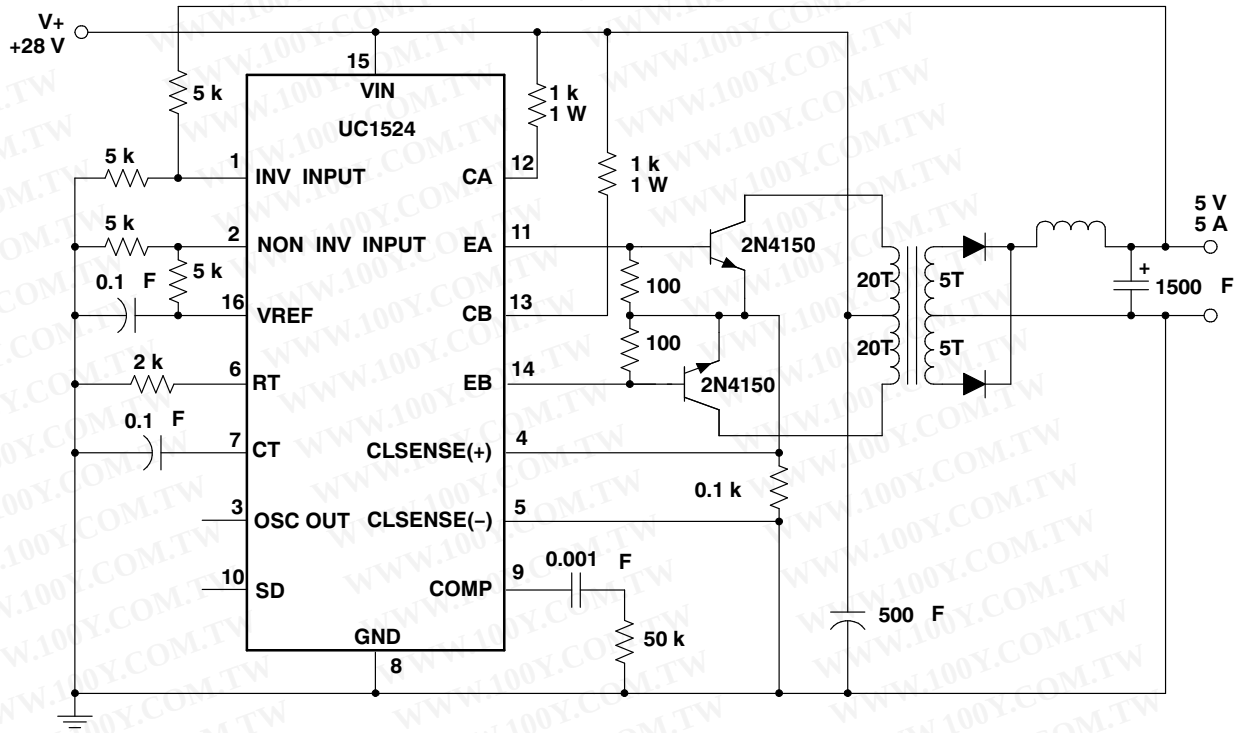



**Figure 7. Push-Pull Transformer Coupled Circuit**

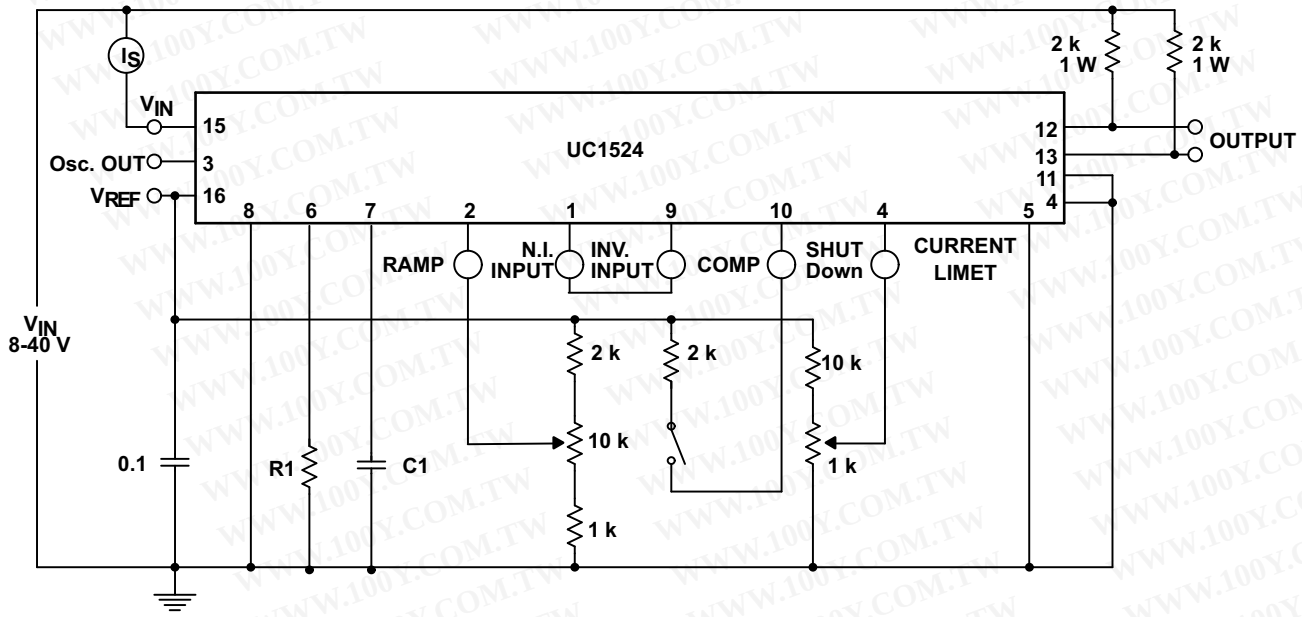



**Figure 8. Open Loop Test Circuit**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UC1524J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| UC1524J/80937 | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| UC1524J883B | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| UC2524DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | UC2524DW | Samples |
| UC2524J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -25 to 85 | | |
| UC2524N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -25 to 85 | UC2524N | Samples |
| UC2524NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -25 to 85 | UC2524N | Samples |
| UC3524-W | ACTIVE | WAFERSALE | YS | 0 | | TBD | Call TI | Call TI | | | Samples |
| UC3524D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3524D | Samples |
| UC3524DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3524D | Samples |
| UC3524DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3524DW | Samples |
| UC3524DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3524DW | Samples |
| UC3524DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3524DW | Samples |
| UC3524J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| UC3524N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3524N | Samples |
| UC3524NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3524N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF UC1524, UC3524 :**

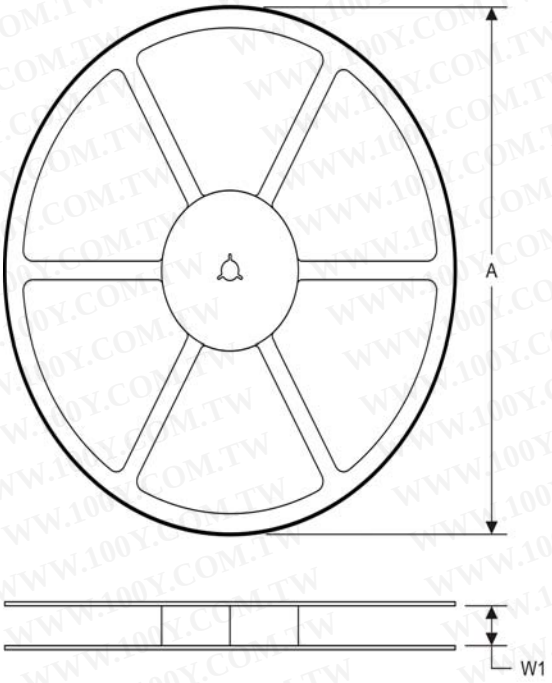
- Catalog: UC3524
- Military: UC1524

NOTE: Qualified Version Definitions:

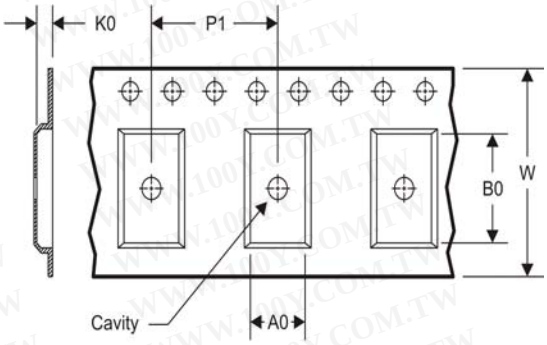
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



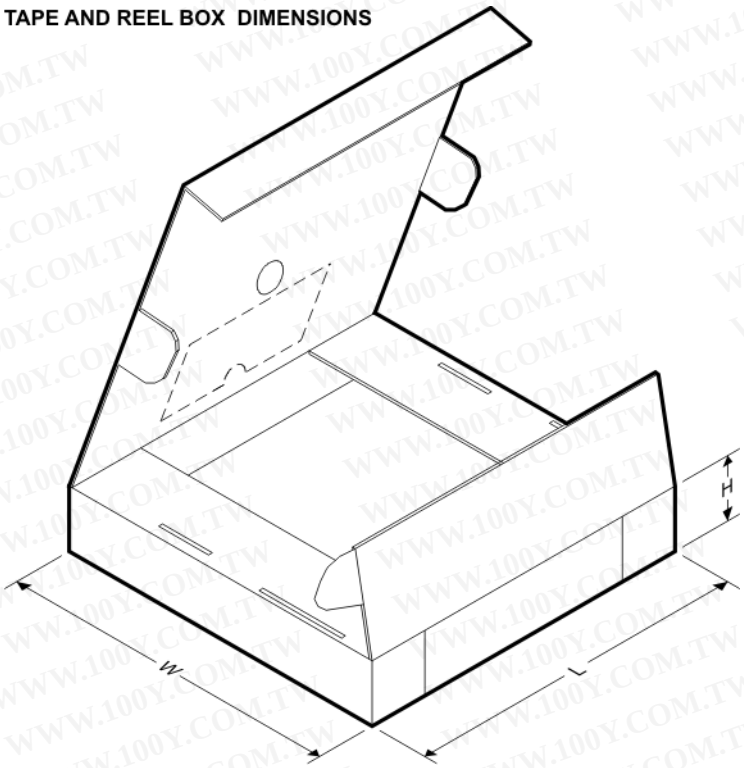

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC3524DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

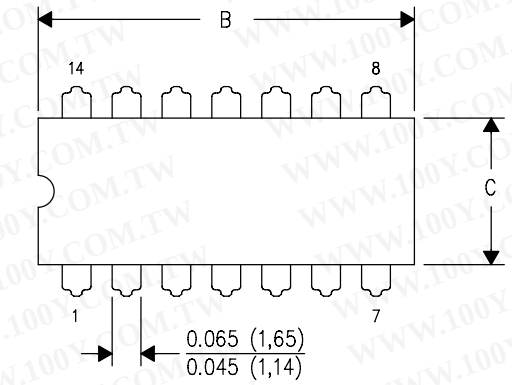



*All dimensions are nominal

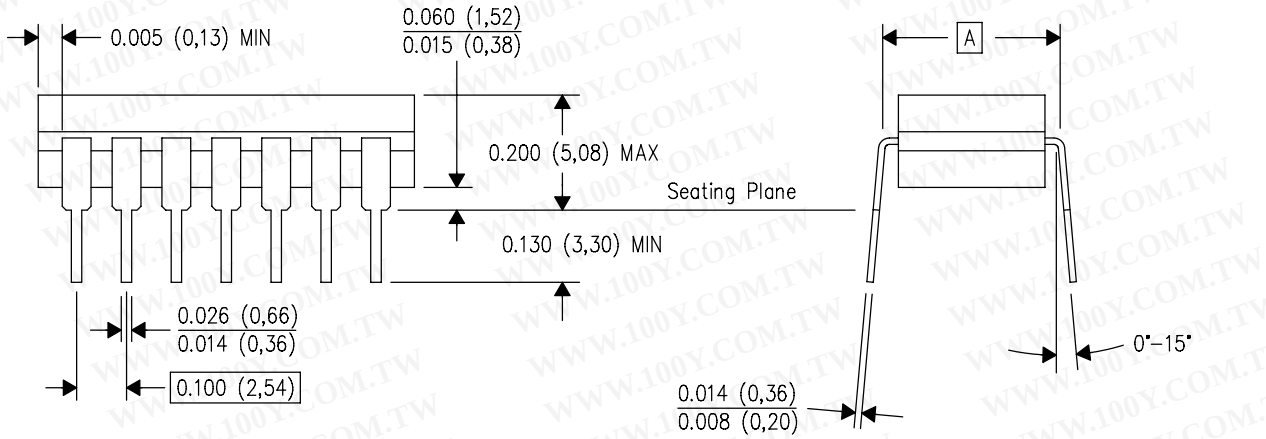
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC3524DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

# J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



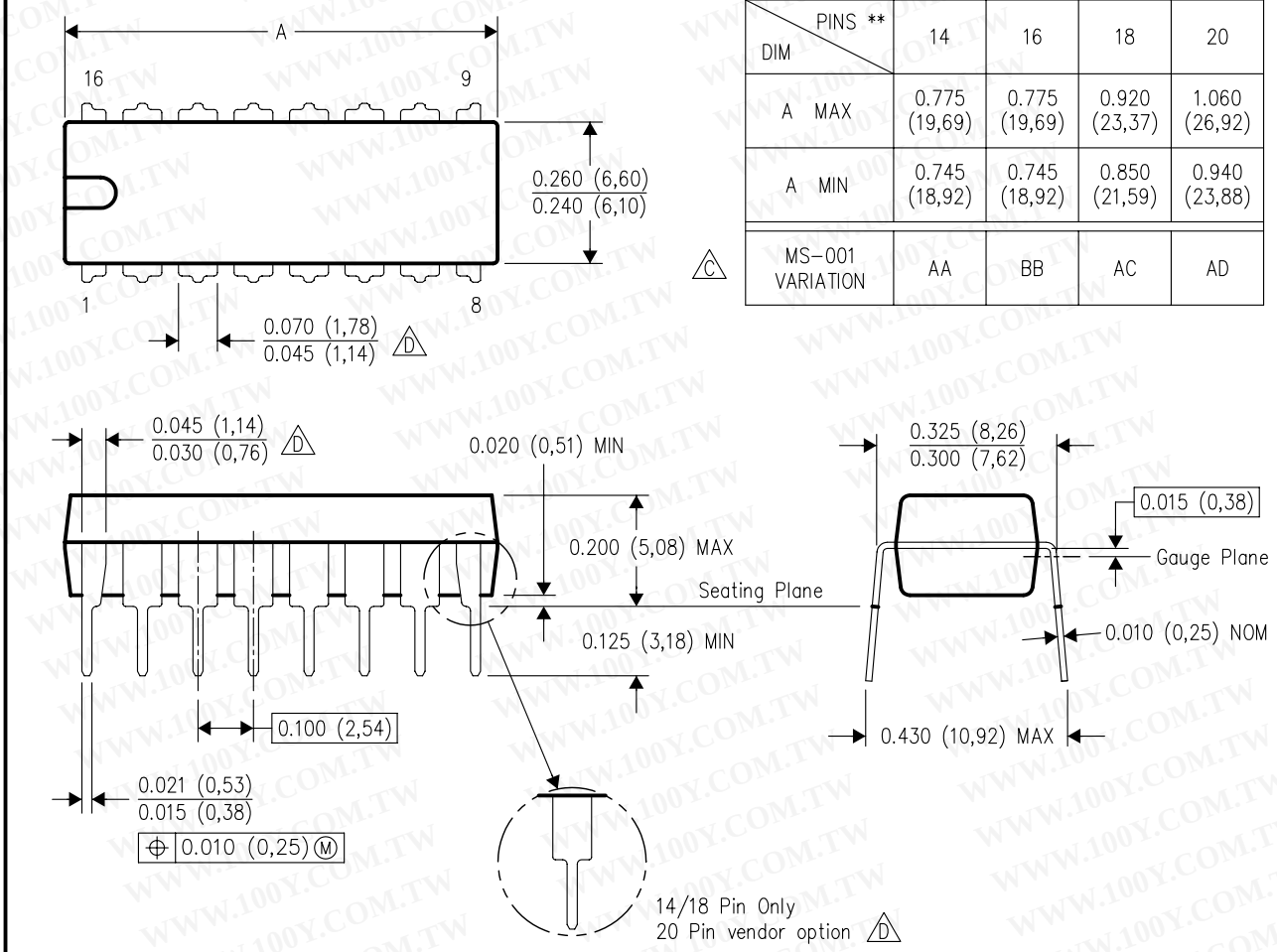

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

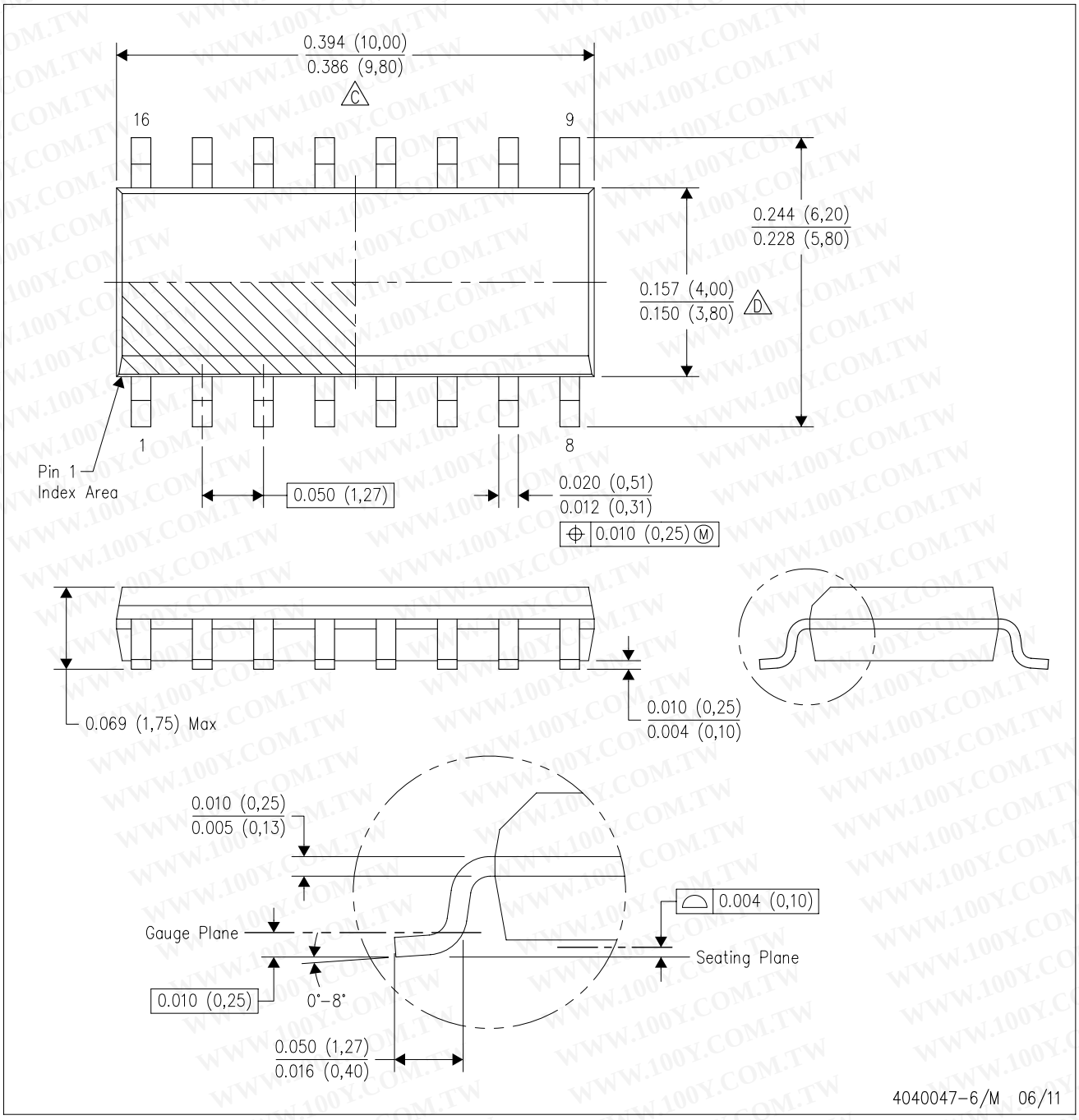



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| C MS–001 VARIATION | AA | BB | AC | AD |

4040049/E 12/2002

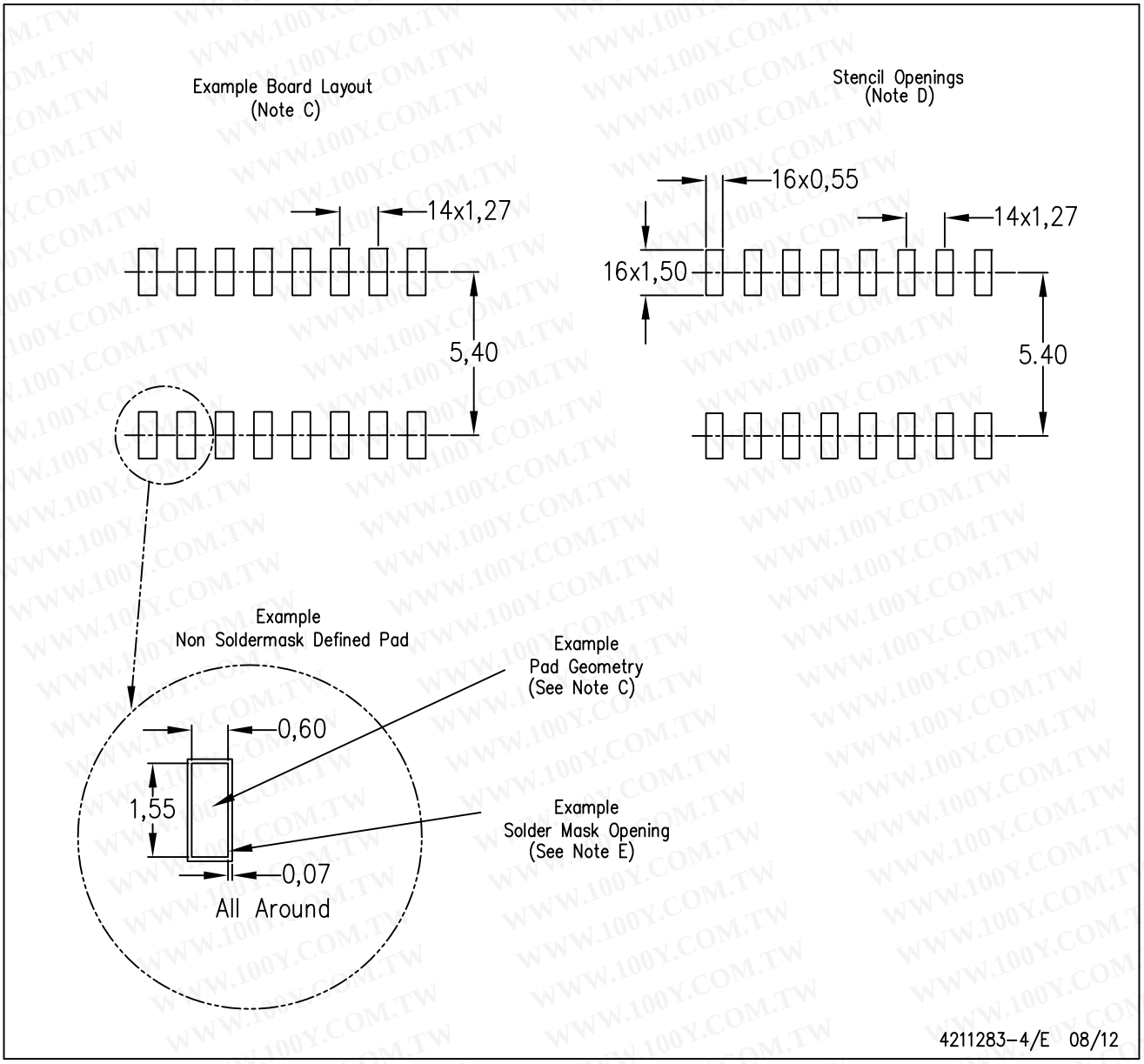
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



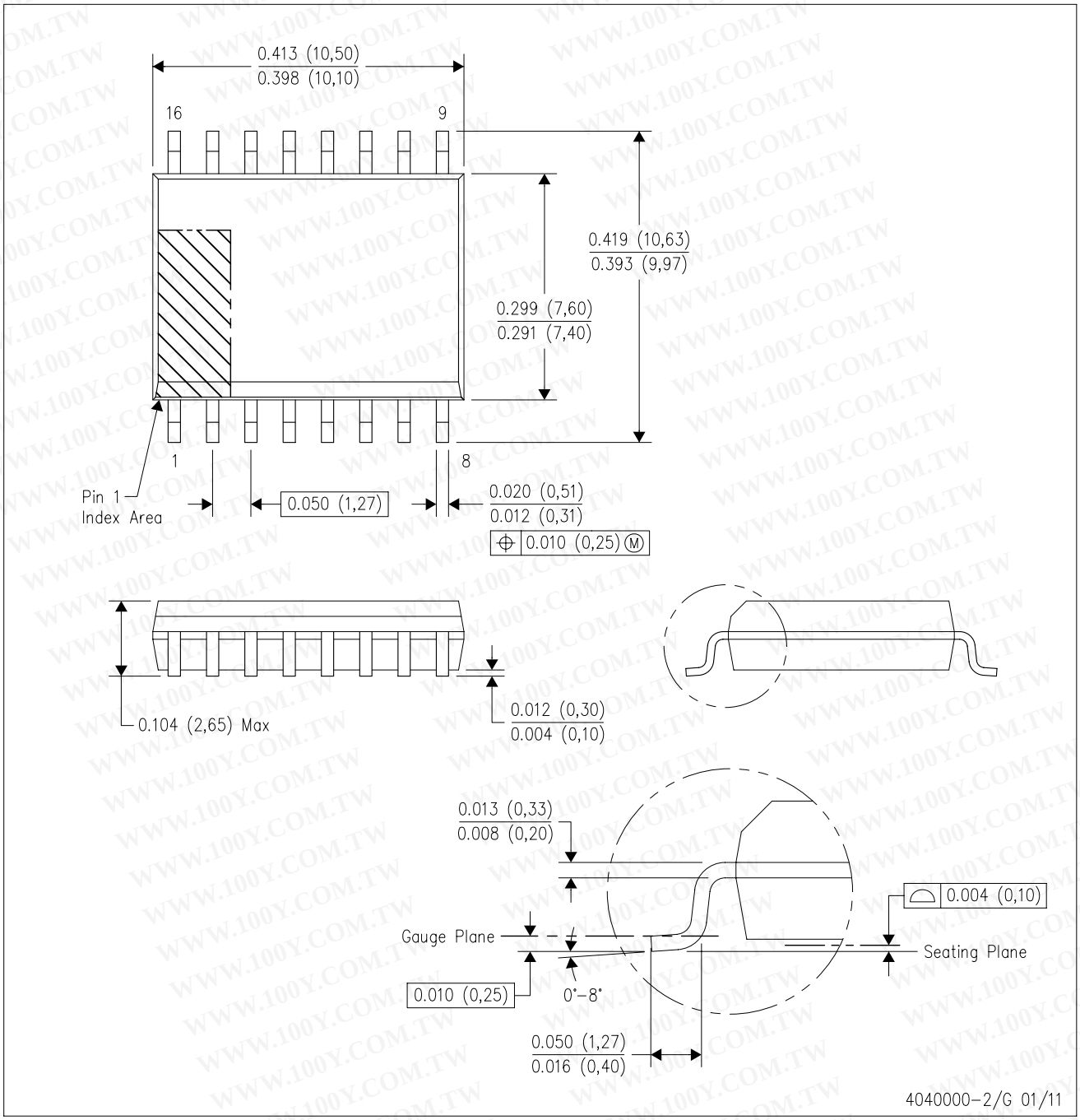

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



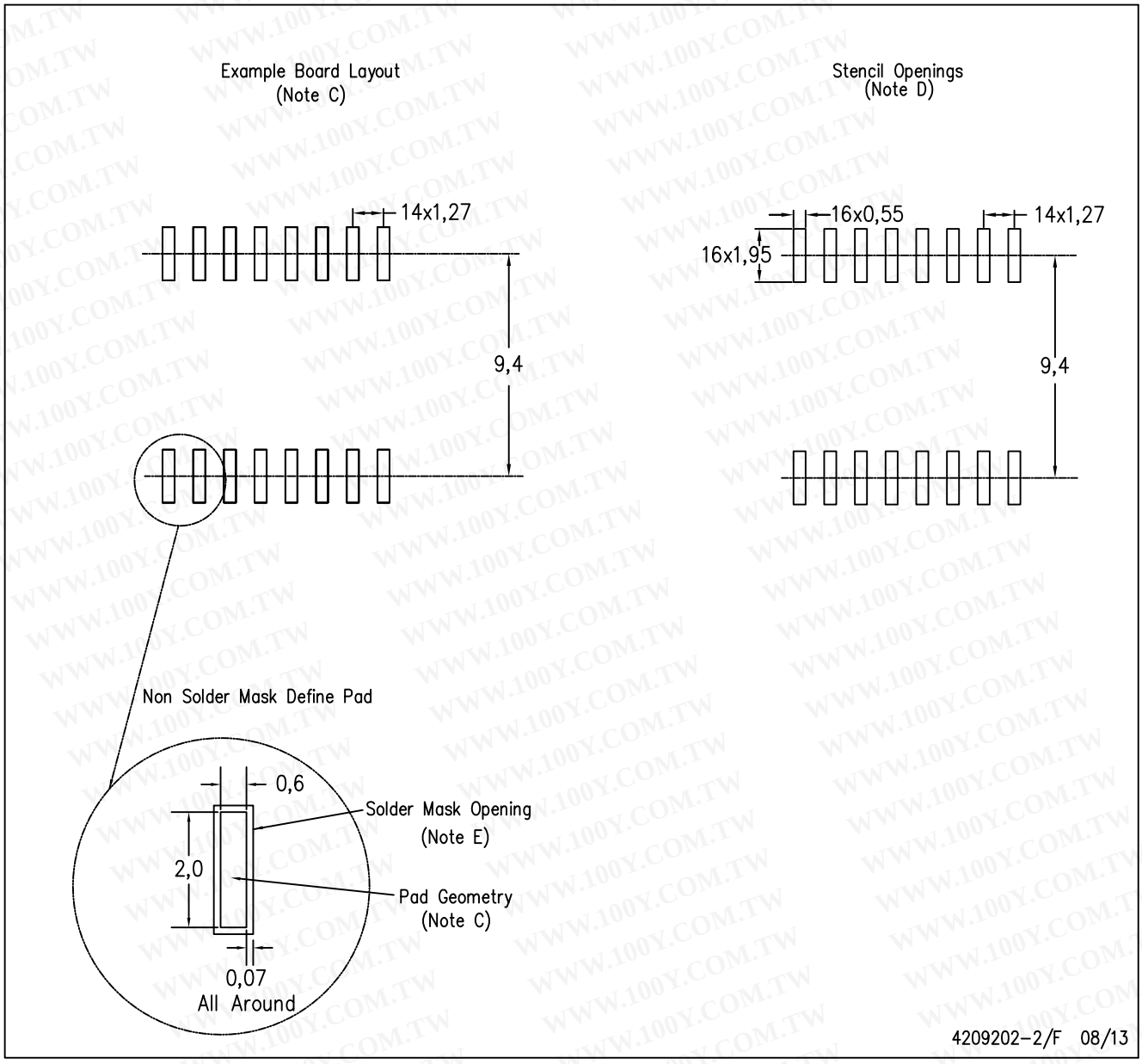

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

# DW (R-PDSO-G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.