REGULATING PULSE WIDTH MODULATORS

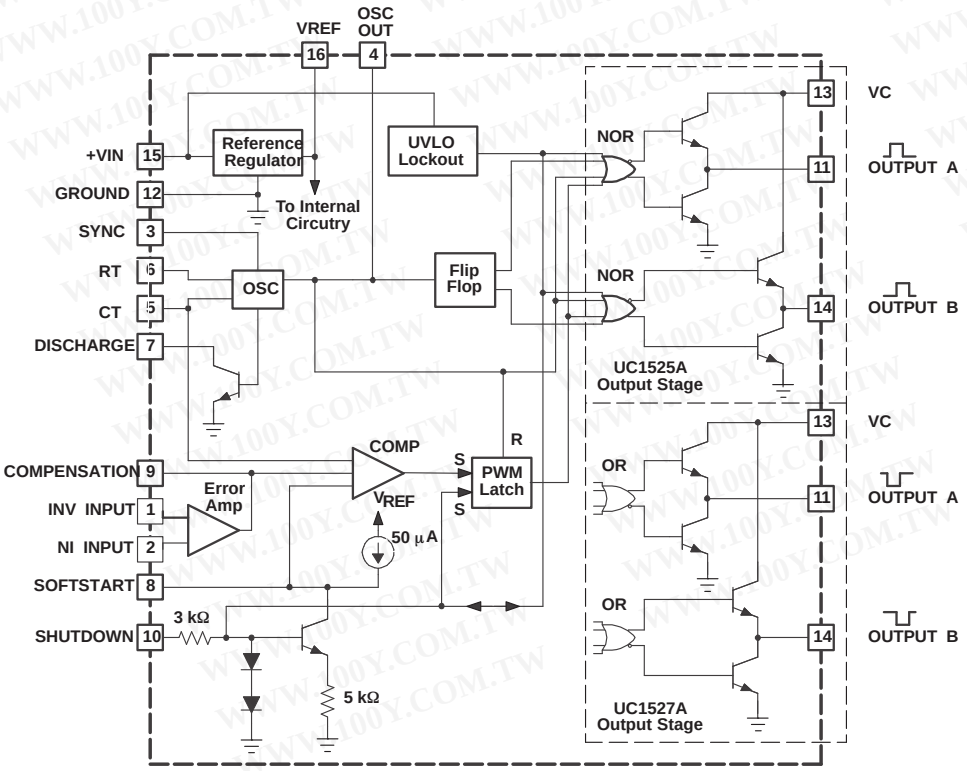
FEATURES

- 8-V to 35-V Operation
- 5.1-V Reference Trimmed to 1%
- 100-Hz to 500-kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout With Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers

DESCRIPTION

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.

BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (continued)

These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter- free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

ABSOLUTE MAXIMUM RATINGS(1)

		UCx52xA	UNIT
$+V_{IN}$	Supply voltage	40	V
V_C	Collector supply voltage	40	
	Logic inputs	–0.3 to +5.5	
	Analog inputs	–0.3 to $+V_{IN}$	
	Output current, source or sink	500	mA
	Reference output current	50	
	Oscillator charging current	5	
	Power dissipation at T_A = +25°C(2)	1000	mW
	Power dissipation at T_C = +25°C(2)	2000	
	Operating junction temperature	–55 to 150	°C
	Storage temperature range	–65 to 150	
	Lead temperature (soldering, 10 seconds)	300	

(1) Values beyond which damage may occur.
(2) See Thermal Characteristics table.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
$+V_{IN}$	Input voltage		8	35	V
V_C	Collector supply voltage		4.5	35	
	Sink/source load current (steady state)		0	100	mA
	Sink/source load current (peak)		0	400	
	Reference load current		0	20	
	Oscillator frequency range		100	400	Hz
	Oscillator timing resistor		2	150	kΩ
	Oscillator timing capacitorm		0.001	0.01	µF
	Dead time resistor range		0	500	Ω
	Operating ambient temperature range	UC1525A, UC1527A	–55	125	°C
		UC2525A, UC2527A	–25	85	
		UC3525A, UC3527A	0	70	

(1) Range over which the device is functional and parameter limits are assured.

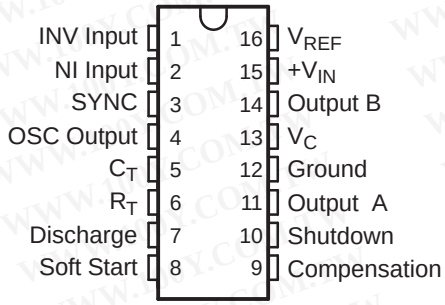
THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

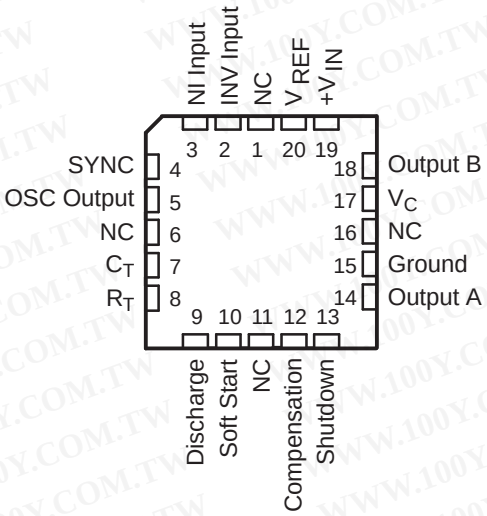
PACKAGE	θ_{JA}	θ_{JC}
J-16	80-120	28
N-16	90	45
DW-16	45-90	25
PLCC-20	43-75	34
LCC-20	70-80	20

CONNECTION DIAGRAMS

DIL-16
J or N PACKAGE
(TOP VIEW)



PLCC-20, LCC-20
Q AND L PACKAGES
(TOP VIEW)



NC − No internal connection

ELECTRICAL CHARACTERISTICS

$+V_{IN}$ = 20 V, and over operating temperature, unless otherwise specified, $T_A = T_J$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J = 25°C	UC152xA, UC252xA	5.05	5.10	5.15	V
		UC352xA	5.0	5.1	5.2	
Line regulationg	V_{IN} = 8 V to 35 V			10	20	mV
Load regulationg	I_L = 0 mA to 20 mA			20	50	
Temperature stability(1)	Over operating range			20	50	
Total output variation(1)	Line, load, and temperature	UC152xA, UC252xA	5.0		5.2	V
		UC352xA	4.95		5.25	
Shorter circuit current	V_{REF} = 0, T_J = 25°C			80	100	mA
Output noise Voltage(1)	10 Hz ≤ 10 kHz, T_J = 25°C			40	200	µVrms
Long term stability (1)	T_J = 125°C			20	50	mV
OSCILLATOR SECTION(2)						
Initial accuracy(1) (2)	T_J = 25°C			2%	6%	
Voltage stability(1) (2)	V_{IN} = 8 V to 35 V	UC152xA, UC252xA		0.3%	1%	
		UC352xA		1%	2%	
Temperature stability(1)	Over operating range			3%	6%	
Minimum frequency	R_T = 200 kΩ, C_T = 0.1 µF				120	Hz
Maximum frequency	R_T = 2 kΩ, C_T = 470 pF		400			kHz
Current mirror	I_{RT} = 2 mA		1.7	2.0	2.2	mA
Clock amplitude(1) (2)			3.0	3.5		V
Clock width(1) (2)	T_J = 25°C		0.3	0.5	1.0	µs
Syncronization threshold(1) (2)			1.2	2.0	2.8	V
Sync input current	Sync voltage = 3.5 V			1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)						
Input offset voltage		UC152xA, UC252xA		0.5	5	mV
		UC352xA		2	10	
Input bias current				1	10	µA
Input offset current					1	
DC open loop gain	R_L ≥ 10 MΩ		60	75		dB
Gain-bandwidth product(1)	A_V = 0 dB, T_J = 25°C		1	2		MHz
DC transconductanc(1) (3)	T_J = 25°C, 30 kΩ ≤ R_L ≤ 1 MΩ		1.1	1.5		mS
Low-level output voltage				0.2	0.5	V
High-level output voltage			3.8	5.6		
Common mode rejection	V_{CM} = 1.5 V to 5.2 V		60	75		dB
Supply voltage rejection	V_{IN} = 8 V to 35 V		50	60		

(1) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.
(2) Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 µF, R_D = 0. Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T\left(0.7R_T + 3R_D\right)}$$

(3) DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

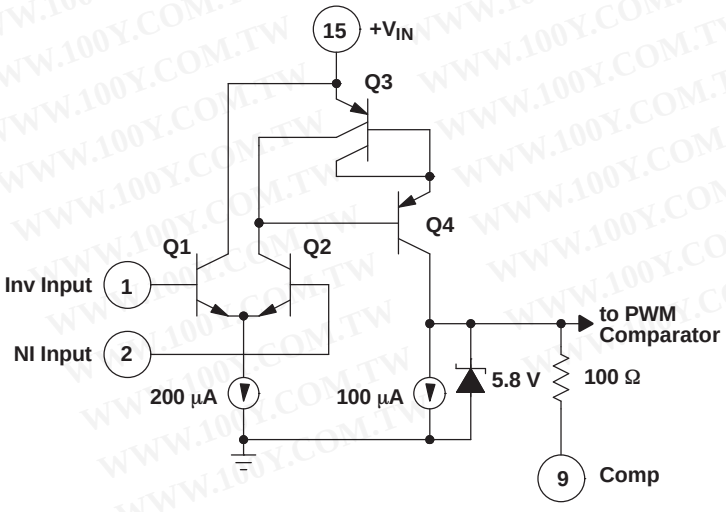
ELECTRICAL CHARACTERISTICS (continued)

$+V_{IN}$ = 20 V, and over operating temperature, unless otherwise specified, $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR					
Minimum duty-cycle				0%	
Maximum duty-cycle		45%	49%		
Input threshold(4)	Zero duty-cycle	0.7	0.9		V
	Maximum duty-cycle		3.3	3.6	
Input bias current(4)			0.05	1.0	µA
SHUTDOWN					
Soft-start current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	µA
Soft-start low level	V_{SD} = 2.5 V		0.4	0.7	V
Shutdown threshold	To outputs, V_{SS} = 5.1 V, T_J = 25°C	0.6	0.8	1.0	
Shutdown input current	V_{SD} = 2.5 V		0.4	1.0	mA
Shutdown Delay(5)	V_{SD} = 2.5 V, T_J = 25°C		0.2	0.5	µs
OUTPUT DRIVERS (each output) (V_C = 20 V)					
Low-level output voltage	I_{SINK} = 20 mA		0.2	0.4	V
	I_{SINK} = 100 mA		1.0	2.0	
High-level output voltage	I_{SOURCE} = 20 mA	18	19		
	I_{SOURCE} = 100 mA	17	18		
Undervoltage lockout	V_{COMP} and V_{SS} = High	6	7	8	
V_C OFF Current(6)	V_C = 35 V			200	µA
Rise Time(5)	C_L = 1 nF, T_J = 25°C		100	600	ns
Fall Time(5)	C_L = 1 nF, T_J = 25°C		50	300	
TOTAL STANDBY CURRENT					
Supply Current	V_{IN} = 35 V		14	20	mA

(4) Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 µF, R_D = 0 Ω.
(5) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.
(6) Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

UC1525A Error Amplifier



PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

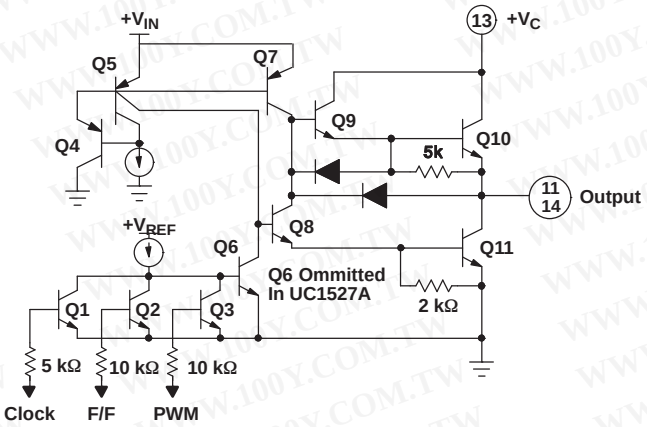


Figure 1. UC1525A Output Circuit (1/2 circuit shown)

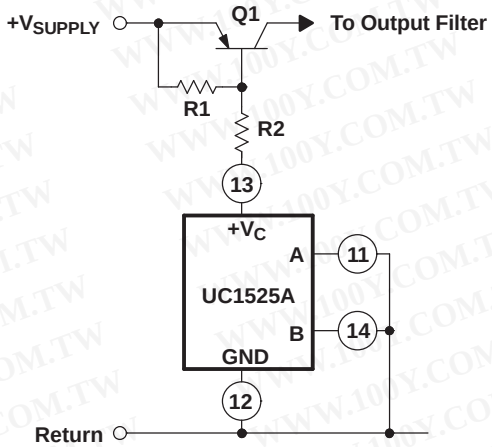


Figure 2. Grounded Driver Outputs For Single-Ended Supplies

For single-ended supplies, the driver outputs are grounded. The V_C termainal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)

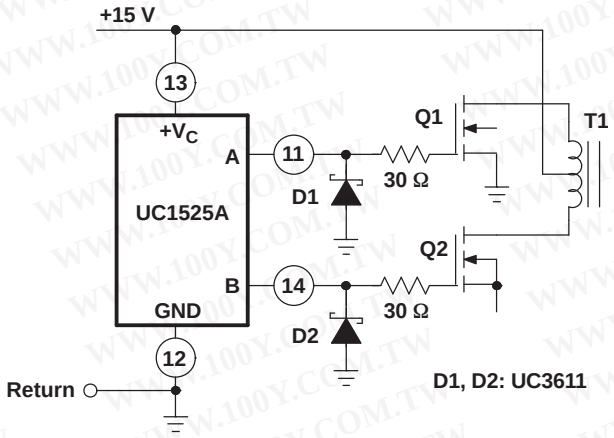


Figure 3. Output Drivers With Low Source Impedance

The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

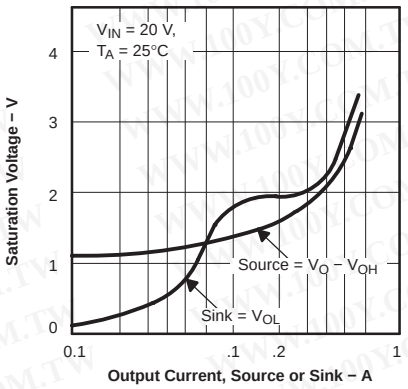


Figure 4. UC1525A Output Saturation Characteristics.

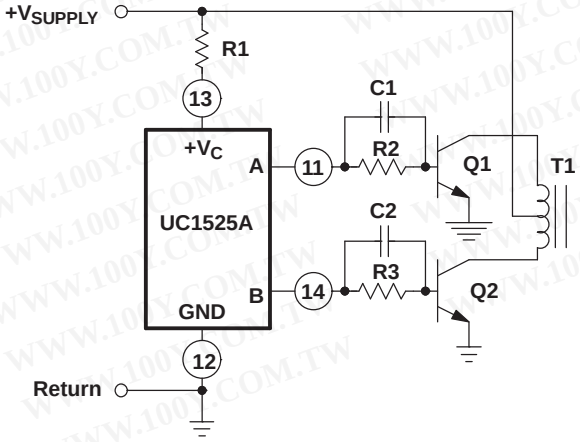


Figure 5. Conventional Push-Pull Bipolar Design

In conventional push-pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)

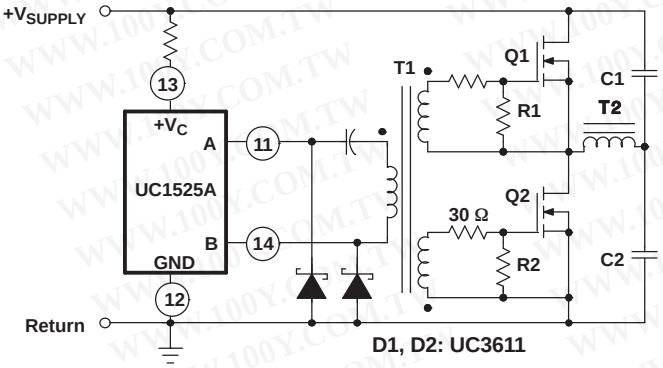


Figure 6. Low Power Transformers

Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

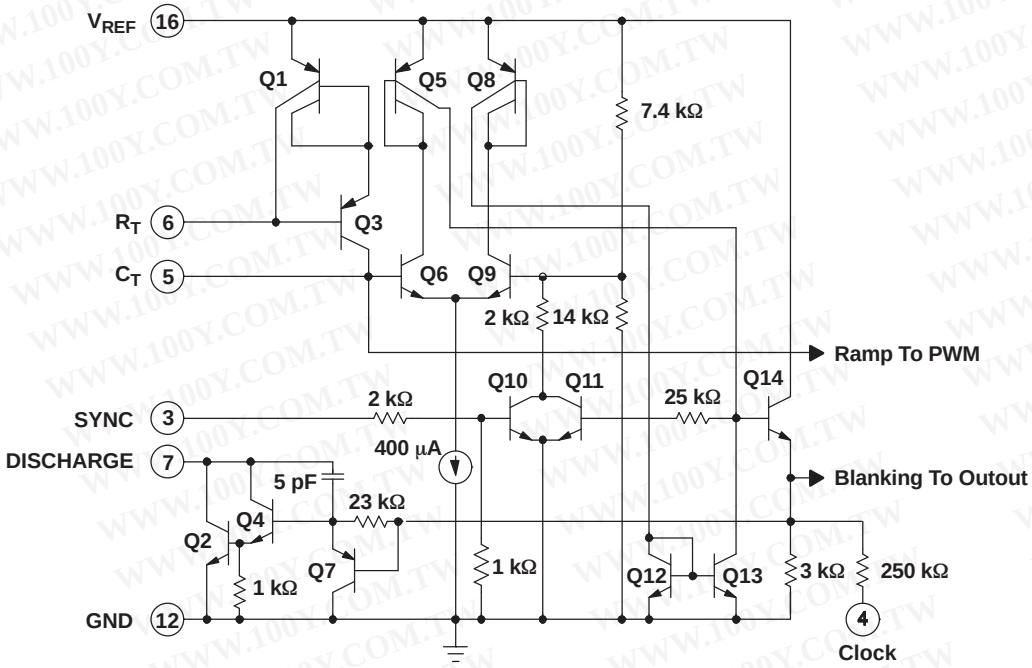


Figure 7. UC1525A Oscillator Schematic

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)

Shutdown Options (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions; the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150-A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation. All transitions of the voltage on pin 10 should be within the time frame of one clock cycle and not repeated at a frequency higher than 10 clock cycles.

Oscillator Charge Time vs R_T and C_T

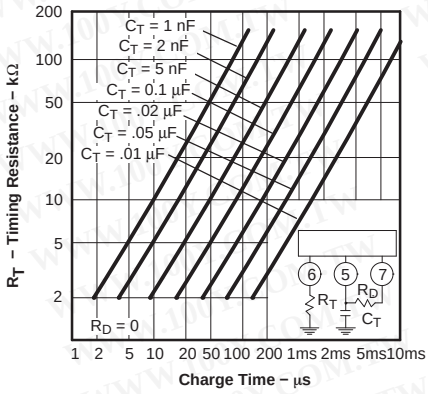


Figure 8.

Oscillator Discharge Time vs R_T C_T

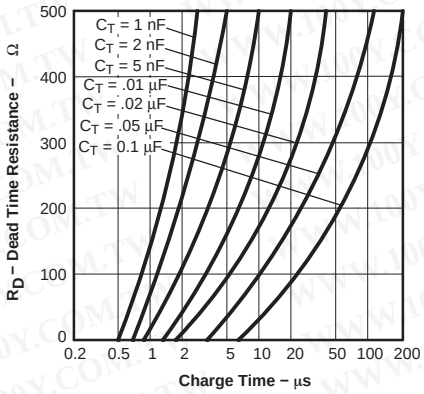


Figure 9.

Maximum Value R_D vs Minimum Value R_T

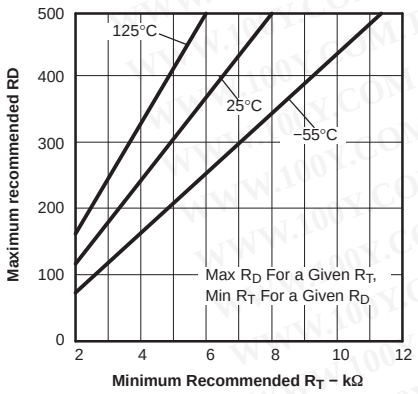


Figure 10.

Error Amplifier Voltage Gain and Phase vs Frequency

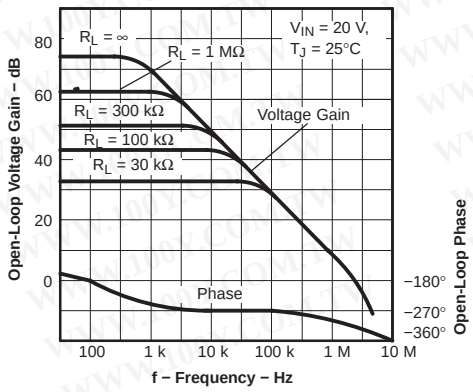


Figure 11.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)

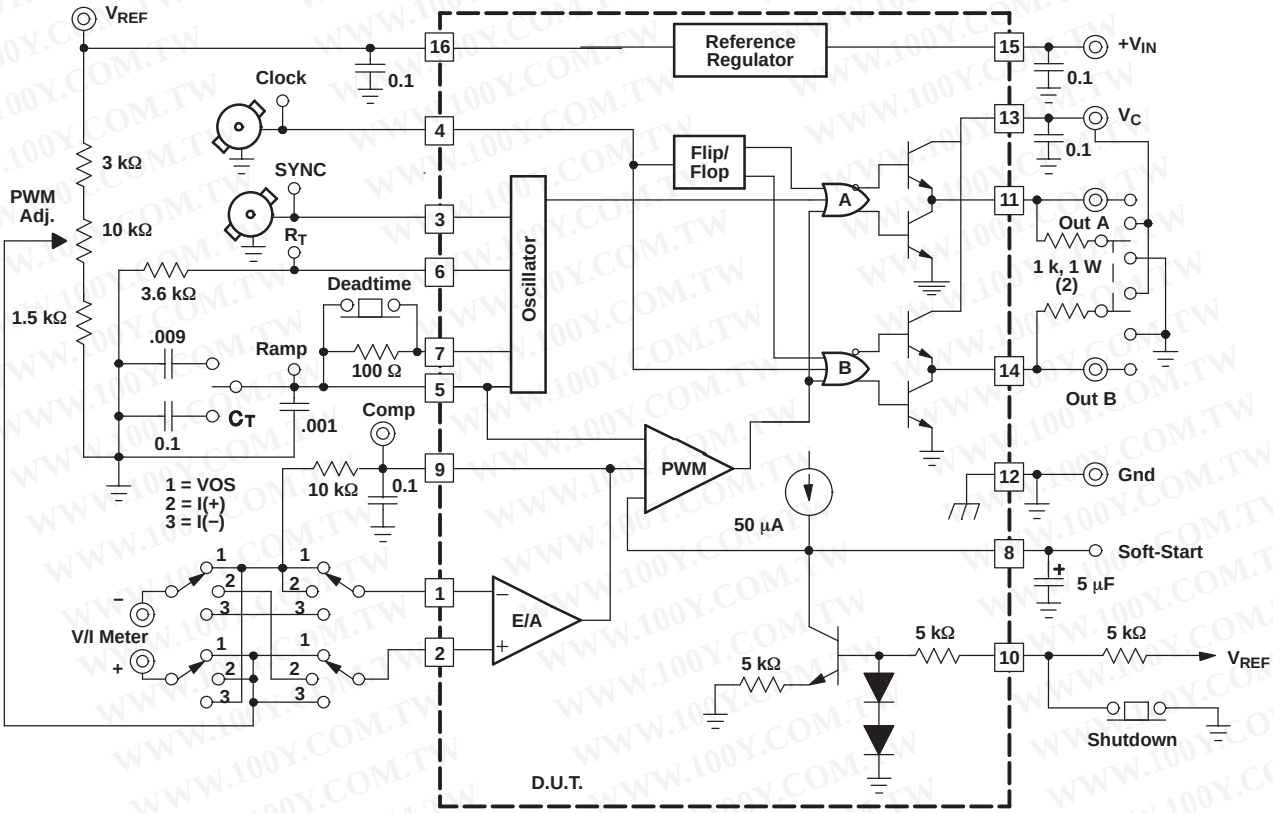
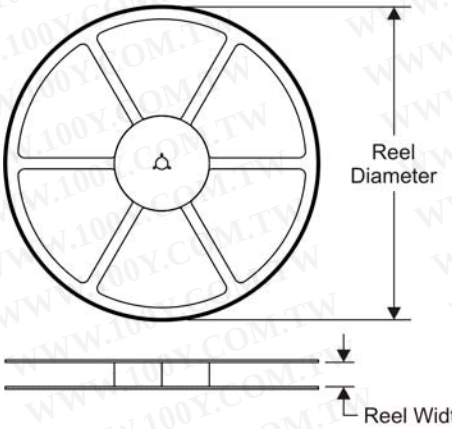


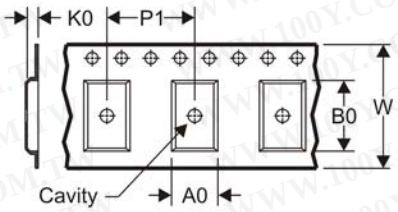
Figure 12. Lab Test Fixture

TAPE AND REEL INFORMATION

REEL DIMENSIONS

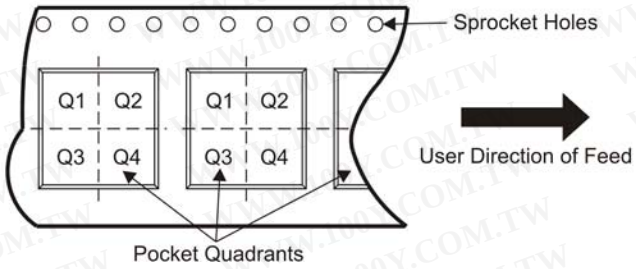


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

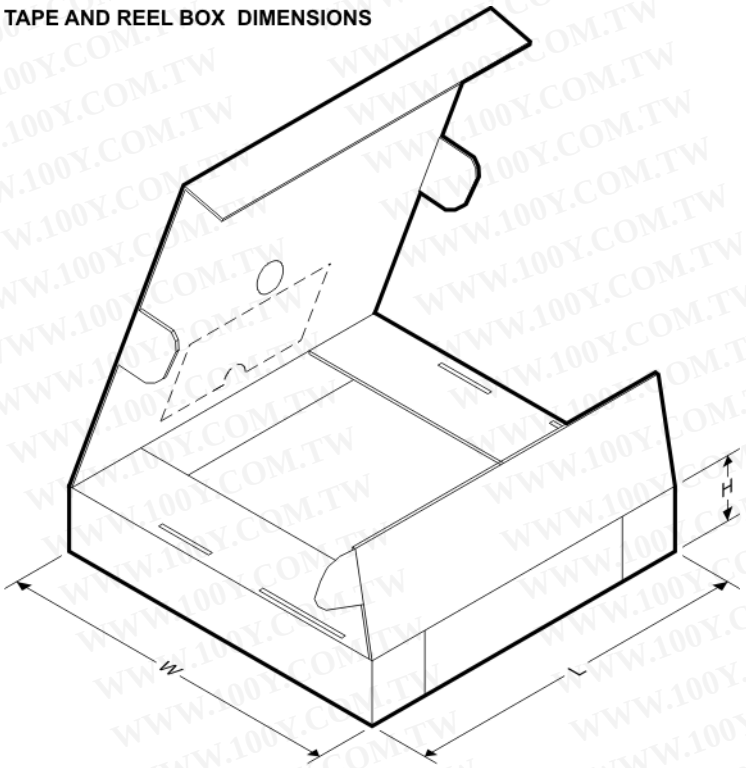
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2525ADWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3525ADWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3525AQTR	PLCC	FN	20	1000	330.0	16.4	10.3	10.3	4.9	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2525ADWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3525ADWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3525AQTR	PLCC	FN	20	1000	346.0	346.0	33.0