v00.0511

HMC985LP4KE

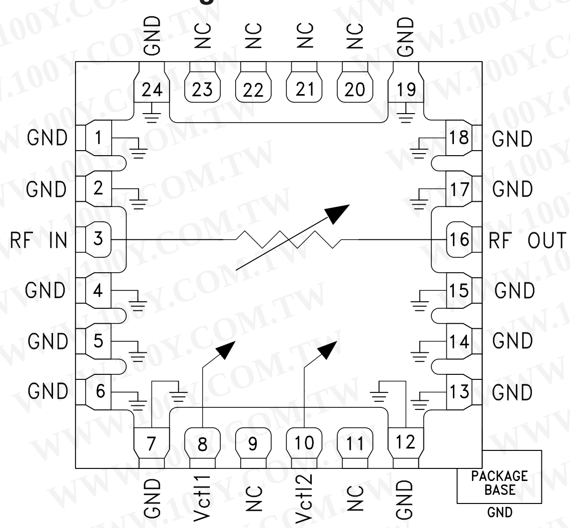
GaAs MMIC VOLTAGE - VARIABLE ATTENUATOR, 10 - 40 GHz

Typical Applications

The HMC985LP4KE is ideal for:

- Point-to-Point Radio
- VSAT Radio
- Test Instrumentation
- Microwave Sensors
- Military, ECM & Radar

Functional Diagram



Features

Wide Bandwidth: 10 - 40 GHz

Excellent Linearity: +32 dB Input IP3

Wide Attenuation Range: 35 dB

No External Matching

24 Lead 4x4 mm SMT Package: 16 mm²

General Description

The HMC985LP4KE is an absorptive Voltage Variable Attenuator (VVA) which operates from 10 - 40 GHz and is ideal in designs where an analog DC control signal must be used to control RF signal levels over a 35 dB dynamic range. It features two shunt-type attenuators which are controlled by two analog voltages, Vctl1 and Vctl2. Optimum linearity performance of the attenuator is achieved by first varying Vctl1 of the first attenuation stage from -3V to 0V with Vctl2 fixed at -3V. The control voltage of the second attenuation stage, Vctl2, should then be varied from -3V to 0V with Vctl1 fixed at 0V.

if the Vctl1 and Vctl2 pins are connected together it is possible to achieve the full analog attenuation range with only a small degradation in input IP3 performance. Applications include AGC circuits and temperature compensation of multiple gain stages in microwave point-to-point and VSAT radios.

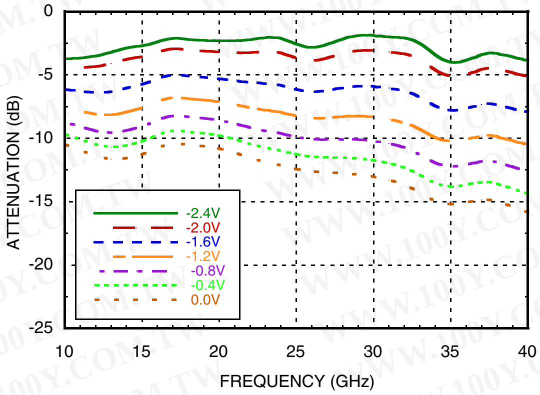
Electrical Specifications, T_A = +25 °C, Test Condition Vctl1 = Vctl2

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss [1]	10 - 20 GHz		3	3.5	dB
	20 - 30 GHz		3	4	dB
	30 -40 GHz		3.5	4.5	dB
Attenuation Range	10 - 20 GHz	25	30		dB
	20 - 30 GHz	30	35		dB
	30 - 40 GHz	35	40		dB
Input Return Loss	10 - 40 GHz		13		dB
Output Return Loss	10 - 40 GHz		13		dB
Input Third Order Intercept (two-tone input Power = 10 dBm Each Tone) [2]			33		dBm

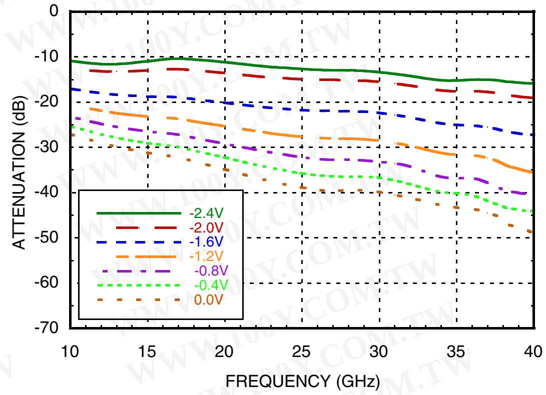
[1] Vcntl1 = Vcntl2 =-2.4V
[2] Vcntl1 = Vcntl2 =-2.0V worst case

GaAs MMIC VOLTAGE - VARIABLE ATTENUATOR, 10 - 40 GHz

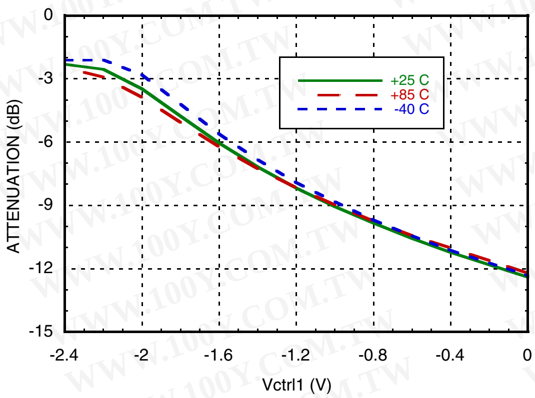
Attenuation vs. Frequency over Vctl1 = Variable, Vctl2 = -3V



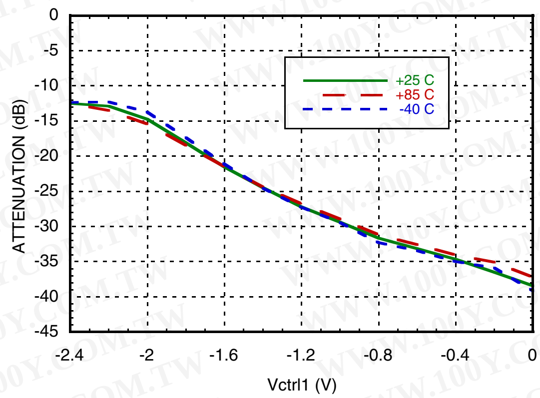
Attenuation vs. Frequency over Vctl1 = 0V, Vctl2 = Variable



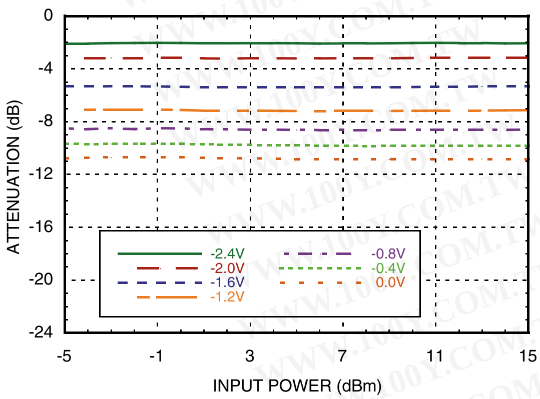
Attenuation vs. Vctl1 Over Temperature @ 25 GHz, Vctl2 = -3V



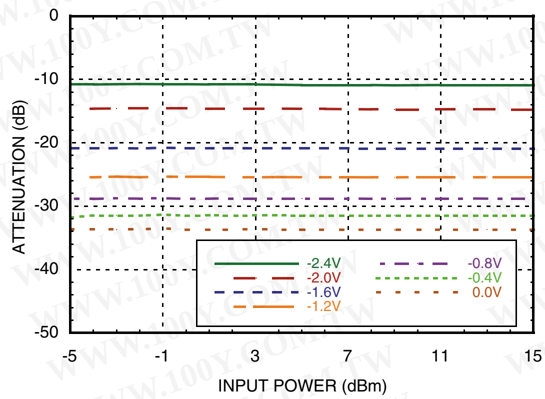
Attenuation vs. Vctl2 Over Temperature @ 30 GHz, Vctl1 = 0V



Attenuation vs. Pin @ 20 GHz over Vctl1 Vctl1 = Variable, Vctl2 = -3V



Attenuation vs. Pin @ 20 GHz over Vctl2 Vctl2 = Variable, Vctl1 = 0V



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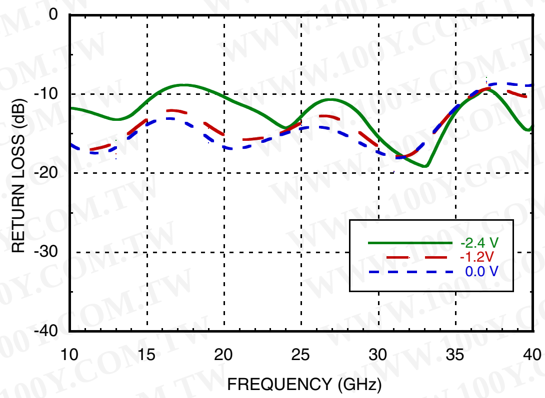
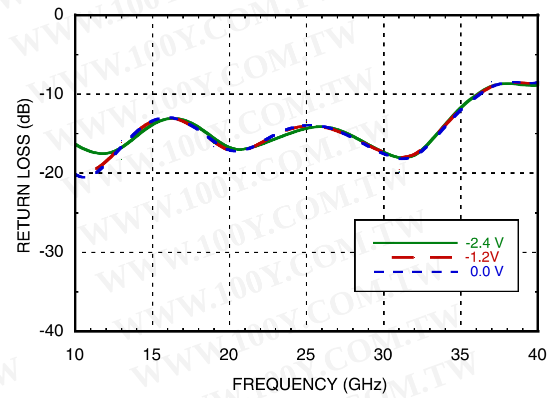
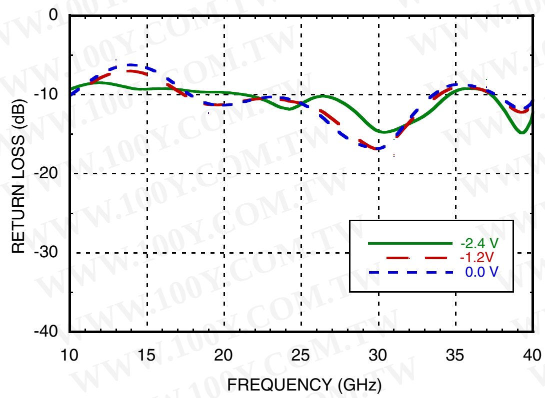
Input Return Loss
Vctl1 = Variable, Vctl2 = -3V



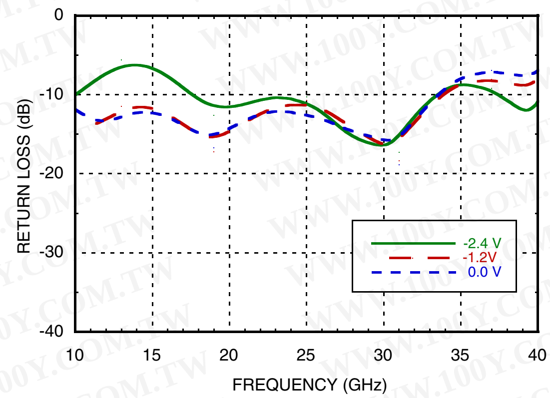
Input Return Loss
Vctl1 = 0V, Vctl2 = Variable



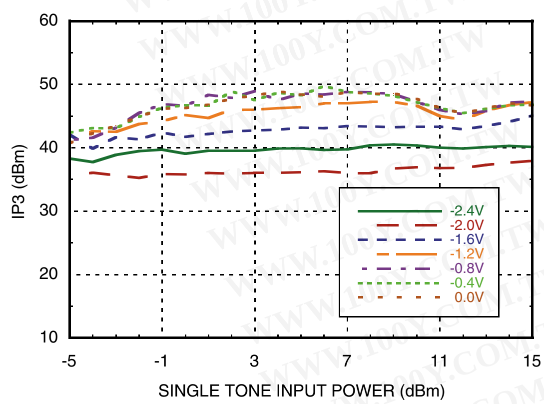
Output Return Loss
Vctl1 = Variable, Vctl2 = -3V



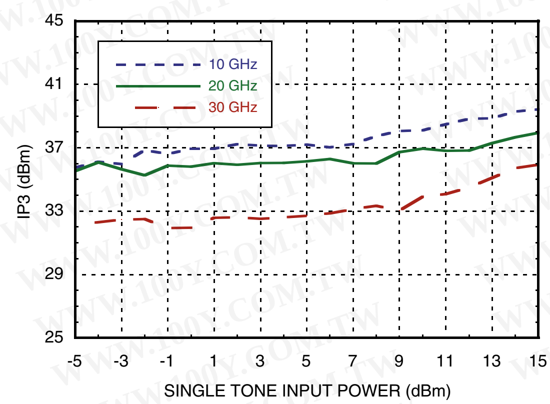
Output Return Loss
Vctl1 = 0V, Vctl2 = Variable



Input IP3 vs. Input Power @ 20 GHz
Vctl1 = Variable, Vctl2 = -3V



Input IP3 vs. Input Power Over Frequency
Vctl1 = -2V, Vctl2 = -3V [1]



[1] Worst Case IP3

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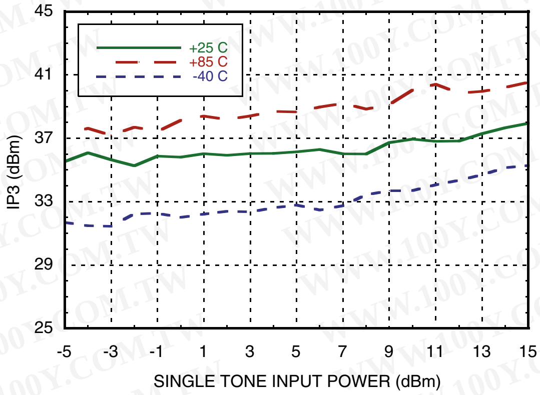
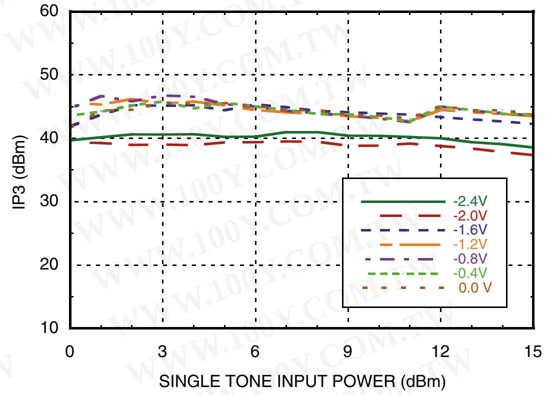
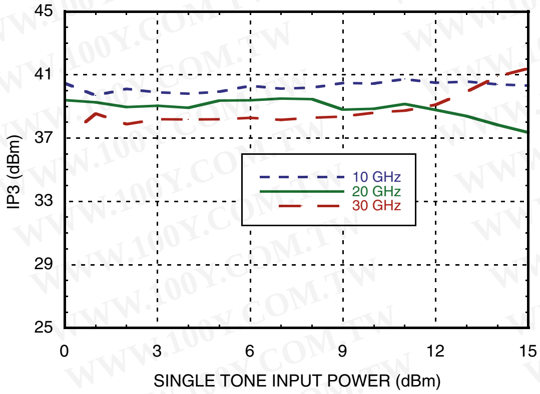
Input IP3 vs. Input Power Over Temperature @ 20 GHz, Vctl1 = -2V, Vctl2 = -3V [1]



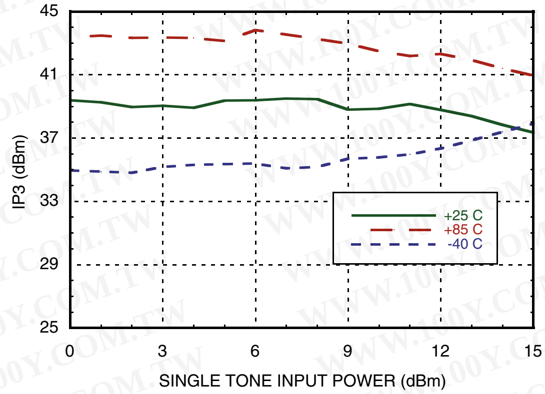
Input IP3 vs. Input Power @ 20 GHz Vctl2 = Variable, Vctl1 = 0V



Input IP3 vs. Input Power Over Frequency Vctl2 = -2V, Vctl1 = 0V [1]



Input IP3 vs Input Power over Temperature @ 20 GHz, Vctl2 = -2V, Vctl1 = 0V [1]



[1] Worst Case IP3

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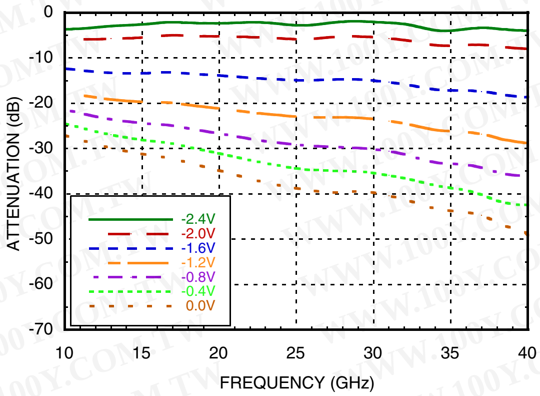
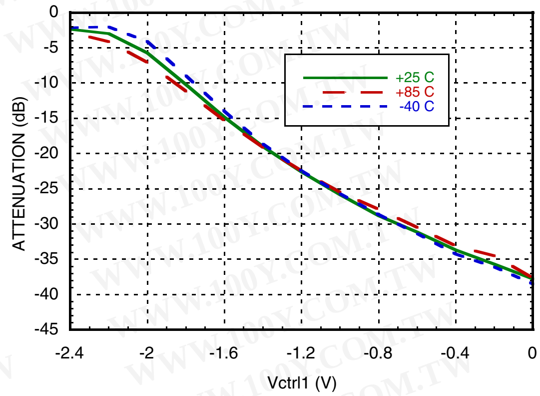
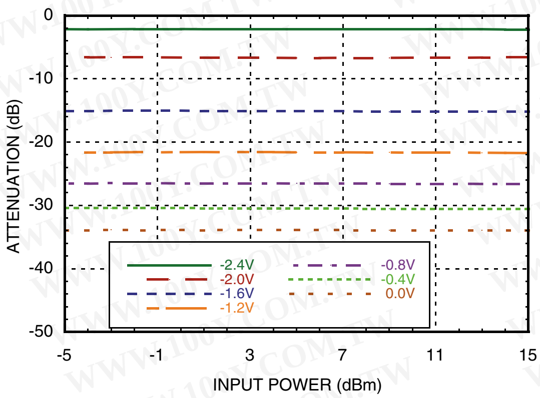
Attenuation vs Frequency Over Vctrl Vctl1 = Vctl2



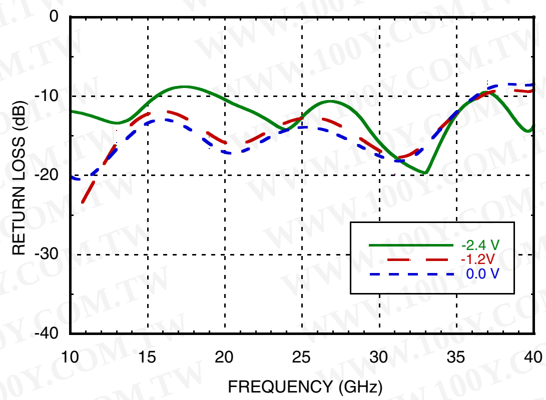
Attenuation vs. Vctrl Over Temperature @ 20 GHz, Vctl1 = Vctl2



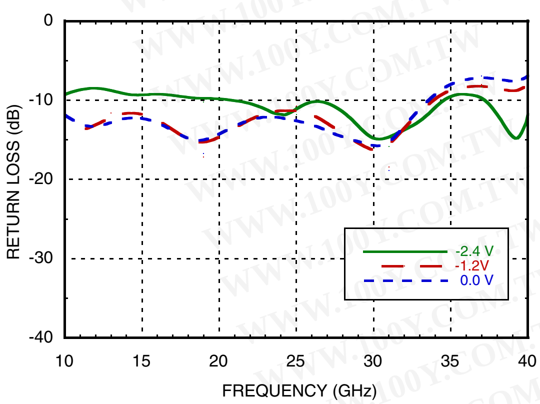
Attenuation vs. Pin @ 20 GHz Over Vctl Vctl1 = Vctl2



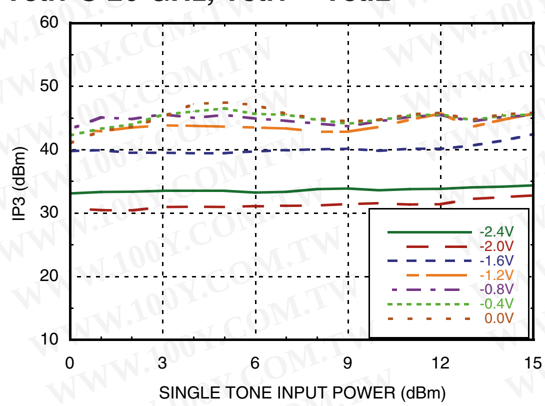
Input Return Loss, Vctl1 = Vctl2



Output Return Loss, Vctl1 = Vctl2



Input IP3 vs. Input Power Over Vctrl @ 20 GHz, Vctl1 = Vctl2



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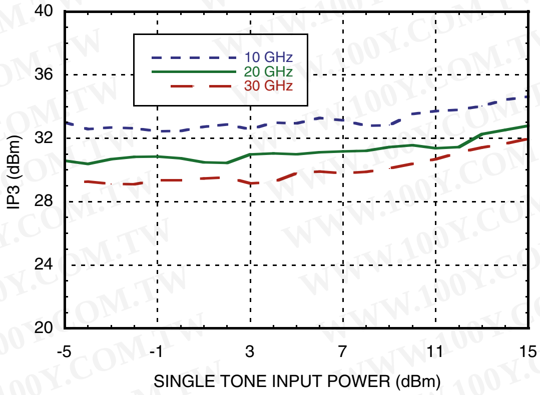
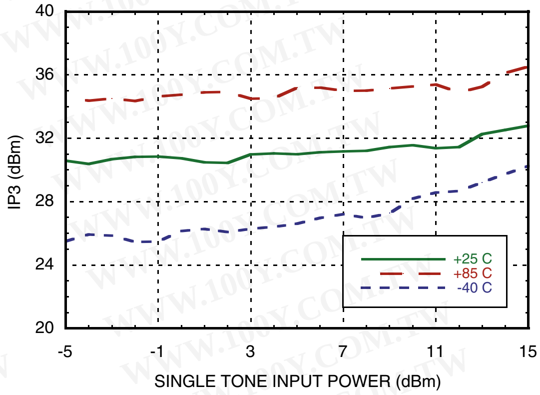
Input IP3 vs. Input Power Over Frequency Vctl1 = Vctl2



Input IP3 vs. Input Power Over Temperature @ 20 GHz Vctl1 = Vctl2



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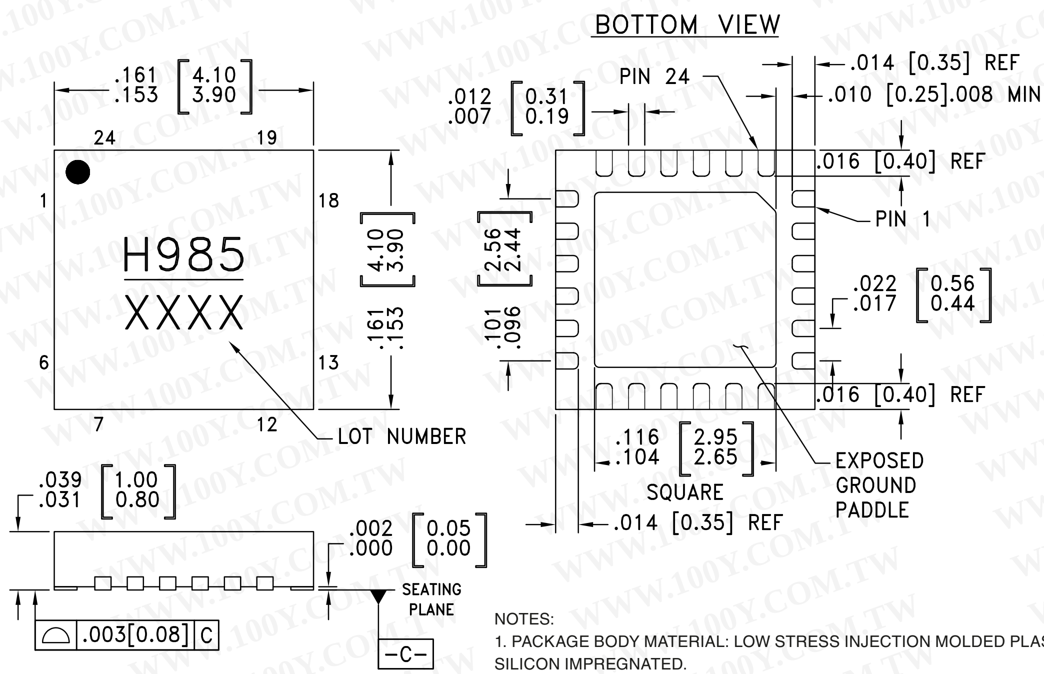
Absolute Maximum Ratings

Control Voltage	+1 to -5V
Input RF Power	30 dBm
Maximum Junction Temperature	165 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	62 °C/W
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 125°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
HMC985LP4KE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H985 XXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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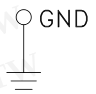
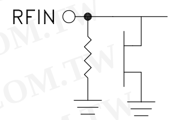
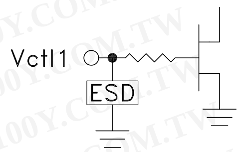
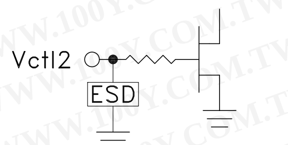
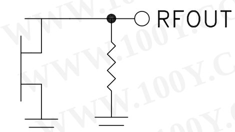
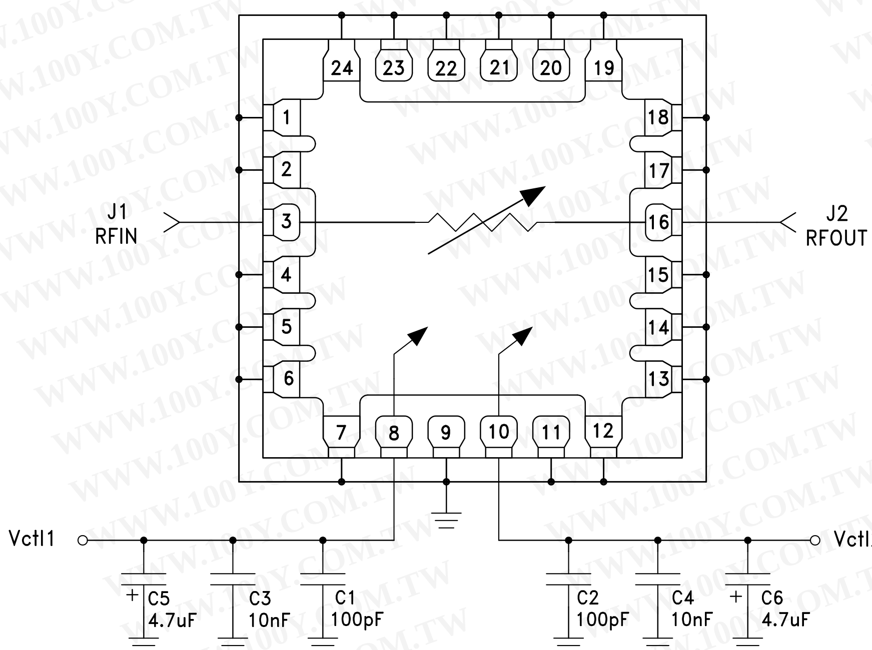
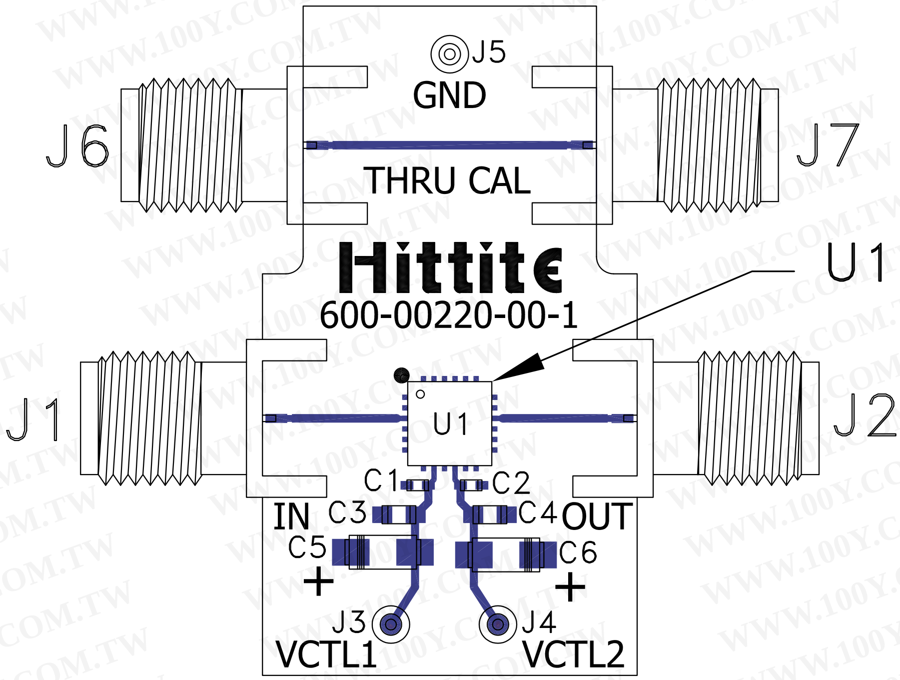
Pin Descriptions

Pin Number	Function	Description	Pin Schematic
1, 2, 4-7, 12-15, 17-19, 24	GND	These pins and package bottom must be connected to RF/DC ground externally.	
3	RFIN	This pad is DC coupled and matched to 50 Ohms.	
8	Vctl1	Control Voltage 1.	
9, 11, 20-23	NC	These pins are not connected internally, however all data shown herein was measured with these pins connected to RF/DC ground externally.	
10	Vctl2	Control Voltage 2.	
16	RFOUT	This pad is DC coupled and matched to 50 Ohms.	

Assembly Diagram



Evaluation PCB



List of Materials for Evaluation PCB EVAL01- HMC985LP4KE [1]

Item	Description
J1-J2, J6-J7	K Connectors.
J3-J5	DC Pins.
C1-C2	100pF Capacitors, 0402 Pkg.
C3-C4	0.01 µF Capacitor, 0603 Pkg.
C5-C6	4.7 µF Case A, Tantalum.
U1	HMC985LP4KE VVA.
PCB	600-00220-00 Evaluation PCB.

[1] Reference this number when ordering complete evaluation PCB

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: