Dual-Current Output, Parallel Input, 16-/14-Bit Multiplying DACs with 4-Quadrant Resistors

AD5547/AD5557

FEATURES

- Dual channel
- 16-bit resolution: AD5547
- 14-bit resolution: AD5557
- 2- or 4-quadrant, 6.8 MHz BW multiplying DAC
- ±1 LSB DNL
- ±1 LSB INL
- Operating supply voltage: 2.7 V to 5.5 V
- Low noise: 12 nV/√Hz
- Low power: I_{DD} = 10 µA max
- 0.5 µs settling time
- Built-in R_{FB} facilitates current-to-voltage conversion
- Built-in 4-quadrant resistors allow 0 V to −10 V, 0 V to +10 V, or ±10 V outputs
- 2 mA full-scale current ± 20%, with V_{REF} = 10 V
- Extended automotive operating temperature range −40°C to +125°C
- Selectable zero-scale/midscale power-on presets
- Compact 38-lead TSSOP package

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration
- Digital waveform generation

FUNCTIONAL BLOCK DIAGRAM

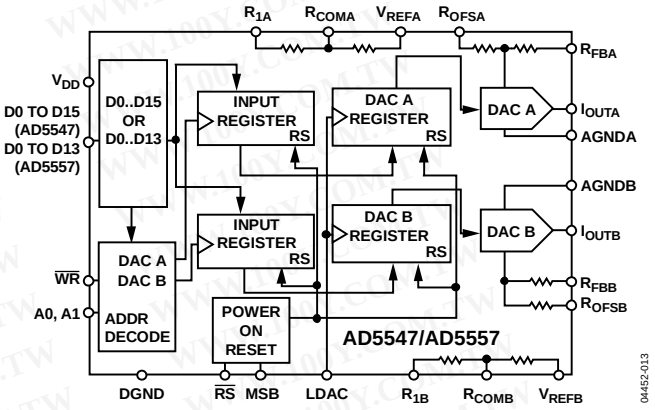

Figure 1.

GENERAL DESCRIPTION

The AD5547/AD5557 are dual precision, 16-/14-bit, multiplying, low power, current-output, parallel input, digital-to-analog converters (DACs). They are designed to operate from single +5 V supply with ±10 V multiplying references for 4-quadrant outputs with 6.8 MHz bandwidth.

The built-in, 4-quadrant resistors facilitate resistance matching and temperature tracking, which minimize the number of components needed for multiquadrant applications. In addition, the feedback resistor (R_{FB}) simplifies the I-to-V conversion with an external buffer.

The AD5547/AD5557 are available in a compact, 38-lead TSSOP package and operate at the extended automotive temperature range of −40°C to +125°C.

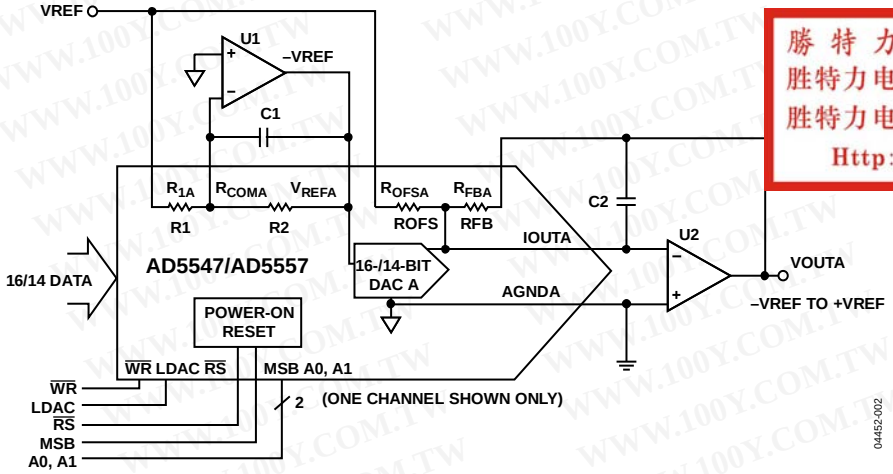

Figure 2. 16-/14-Bit 4-Quadrant Multiplying DAC with Minimum of External Components (Only One Channel Is Shown)

Rev. B

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Added Reference Selection Section, Amplifier Selection Section, Table 10, and Table 11; Renumbered Sequentially ... 18
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9/09—Rev. 0 to Rev. A

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1/04—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = −10 V to +10 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	AD5547, 1 LSB = $V_{REF}/2^{16}$ = 153 µV at V_{REF} = 10 V		16		Bits
		AD5557, 1 LSB = $V_{REF}/2^{14}$ = 610 µV at V_{REF} = 10 V		14		Bits
Relative Accuracy	INL	Grade: AD5557C			±1	LSB
		Grade: AD5547B			±2	LSB
		Grade: AD5547C			±1	LSB
Differential Nonlinearity	DNL	Monotonic			±1	LSB
Output Leakage Current	I_{OUT}	Data = zero scale, T_A = 25°C			10	nA
		Data = zero scale, T_A = T_A maximum			20	nA
Full-Scale Gain Error	G_{FSE}	Data = full scale		±1	±4	mV
Bipolar Mode Gain Error	G_E	Data = full scale		±1	±4	mV
Bipolar Mode Zero-Scale Error	G_{ZSE}	Data = full scale		±1	±3	mV
Full-Scale Temperature Coefficient[2]	TCV_{FS}			1		ppm/°C
REFERENCE INPUT						
V_{REF} Range	V_{REF}		−18		+18	V
REF Input Resistance	REF		4	5	6	kΩ
R1 and R2 Resistance	R1 and R2		4	5	6	kΩ
R1-to-R2 Mismatch	Δ(R1 to R2)			±0.5	±1.5	Ω
Feedback and Offset Resistance	R_{FB}, R_{OFS}		8	10	12	kΩ
Input Capacitance[2]	C_{REF}			5		pF
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = full scale		2		mA
Output Capacitance[2]	C_{OUT}	Code dependent		200		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	V
Logic Input High Voltage	V_{IH}	V_{DD} = 5 V	2.4			V
		V_{DD} = 3 V	2.1			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[2]	C_{IL}				10	pF
INTERFACE TIMING[2, 3]		See Figure 3				
Data to $\overline{WR}$ Setup Time	t_{DS}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
Data to $\overline{WR}$ Hold Time	t_{DH}	V_{DD} = 5 V	0			ns
		V_{DD} = 3 V	0			ns
$\overline{WR}$ Pulse Width	$t_{\overline{WR}}$	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
LDAC Pulse Width	t_{LDAC}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
$\overline{RS}$ Pulse Width	t_{RS}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
$\overline{WR}$ to LDAC Delay Time	t_{LWD}	V_{DD} = 5 V	0			ns
		V_{DD} = 3 V	0			ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			10	μA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			0.055	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%			0.003	%/%
AC CHARACTERISTICS[4]						
Output Voltage Settling Time	t_S	To ±0.1% of full scale, data cycles from zero scale to full scale to zero scale		0.5		μs
Reference Multiplying BW	BW	V_{REF} = 100 mV rms, data = full scale		6.8		MHz
DAC Glitch Impulse	Q	V_{REF} = 0 V, midscale – 1 to midscale		–3.5		nV-s
Multiplying Feedthrough Error	V_{OUT}/V_{REF}	V_{REF} = 100 mV rms, f = 10 kHz		–78		dB
Digital Feedthrough	Q_D	$\overline{WR}$ = 1, LDAC toggles at 1 MHz		7		nV-s
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, data = full scale, f = 1 kHz		–104		dB
Output Noise Density	e_N	f = 1 kHz, BW = 1 Hz		12		nV/√Hz
Analog Crosstalk	C_{AT}	Signal input at Channel A and measures the output at Channel B, f = 1 kHz		–95		dB

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP97 I-to-V converter amplifier. The device R_{FB} terminal is tied to the amplifier output. The +IN pin of the OP97 is grounded, and the I_{OUT} of the DAC is tied to the OP97's –IN pin. Typical values represent average readings measured at 25°C.
[2] Guaranteed by design; not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and are timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier except for THD where the AD8065 was used.

Timing Diagram

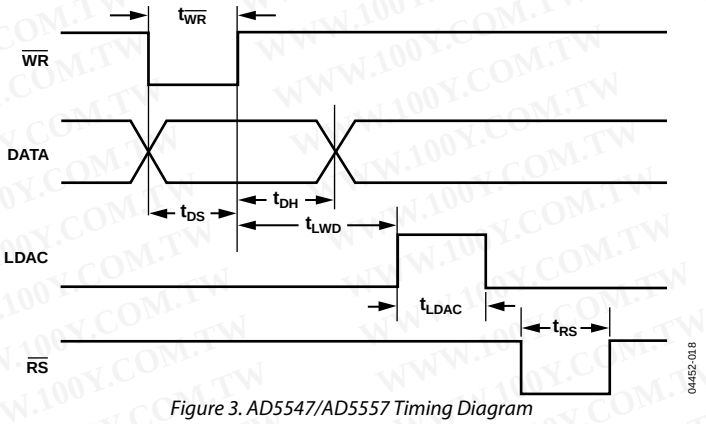

Figure 3. AD5547/AD5557 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +8 V
R_{FB}, R_{OFS}, R1, R_{COM}, and VREF to GND	−18 V to +18 V
Logic Inputs to GND	−0.3 V to +8 V
V(I_{OUT}) to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin except Supplies	±50 mA
Thermal Resistance (θ_{JA})[1]	
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Vapor Phase, 60 s	215°C
Infrared, 15 s	220°C

[1] Package power dissipation = ($T_{J\ MAX}$ − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

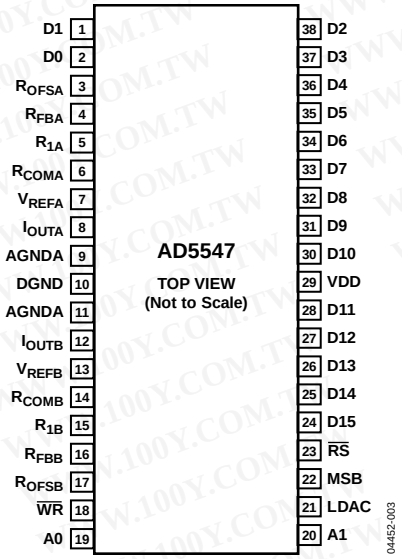

Figure 4. AD5547 Pin Configuration

Table 3. AD5547 Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 24 to 28, 30 to 38	D0 to D15	Digital Input Data Bits D0 to D15. Signal level must be ≤ V_{DD} + 0.3 V.
3	R_{OFSA}	Bipolar Offset Resistor A. Accepts up to ±18 V. In 2-quadrant mode, R_{OFSA} ties to R_{FBA}. In 4-quadrant mode, R_{OFSA} ties to R_{1A} and the external reference.
4	R_{FBA}	Internal Matching Feedback Resistor A. Connects to the external op amp for I-to-V conversion.
5	R_{1A}	4-Quandrant Resistor. In 2-quadrant mode, R_{1A} shorts to the V_{REFA} pin. In 4-quadrant mode, R_{1A} ties to R_{OFSA}. Do not connect when operating in unipolar mode.
6	R_{COMA}	Center Tap Point of the Two 4-Quadrant Resistors, R_{1A} and R_{2A}. In 4-quadrant mode, R_{COMA} ties to the inverting node of the reference amplifier. In 2-quadrant mode, R_{COMA} shorts to the associated V_{REFA} pin. Do not connect if operating in unipolar mode.
7	V_{REFA}	DAC A Reference Input in 2-Quadrant Mode, R2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, V_{REFA} is the reference input with constant input resistance vs. code. In 4-quadrant mode, V_{REFA} is driven by the external reference amplifier.
8	I_{OUTA}	DAC A Current Output. Connects to the inverting terminal of external precision I-to-V op amp for voltage output.
9	AGNDA	DAC A Analog Ground.
10	DGND	Digital Ground.
11	AGNDB	DAC B Analog Ground.
12	I_{OUTB}	DAC B Current Output. Connects to inverting terminal of external precision I-to-V op amp for voltage output.
13	V_{REFB}	DAC B Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code. If configured with an external op amp for 4-quadrant multiplying, V_{REFB} becomes $-V_{REF}$.
14	R_{COMB}	Center Tap Point of the Two 4-Quadrant Resistors, R_{1B} and R_{2B}. In 4-quadrant mode, R_{COMB} ties to the inverting node of the reference amplifier. In 2-quadrant mode, R_{COMB} shorts to the V_{REFB} pin. Do not connect if operating in unipolar mode.
15	R_{1B}	4-Quandrant Resistor. In 2-quadrant mode, R_{1B} shorts to the V_{REFB} pin. In 4-quadrant mode, R_{1B} ties to R_{OFSB}. Do not connect if operating in unipolar mode.
16	R_{FBB}	Internal Matching Feedback Resistor B. Connects to external op amp for I-to-V conversion.
17	R_{OFSB}	Bipolar Offset Resistor B. Accepts up to ±18 V. In 2-quadrant mode, R_{OFSB} ties to R_{FBB}. In 4-quadrant mode, R_{OFSB} ties to R_{1B} and an external reference.
18	$\overline{WR}$	Write Control Digital Input In, Active Low. $\overline{WR}$ transfers shift register data to the DAC register on the rising edge. Signal level must be ≤V_{DD} + 0.3 V.

Pin No.	Mnemonic	Function
19	A0	Address Pin 0. Signal level must be $\leq V_{DD} + 0.3$ V.
20	A1	Address Pin 1. Signal level must be $\leq V_{DD} + 0.3$ V.
21	LDAC	Digital Input Load DAC Control. Signal level must be $\leq V_{DD} + 0.3$ V.
22	MSB	Power-On Reset State. MSB = 0 corresponds to zero-scale reset; MSB = 1 corresponds to midscale reset. The signal level must be $\leq V_{DD} + 0.3$ V.
23	$\overline{RS}$	Active low resets both input and DAC registers. Resets to zero-scale if MSB = 0 and resets to midscale if MSB = 1. Signal level must be $\leq V_{DD} + 0.3$ V.
29	VDD	Positive Power Supply Input. The specified range of operation is 2.7 V to 5.5 V.

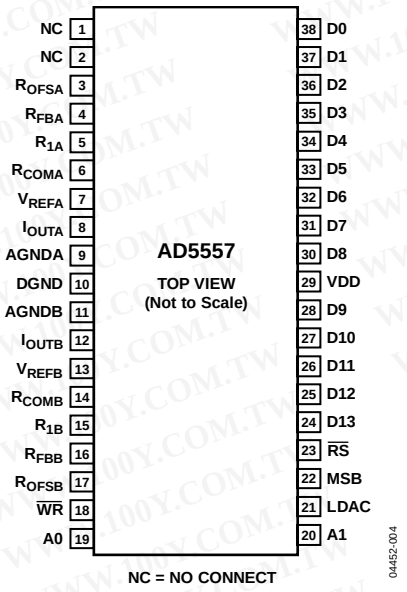

Figure 5. AD5557 Pin Configuration

Table 4. AD5557 Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2	NC	No Connection. Do not connect anything other than the dummy pads to these pins.
3	R_{OFSA}	Bipolar Offset Resistor A. Accepts up to ±18 V. In 2-quadrant mode, R_{OFSA} ties to R_{FBA}. In 4-quadrant mode, R_{OFSA} ties to R_{1A} and the external reference.
4	R_{FBA}	Internal Matching Feedback Resistor A. Connects to the external op amp for I-to-V conversion.
5	R_{1A}	4-Quandrant Resistor. In 2-quadrant mode, R_{1A} shorts to the V_{REFA} pin. In 4-quadrant mode, R_{1A} ties to R_{OFSA}. Do not connect when operating in unipolar mode.
6	R_{COMA}	Center Tap Point of the Two 4-Quadrant Resistors, R_{1A} and R_{2A}. In 4-quadrant mode, R_{COMA} ties to the inverting node of the reference amplifier. In 2-quadrant mode, R_{COMA} shorts to the V_{REFA} pin. Do not connect if operating in unipolar mode.
7	V_{REFA}	DAC A Reference Input in 2-Quadrant Mode, R2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, V_{REFA} is the reference input with constant input resistance vs. code. In 4-quadrant mode, V_{REFA} is driven by the external reference amplifier.
8	I_{OUTA}	DAC A Current Output. Connects to the inverting terminal of external precision I-to-V op amp for voltage output.
9	AGNDA	DAC A Analog Ground.
10	DGND	Digital Ground.
11	AGNDB	DAC B Analog Ground.
12	I_{OUTB}	DAC B Current Output. Connects to inverting terminal of external precision I-to-V op amp for voltage output.
13	V_{REFB}	DAC B Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code. If configured with an external op amp for 4-quadrant multiplying, V_{REFB} becomes $-V_{REF}$.
14	R_{COMB}	Center Tap Point of the Two 4-Quadrant Resistors, R_{1B} and R_{2B}. In 4-quadrant mode, R_{COMB} ties to the inverting node of the reference amplifier. In 2-quadrant mode, R_{COMB} shorts to the V_{REFB} pin. Do not connect if operating in unipolar mode.
15	R_{1B}	4-Quandrant Resistor. In 2-quadrant mode, R_{1B} shorts to the V_{REFB} pin. In 4-quadrant mode, R_{1B} ties to R_{OFSB}. Do not connect if operating in unipolar mode.
16	R_{FBB}	Internal Matching Feedback Resistor B. Connects to external op amp for I-to-V conversion.
17	R_{OFSB}	Bipolar Offset Resistor B. Accepts up to ±18 V. In 2-quadrant mode, R_{OFSB} ties to R_{FBB}. In 4-quadrant mode, R_{OFSB} ties to R_{1B} and an external reference.
18	$\overline{WR}$	Write Control Digital Input In, Active Low. Transfers shift register data to the DAC register on the rising edge. Signal level must be $\leq V_{DD} + 0.3$ V.
19	A0	Address Pin 0. Signal level must be $\leq V_{DD} + 0.3$ V.
20	A1	Address Pin 1. Signal level must be $\leq V_{DD} + 0.3$ V.
21	LDAC	Digital Input Load DAC Control. Signal level must be $\leq V_{DD} + 0.3$ V.
22	MSB	Power-On Reset State. MSB = 0 corresponds to zero-scale reset; MSB = 1 corresponds to midscale reset. The signal level must be $\leq V_{DD} + 0.3$ V.

Pin No.	Mnemonic	Function
23	$\overline{RS}$	Active low resets both input and DAC registers. Resets to zero-scale if MSB = 0 and resets to midscale if MSB = 1. Signal level must be $\leq V_{DD} + 0.3$ V.
24 to 28, 30 to 38	D13 to D0	Digital Input Data Bits D13 to D0. Signal level must be $\leq V_{DD} + 0.3$ V.
29	VDD	Positive Power Supply Input. The specified range of operation is 2.7 V to 5.5 V.

Table 5. Address Decoder Pins

A1	A0	Output Update
0	0	DAC A
0	1	None
1	0	DAC A and DAC B
1	1	DAC B

Table 6. Control Inputs

$\overline{RS}$	$\overline{WR}$	LDAC	Register Operation
0	X	X	Reset the output to 0 with MSB = 0; reset the output to midscale with MSB = 1.
1	0	0	Load the input register with data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC registers are transparent.
1	⊓	⊓	When LDAC and $\overline{WR}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse and are then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

TYPICAL PERFORMANCE CHARACTERISTICS

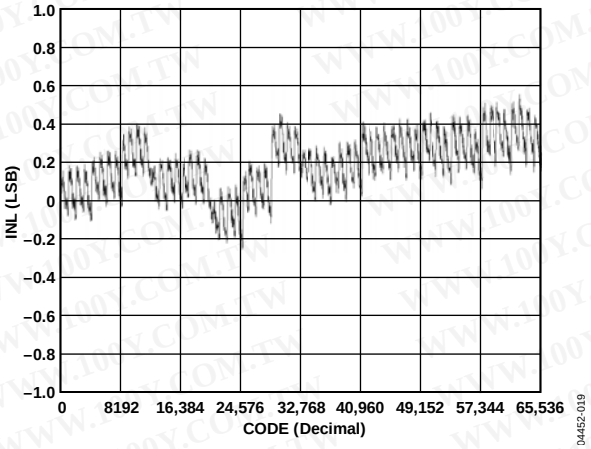

Figure 6. AD5547 Integral Nonlinearity Error

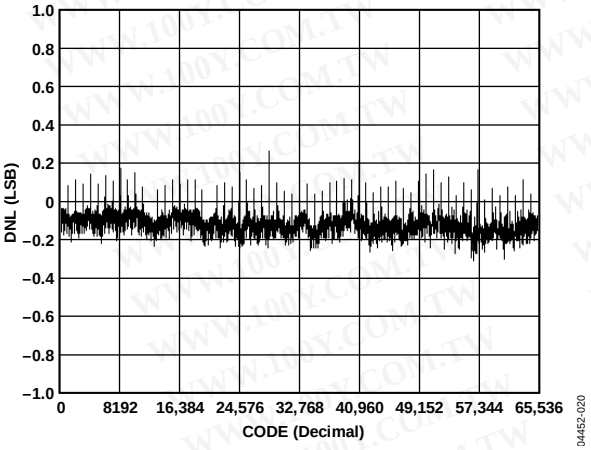

Figure 7. AD5547 Differential Nonlinearity Error

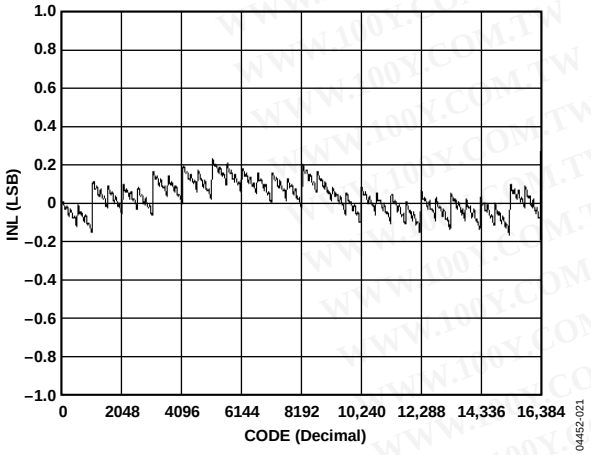

Figure 8. AD5557 Integral Nonlinearity Error

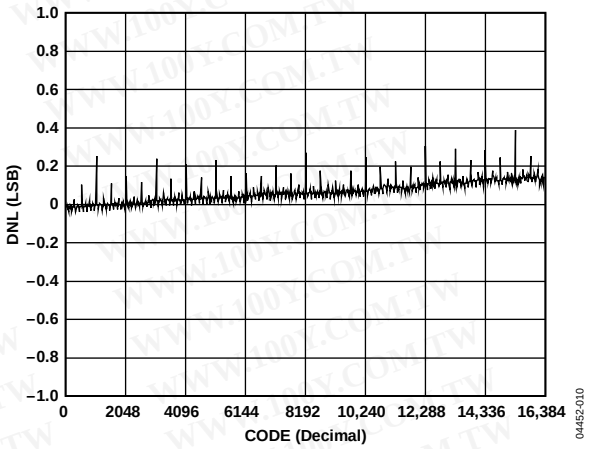

Figure 9. AD5557 Differential Nonlinearity Error

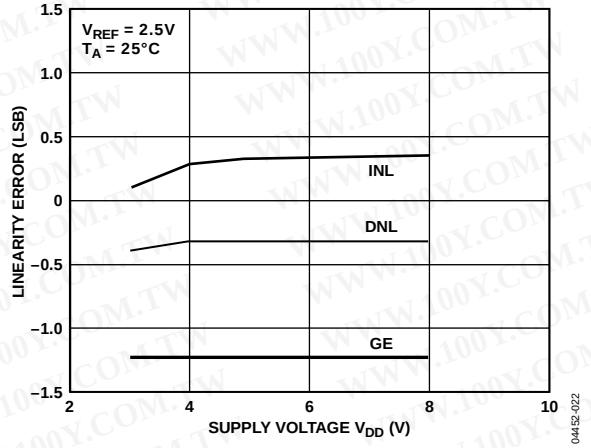

Figure 10. Linearity Error vs. Supply Voltage, V_{DD}

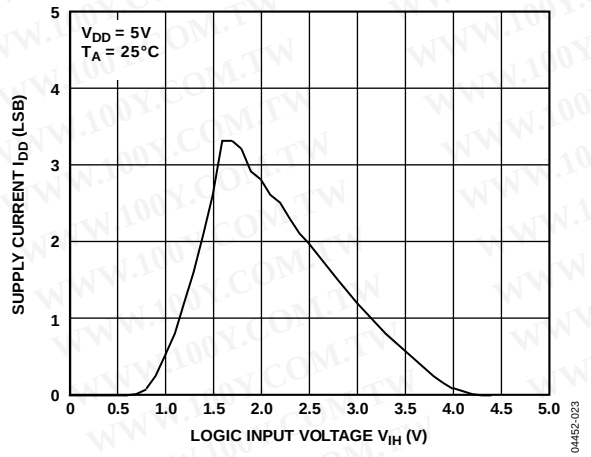

Figure 11. Supply Current vs. Logic Input Voltage

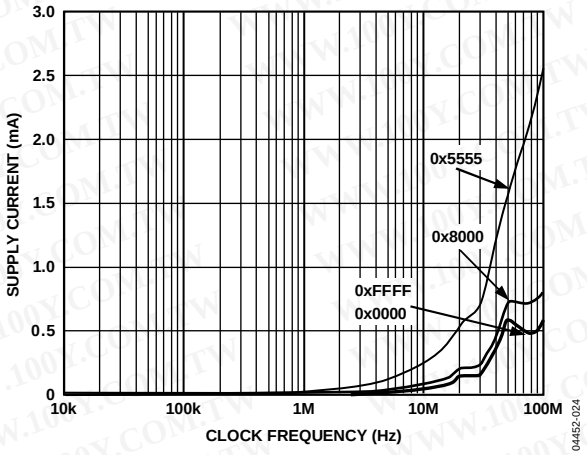

Figure 12. AD5547 Supply Current vs. Clock Frequency

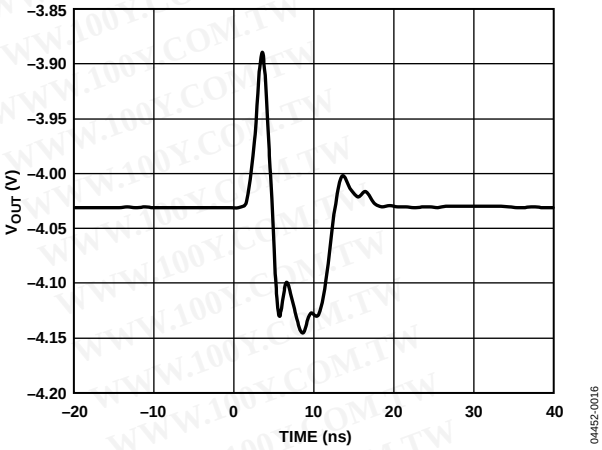

Figure 15. AD5547 Midscale Transition and Digital Feedthrough

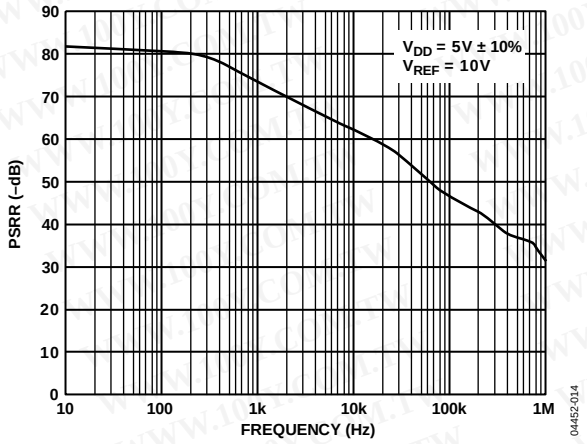

Figure 13. Power Supply Rejection Ratio (PSRR) vs. Frequency

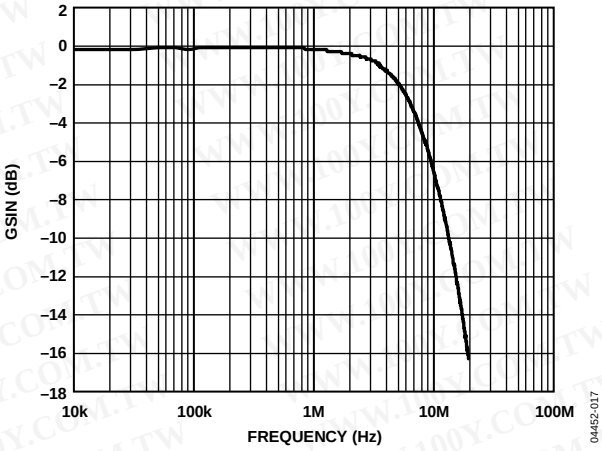

Figure 16. AD5547 Unipolar Reference Multiplying Bandwidth

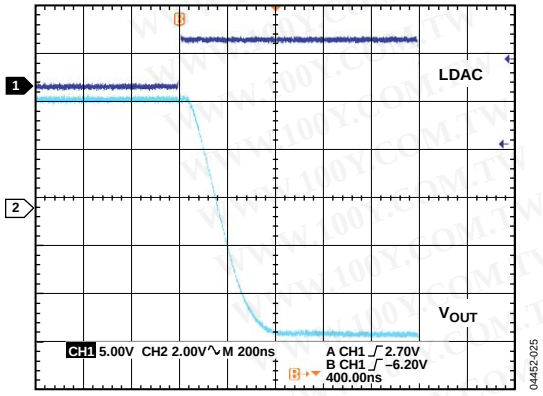

Figure 14. Settling Time from Full Scale to Zero Scale

CIRCUIT OPERATION

DAC SECTION

The AD5547/AD5557 are 16-/14-bit, multiplying, current-output, parallel input DACs. The devices operate from a single 2.7 V to 5.5 V supply and provide both unipolar (0 V to $-V_{REF}$ or 0 V to $+V_{REF}$) and bipolar ($\pm V_{REF}$) output ranges from −18 V to +18 V references. In addition to the precision conversion R_{FB} commonly found in current output DACs, there are three additional precision resistors for 4-quadrant bipolar applications.

The AD5547/AD5557 consist of two groups of precision R-2R ladders, which make up the 12/10 LSBs, respectively. Furthermore, the 4 MSBs are decoded into 15 segments of resistor value 2R. Figure 17 shows the architecture of the 16-bit AD5547. Each of the 16 segments and the R-2R ladder carries an equally weighted current of one-sixteenth of full scale. The feedback resistor R_{FB} and 4-quadrant resistor R_{OFS} have values of 10 kΩ. Each 4-quadrant resistor, R1 and R2, equals 5 kΩ. In 4-quadrant operation, R1, R2, and an external op amp work together to invert the reference voltage and apply it to the V_{REF} input. With R_{OFS} and R_{FB} connected as shown in Figure 2, the output can swing from $-V_{REF}$ to $+V_{REF}$.

The reference voltage inputs exhibit a constant input resistance of 5 kΩ ± 20%. The impedance of I_{OUT}, the DAC output, is code dependent. External amplifier choice should take into account the variation of the AD5547/AD5557 output impedance. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. To maintain good analog performance, it is recommended that the power supply is bypassed with a 0.01 µF to 0.1 µF ceramic or chip capacitor in parallel with a 1 µF tantalum capacitor. Also, to minimize gain error, PCB metal traces between V_{REF} and R_{FB} should match.

Every code change of the DAC corresponds to a step function; gain peaking at each output step may occur if the op amp has limited GBP and excessive parasitic capacitance present at the inverting node of the op amp. A compensation capacitor, therefore, may be needed between the I-to-V op amp inverting and output nodes to smooth the step transition. Such a compensation capacitor should be found empirically, but a 20 pF capacitor is generally adequate for the compensation.

The V_{DD} power is used primarily by the internal logic to drive the DAC switches. Note that the output precision degrades if the operating voltage falls below the specified voltage. Users should also avoid using switching regulators because device power supply rejection degrades at higher frequencies.

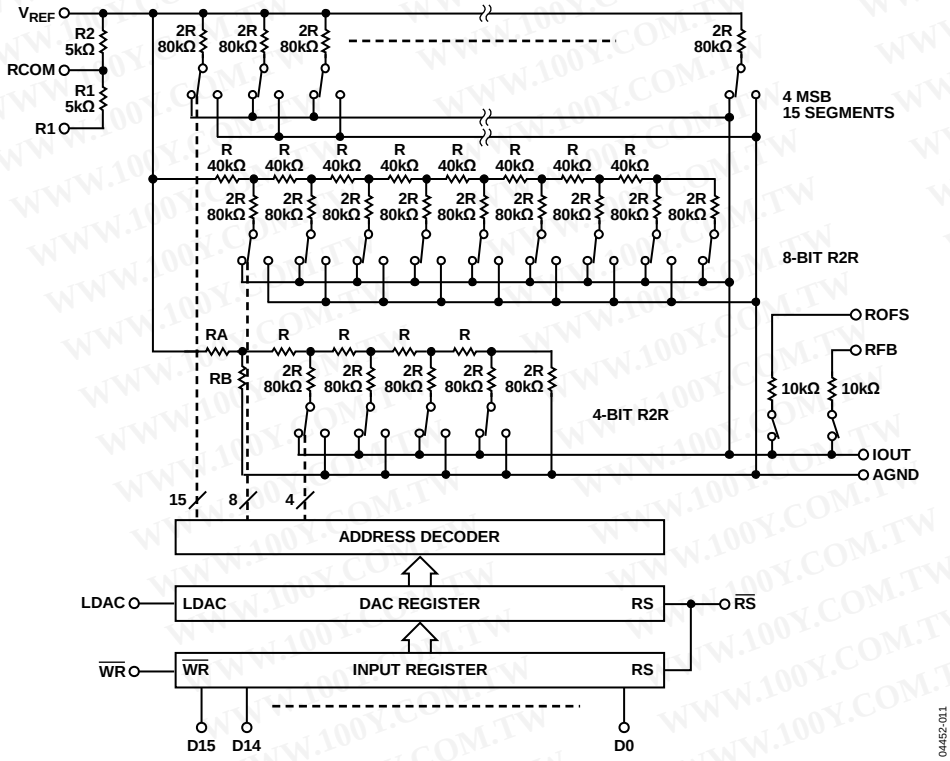

Figure 17. 16-Bit AD5547 Equivalent R-2R DAC Circuit with Digital Section, One Channel Shown

DIGITAL SECTION

The AD5547/AD5557 have 16-/14-bit parallel inputs. The devices are double buffered with 16-/14-bit registers. The double buffered feature allows the simultaneous update of several AD5547s/AD5557s. For the AD5547, the input register is loaded directly from a 16-bit controller bus when $\overline{WR}$ is brought low. The DAC register is updated with data from the input register when LDAC is brought high. Updating the DAC register updates the DAC output with the new data (see Figure 17). To make both registers transparent, tie $\overline{WR}$ low and LDAC high. The asynchronous $\overline{RS}$ pin resets the part to zero scale if MSB = 0 and to midscale if MSB = 1.

ESD Protection Circuits

All logic input pins contain back-biased ESD protection Zeners connected to ground (DGND) and V_{DD}, as shown in Figure 18. As a result, the voltage level of the logic input should not be greater than the supply voltage.

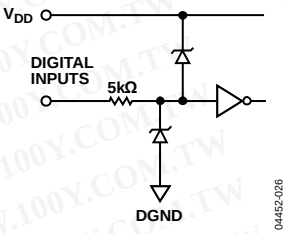

Figure 18. Equivalent ESD Protection Circuits

Amplifier Selection

In addition to offset voltage, the bias current is important in op amp selection for precision current output DACs. A 30 nA input bias current in the op amp contributes to 1 LSB in the full-scale error of the AD5547. The OP1177 and AD8628 op amps are good candidates for the I-to-V conversion.

Reference Selection

The initial accuracy and rated output of the voltage reference determine the full-span adjustment. The initial accuracy of the reference is usually a secondary concern because it can be trimmed. Figure 24 shows an example of a trimming circuit. The zero-scale error can also be minimized by standard op amp nulling techniques.

The voltage reference temperature coefficient (TC) and long-term drift are primary considerations. For example, a 5 V reference with a TC of 5 ppm/°C means the output changes by 25 µV/°C. As a result, a reference operating at 55°C contributes an additional 750 µV full-scale error.

Similarly, the same 5 V reference with a ±50 ppm long-term drift means the output may change by ±250 µV over time. Therefore, it is practical to calibrate a system periodically to maintain its optimum precision.

PCB LAYOUT, POWER SUPPLY BYPASSING, AND GROUND CONNECTIONS

It is a good practice to employ a compact, minimum lead length, PCB layout design. The leads to the input should be as short as possible to minimize IR drop and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error.

It is also essential to bypass the power supply with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supply in parallel with the ceramic capacitor to minimize transient disturbance and filter out low frequency ripple.

To minimize the digital ground bounce, the AD5547/AD5557 DGND terminal should be joined with the AGND terminal at a single point. Figure 19 illustrates the basic supply bypassing configuration and AGND/DGND connection for the AD5547/AD5557.

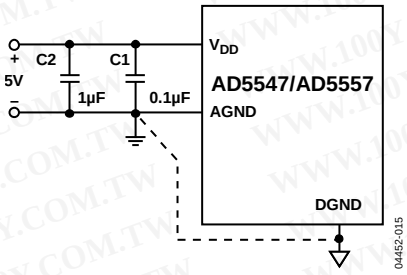

Figure 19. Power Supply Bypassing

APPLICATIONS INFORMATION

UNIPOLAR MODE

2-Quadrant Multiplying Mode, V_{OUT} = 0 V to $-V_{REF}$

The AD5547/AD5557 DAC architecture uses a current-steering R-2R ladder design that requires an external reference and op amp to convert the unipolar mode of the output voltage to

$$V_{OUT} = -V_{REF} \times D/65{,}536 \text{ (AD5547)} \quad (1)$$

$$V_{OUT} = -V_{REF} \times D/16{,}384 \text{ (AD5557)} \quad (2)$$

where D is the decimal equivalent of the input code.

In this case, the output voltage polarity is opposite the V_{REF} polarity (see Figure 20). Table 7 shows the negative output vs. code for the AD5547.

Table 7. AD5547 Unipolar Mode Negative Output vs. Code

D in Binary	V_{OUT} (V)
1111 1111 1111 1111	$-V_{REF}$ (65,535/65,536)
1000 0000 0000 0000	$-V_{REF}/2$
0000 0000 0000 0001	$-V_{REF}$ (1/65,536)
0000 0000 0000 0000	0

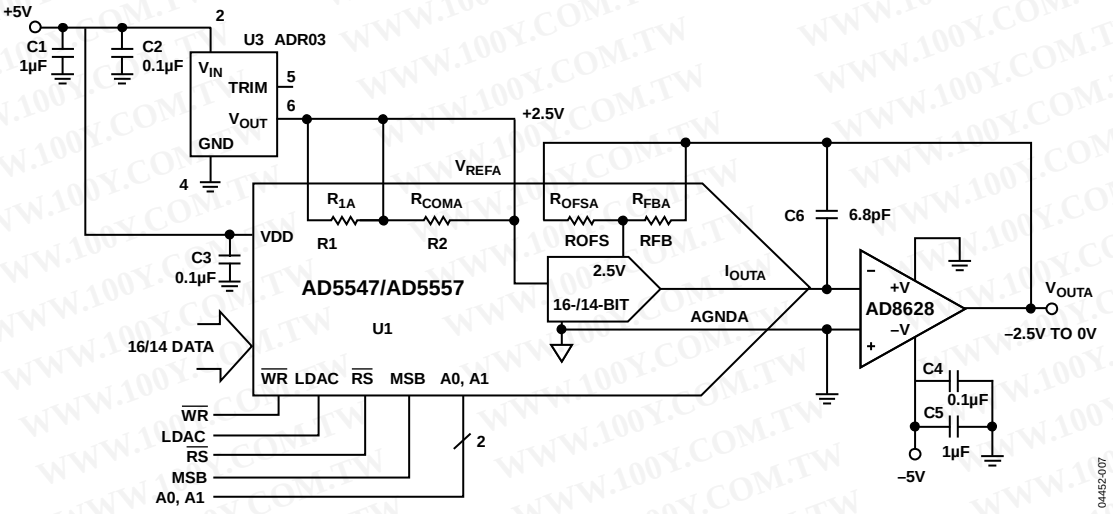

Figure 20. Unipolar 2-Quadrant Multiplying Mode, V_{OUT} = 0 to $-V_{REF}$

2-Quadrant Multiplying Mode, V_{OUT} = 0 V to +V_{REF}

The AD5547/AD5557 are designed to operate with either positive or negative reference voltages. As a result, a positive output can be achieved with an additional op amp, (see Figure 21); the output becomes

$$V_{OUT} = +V_{REF} \times D/65{,}536 \text{ (AD5547)} \quad (3)$$

$$V_{OUT} = +V_{REF} \times D/16{,}384 \text{ (AD5557)} \quad (4)$$

Table 8 shows the positive output vs. code for the AD5547.

Table 8. AD5547 Unipolar Mode Positive Output vs. Code

D in Binary	V_{OUT} (V)
1111 1111 1111 1111	+V_{REF}(65,535/65,536)
1000 0000 0000 0000	+V_{REF}/2
0000 0000 0000 0001	+V_{REF}(1/65,536)
0000 0000 0000 0000	0

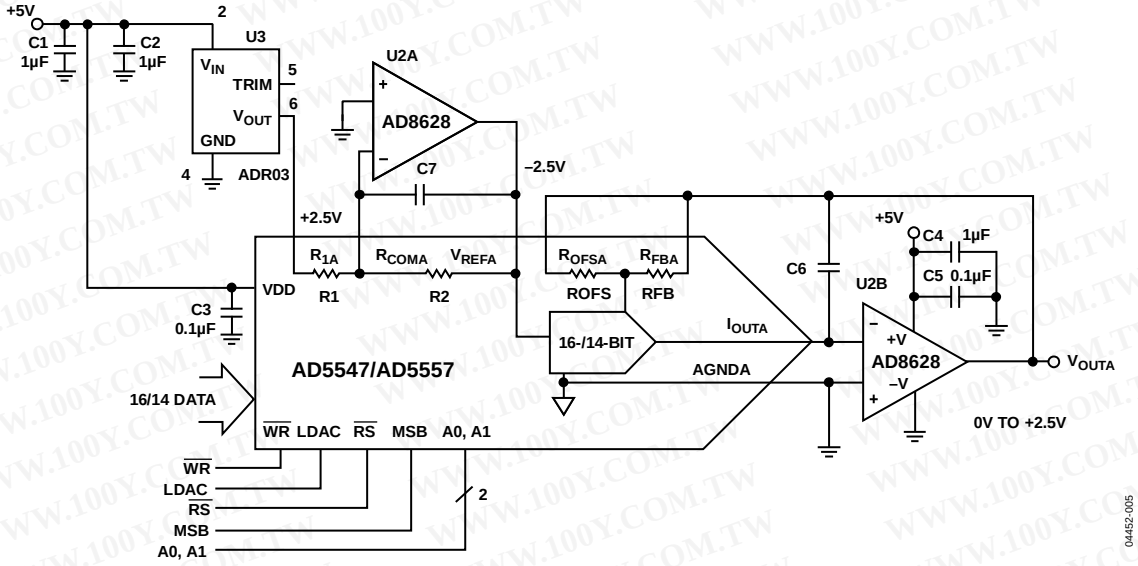

Figure 21. Unipolar 2-Quadrant Multiplying Mode, V_{OUT} = 0 to +V_{REF}

BIPOLAR MODE

4-Quadrant Multiplying Mode, V_{OUT} = –V_{REF} to +V_{REF}

The AD5547/AD5557 contain on-chip all the 4-quadrant resistors necessary for precision bipolar multiplying operation. Such a feature minimizes the number of exponent components to only a voltage reference, dual op amp, and compensation capacitor (see Figure 22). For example, with a +10 V reference, the circuit yields a precision, bipolar –10 V to +10 V output.

$$V_{OUT} = (D/32768 - 1) \times V_{REF} \text{ (AD5547)} \quad (5)$$

$$V_{OUT} = (D/16384 - 1) \times V_{REF} \text{ (AD5557)} \quad (6)$$

Table 9 shows some of the results for the 16-bit AD5547.

Table 9. AD5547 Output vs. Code

D in Binary	V_{OUT}
1111 1111 1111 1111	+V_{REF} (32,767/32,768)
1000 0000 0000 0001	+V_{REF} (1/32,768)
1000 0000 0000 0000	0
0111 1111 1111 1111	–V_{REF} (1/32,768)
0000 0000 0000 0000	–V_{REF}

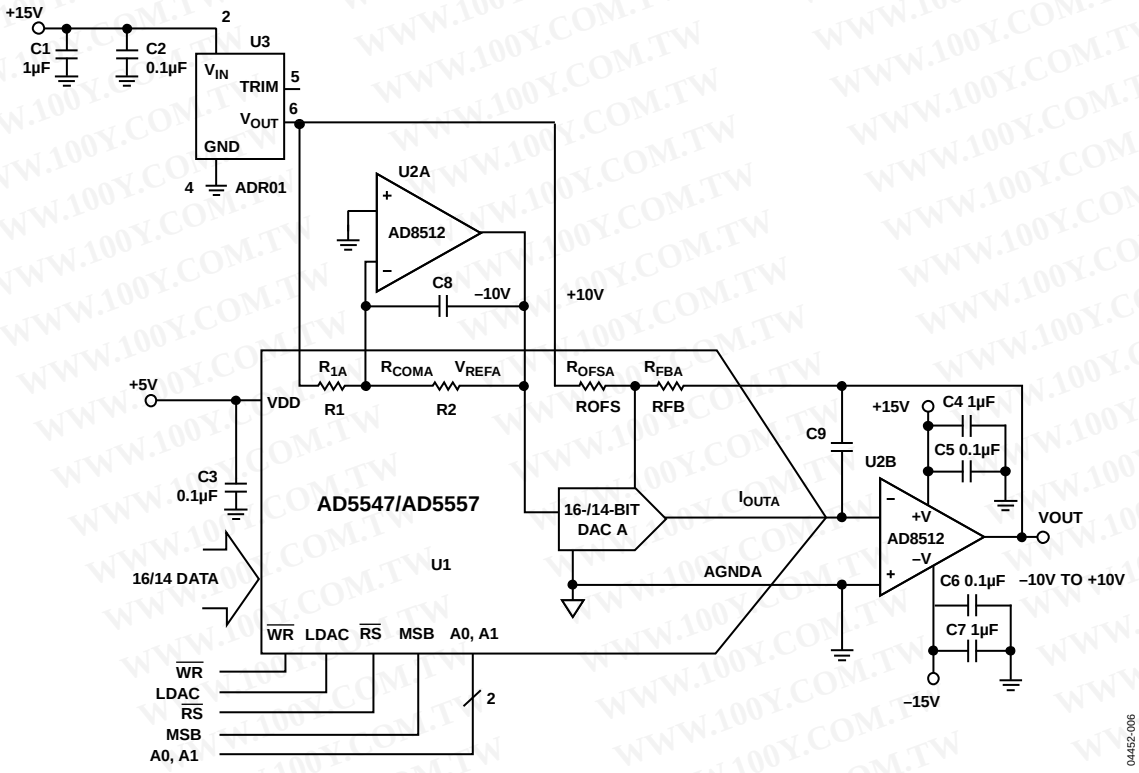

Figure 22. 4-Quadrant Multiplying Mode, V_{OUT} = –V_{REF} to +V_{REF}

AC Reference Signal Attenuator

Besides handling the digital waveform decoded from the parallel input data, the AD5547/AD5557 can also handle low frequency ac reference signals for signal attenuation, channel equalization, and waveform generation applications. The maximum signal range can be up to ±18 V (see Figure 23).

System Calibration

The initial accuracy of the system can be adjusted by trimming the voltage reference ADR0x with a digital potentiometer (see Figure 24). The AD5170 provides a one-time programmable (OTP), 8-bit adjustment that is ideal and reliable for such calibration. Analog Devices, Inc., OTP digital potentiometer comes with programmable software that simplifies factory calibration.

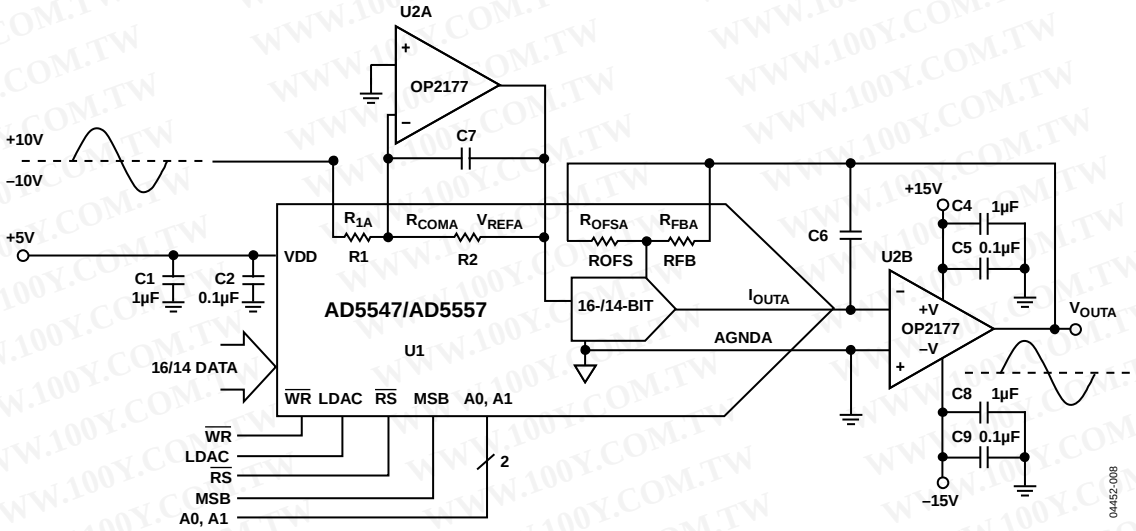

Figure 23. Signal Attenuator with AC Reference

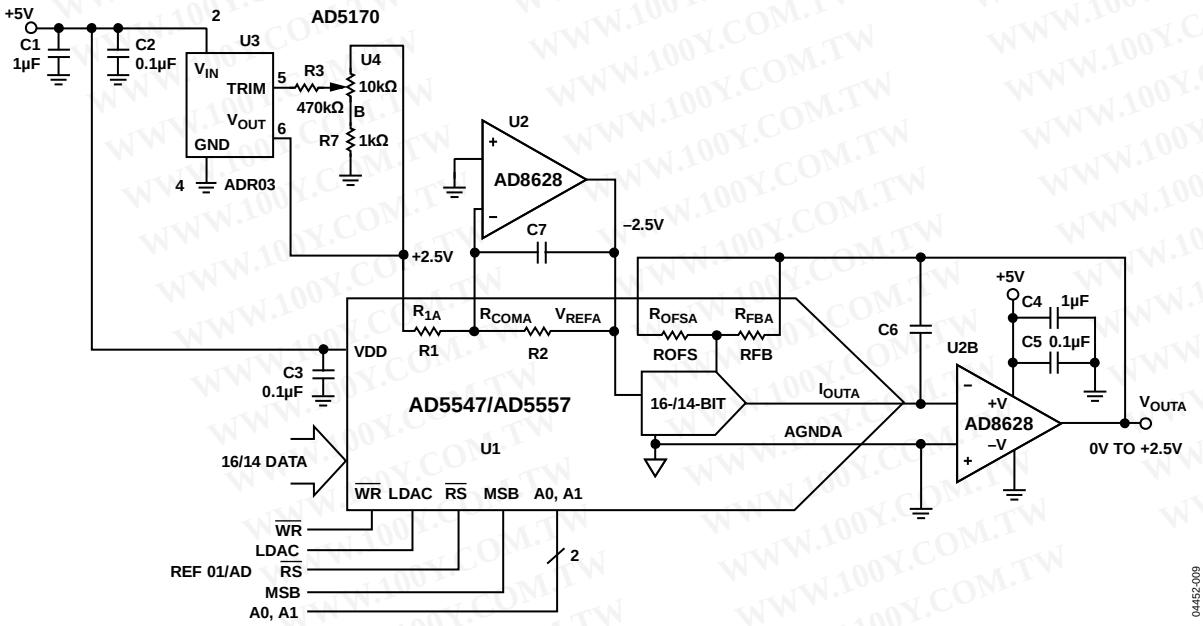

Figure 24. Full-Span Calibration

REFERENCE SELECTION

When selecting a reference for use with the AD55xx series of current output DACs, pay attention to the output voltage, temperature coefficient specification of the reference. Choosing a precision reference with a low output temperature coefficient minimizes error sources. Table 10 lists some of the references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output because of the bias current flowing in the feedback resistor, R_{FB}.

Common-mode rejection of the op amp is important in voltage-switching circuits because it produces a code-dependent error at the voltage output of the circuit.

Provided that the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Analog Devices offers a wide range of amplifiers for both precision dc and ac applications, as listed in Table 11 and Table 12.

Table 10. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Maximum Temperature Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package(s)
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-5, SC70-5
ADR02	5.0	0.06	3	1	10	SOIC-8
ADR02	5.0	0.06	9	1	10	TSOT-5, SC70-5
ADR03	2.5	0.1	3	1	6	SOIC-8
ADR03	2.5	0.1	9	1	6	TSOT-5, SC70-5
ADR06	3.0	0.1	3	1	10	SOIC-8
ADR06	3.0	0.1	9	1	10	TSOT-5, SC70-5
ADR420	2.048	0.05	3	0.5	1.75	SOIC-8, MSOP-8
ADR421	2.50	0.04	3	0.5	1.75	SOIC-8, MSOP-8
ADR423	3.00	0.04	3	0.5	2	SOIC-8, MSOP-8
ADR425	5.00	0.04	3	0.5	3.4	SOIC-8, MSOP-8
ADR431	2.500	0.04	3	0.8	3.5	SOIC-8, MSOP-8
ADR435	5.000	0.04	3	0.8	8	SOIC-8, MSOP-8
ADR391	2.5	0.16	9	0.12	5	TSOT-5
ADR395	5.0	0.10	9	0.12	8	TSOT-5

Table 11. Suitable Analog Devices Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} Maximum (µV)	I_B Maximum (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package(s)
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8 , PDIP-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP-8, SOIC-8
AD8675	±5 to ±18	75	2	0.1	2300	MSOP-8, SOIC-8
AD8671	±5 to ±15	75	12	0.077	3000	MSOP-8, SOIC-8
ADA4004-1	±5 to ±15	125	90	0.1	2000	SOIC-8, SOT-23-5
AD8603	1.8 to 5	50	0.001	2.3	40	TSOT-5
AD8607	1.8 to 5	50	0.001	2.3	40	MSOP-8, SOIC-8
AD8605	2.7 to 5	65	0.001	2.3	1000	WLCSP-5, SOT-23-5
AD8615	2.7 to 5	65	0.001	2.4	2000	TSOT-5
AD8616	2.7 to 5	65	0.001	2.4	2000	MSOP-8, SOIC-8

Table 12. Suitable Analog Devices High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package(s)
AD8065	5 to 24	145	180	1500	0.006	SOIC-8, SOT-23-5
AD8066	5 to 24	145	180	1500	0.006	SOIC-8, MSOP-8
AD8021	5 to 24	490	120	1000	10,500	SOIC-8, MSOP-8
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
ADA4899	5 to 12	600	310	35	100	LFCSP-8, SOIC-8
AD8057	3 to 12	325	1000	5000	500	SOT-23-5, SOIC-8
AD8058	3 to 12	325	850	5000	500	SOIC-8, MSOP-8
AD8061	2.7 to 8	320	650	6000	350	SOT-23-5, SOIC-8
AD8062	2.7 to 8	320	650	6000	350	SOIC-8, MSOP-8
AD9631	±3 to ±6	320	1300	10,000	7000	SOIC-8, PDIP-8

Table 13 lists the latest DACS available from Analog Devices.

Table 13. ADI Current Output DACs

Model	Bits	Outputs	Interface	Package	Comments
AD5425	8	1	SPI, 8-Bit Load	MSOP-10	Fast 8-bit load; see also AD5426
AD5426	8	1	SPI	MSOP-10	See also AD5425 fast load
AD5450	8	1	SPI	TSOT-8	See also AD5425 fast load
AD5424	8	1	Parallel	TSSOP-16	
AD5429	8	2	SPI	TSSOP-16	
AD5428	8	2	Parallel	TSSOP-20	
AD5432	10	1	SPI	MSOP-10	
AD5451	10	1	SPI	TSOT-8	
AD5433	10	1	Parallel	TSSOP-20	
AD5439	10	2	SPI	TSSOP-16	
AD5440	10	2	Parallel	TSSOP-24	
AD5443	12	1	SPI	MSOP-10	See also AD5452 and AD5444
AD5452	12	1	SPI	TSOT-8	Higher accuracy version of AD5443; see also AD5444
AD5445	12	1	Parallel	TSSOP-20	
AD5444	12	1	SPI	MSOP-10	Higher accuracy version of AD5443; see also AD5452
AD5449	12	2	SPI	TSSOP-16	
AD5415	12	2	SPI	TSSOP-24	Uncommitted resistors
AD5447	12	2	Parallel	TSSOP-24	
AD5405	12	2	Parallel	LFCSP-40	Uncommitted resistors
AD5453	14	1	SPI	TSOT-8	
AD5553	14	1	SPI	MSOP-8	
AD5556	14	1	Parallel	TSSOP-28	
AD5446	14	1	SPI	MSOP-10	MSOP version of AD5453; compatible with AD5443, AD5432, and AD5426
AD5555	14	2	SPI	TSSOP-16	
AD5557	14	2	Parallel	TSSOP-38	
AD5543	16	1	SPI	MSOP-8	
AD5546	16	1	Parallel	TSSOP-28	
AD5545	16	2	SPI	TSSOP-16	
AD5547	16	2	Parallel	TSSOP-38	

OUTLINE DIMENSIONS

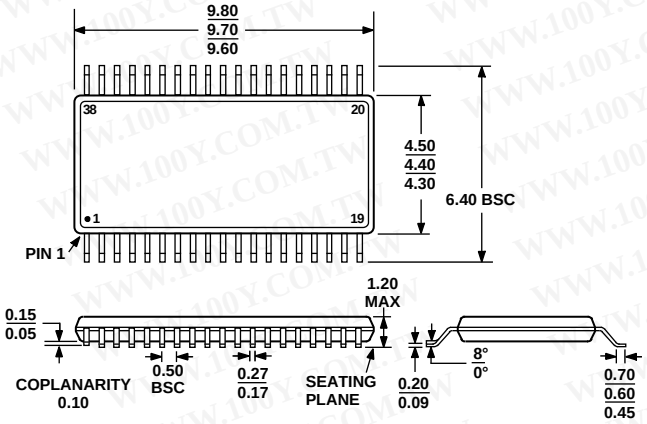

Figure 25. 38-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-38)
Dimension s shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	DNL (LSB)	INL (LSB)	Temperature Range	Package Description	Package Option	Ordering Quantity
AD5547BRU	16	±1	±2	−40°C to +125°C	38-Lead TSSOP	RU-38	50
AD5547BRU-REEL7	16	±1	±2	−40°C to +125°C	38-Lead TSSOP	RU-38	1,000
AD5547BRUZ	16	±1	±2	−40°C to +125°C	38-Lead TSSOP	RU-38	50
AD5547CRUZ	16	±1	±1	−40°C to +125°C	38-Lead TSSOP	RU-38	50
AD5547CRUZ-REEL7	16	±1	±1	−40°C to +125°C	38-Lead TSSOP	RU-38	1,000
AD5557CRU	14	±1	±1	−40°C to +125°C	38-Lead TSSOP	RU-38	50
AD5557CRU-REEL7	14	±1	±1	−40°C to +125°C	38-Lead TSSOP	RU-38	1,000
AD5557CRUZ	14	±1	±1	−40°C to +125°C	38-Lead TSSOP	RU-38	50

[1] Z = RoHS Compliant Part.