

FEATURES

- 40 MHz correlated double sampler (CDS)
- Fixed 3.5 dB CDS gain
- Low noise optical black clamp circuit
- 3 V single-supply operation
- 14-lead TSSOP package

APPLICATIONS

- Digital still cameras
- Digital video camcorders
- CCTV cameras
- PC cameras
- Portable CCD imaging devices

FUNCTIONAL BLOCK DIAGRAM

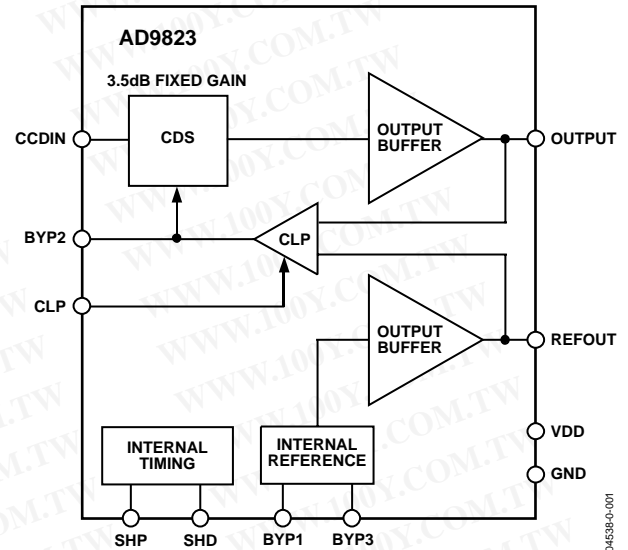


Figure 1. Functional Block Diagram

PRODUCT DESCRIPTION

The AD9823 is a correlated double sampler for digital camera applications. It features a 40 MHz CDS amplifier with 3.5 dB of fixed gain, an internal voltage reference supply, and timing control for the SHP and SHD sampling clocks. Output buffers are also included, providing drive strength for PCB traces and direct connection to an image signal processor such as the AD9821.

The AD9823 is ideal for applications that need to place the CDS and VGA/ADC circuits on separate PC boards. The “pseudo differential” outputs of the AD9823 provide good signal integrity when interfaced with the differential input AD9821.

The AD9823 operates from a single 3 V power supply, typically dissipates 50 mW, and is packaged in a 14-lead TSSOP package.

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Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

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SPECIFICATIONS

GENERAL SPECIFICATIONS

Table 1.

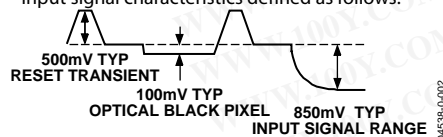
| Parameter | Min | Typ | Max | Unit |
|--|-----|-----|------|------|
| Temperature Range | | | | |
| Operating | -25 | | +85 | °C |
| Storage | -65 | | +150 | °C |
| Power Supply Voltage | 2.7 | | 3.6 | V |
| Power Consumption: $f_{SAMP} = 40$ MHz, $V_{DD} = 3.0$ V | | 50 | | mW |
| Maximum Clock Rate | 40 | | | MHz |
| Minimum Clock Rate | | 5 | | MHz |

ANALOG SPECIFICATIONS

Table 2. T_{MIN} to T_{MAX} , $V_{DD} = 3.0$ V, $f_{SAMP} = 40$ MHz, unless otherwise noted.

| Parameter | Min | Typ | Max | Unit | Notes |
|--|-----|-----|-----|--------|---|
| Analog Input (CCDIN) | | | | | |
| Max Input Range Before Saturation ¹ | | 850 | | mV p-p | |
| Allowable CCD Reset Transient ¹ | | 500 | | mV | |
| Max CCD Black Pixel Amplitude ¹ | | 100 | | mV | |
| Gain | 2.5 | 3.5 | 4.5 | dB | |
| Nonlinearity, 500 mV Input | | 1.0 | | % | Max deviation from ideal straight line |
| Input Referred Noise | | 100 | | μV rms | Output noise divided by 3.5 dB gain |
| Clamp Time Constant | | 190 | | μsec | 0.1 μF BYP2 capacitor (proportional to capacitor value) |
| Analog Outputs | | | | | |
| Typical Data Out Signal Range | 0.5 | | 1.5 | V | 0.5 V corresponds to black level |
| REFOUT Voltage Level | | 0.5 | | V | Fixed dc reference for signal output |

¹ Input signal characteristics defined as follows:



All specifications subject to change without notice.

DIGITAL SPECIFICATIONS

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|----------|-----|-----|-----|------|
| Logic Inputs (SHP, SHD, CLP) | | | | | |
| High Level Input Voltage | V_{IH} | 2.1 | | | V |
| Low Level Input Voltage | V_{IL} | | | 0.6 | V |
| High Level Input Current | I_{IH} | | 10 | | μA |
| Low Level Input Current | I_{IL} | | 10 | | μA |
| Input Capacitance | C_{IN} | | 10 | | pF |

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TIMING SPECIFICATIONS

Table 4. T_{MIN} to T_{MAX} , $VDD = 3.0 V$, $f_{SAMP} = 40 MHz$, unless otherwise noted.

| Parameter (See Figure 3) | Symbol | Min | Typ | Max | Unit |
|--|-----------|------|------|-----|--------|
| Sample Clocks | | | | | |
| SHP, SHD Clock Period | t_{CP} | 25 | | | ns |
| SHP Pulse Width | t_{SHP} | 5 | 6.25 | | ns |
| SHD Pulse Width | t_{SHD} | 5 | 6.25 | | ns |
| CLP Pulse Width ¹ | t_{COB} | 4 | 10 | | pixels |
| SHP Rising Edge to SHD Rising Edge | t_{S1} | 12.0 | 12.5 | | ns |
| SHD Rising Edge to SHP Rising Edge | t_{S2} | 12.0 | 12.5 | | ns |
| Internal Clock Delay | t_{ID} | | 3.0 | | ns |
| Recommended Data CLK Timing (for AD9821) | t_{REC} | | 4.5 | | ns |

¹ Minimum CLP pulse width is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance. Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | With Respect To | Min | Max | Unit |
|---------------------------|-----------------|------|-----------|------|
| VDD | GND | -0.3 | 3.9 | V |
| SHP, SHD | GND | -0.3 | VDD + 0.3 | V |
| BYP1, BYP2, BYP3 | GND | -0.3 | VDD + 0.3 | V |
| CCDIN | GND | -0.3 | VDD + 0.3 | V |
| DATAOUT, REFOUT | GND | -0.3 | VDD + 0.3 | V |
| CLP | GND | -0.3 | VDD + 0.3 | V |
| Junction Temperature | | | 150 | °C |
| Lead Temperature (10 sec) | | | 350 | °C |

THERMAL CHARACTERISTICS

Thermal Resistance

14-Pin, TSSOP Package

$$\theta_{JA} = 89.2^{\circ}\text{C}/\text{W}$$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

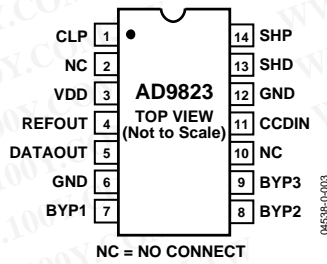


Figure 2. Pin Configurations

Table 6. Pin Function Descriptions

| Pin Number | Name | Type ¹ | Description |
|------------|---------|-------------------|---|
| 1 | CLP | DI | Input Clamp Clock Input (active low, not latched internally). |
| 2 | NC | NC | No connection should be connected to GND or VDD. |
| 3 | VDD | P | Analog Supply. |
| 4 | REFOUT | AO | Output Reference Level. |
| 5 | DATAOUT | AO | Output Data Signal. |
| 6 | GND | P | Analog Ground. |
| 7 | BYP1 | AO | Internal Bias Level Decoupling. |
| 8 | BYP2 | AO | Internal Bias Level Decoupling. |
| 9 | BYP3 | AO | Internal Bias Level Decoupling. |
| 10 | NC | NC | No connection should be connected to GND or VDD. |
| 11 | CCDIN | AI | CCD Input. |
| 12 | GND | P | Analog Ground. |
| 13 | SHD | DI | CDS Sampling Clock Input (For CCD Data Level). |
| 14 | SHP | DI | CDS Sampling Clock Input (For CCD Ref Level). |

¹AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power, NC = No Connect.

SHP AND SHD TIMING

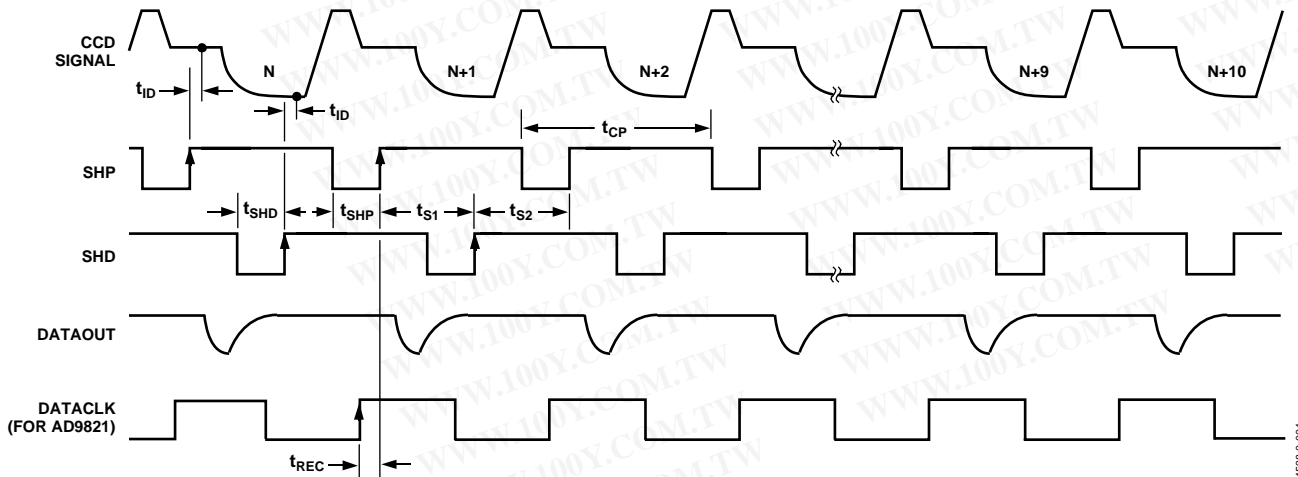


Figure 3. SHP and SHD Timing

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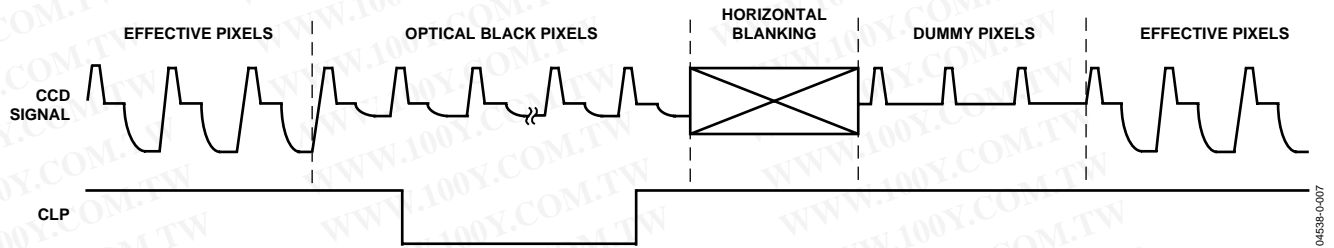


Figure 4. CLP Timing

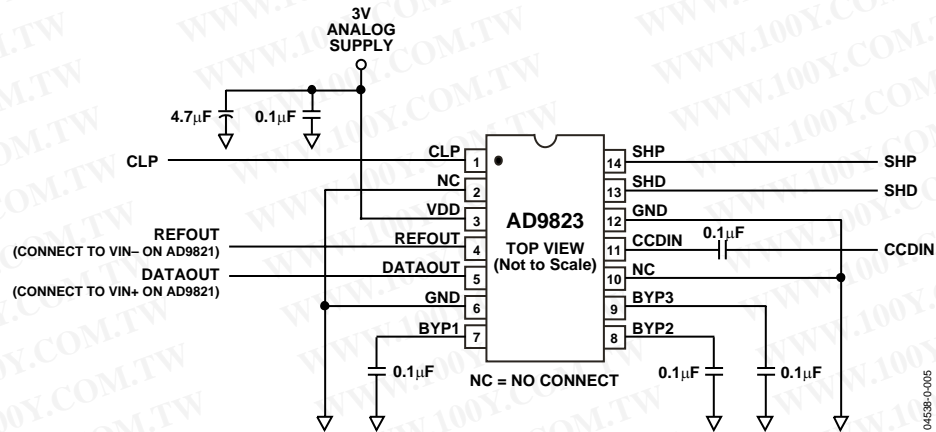


Figure 5. AD9823 Circuit Configuration

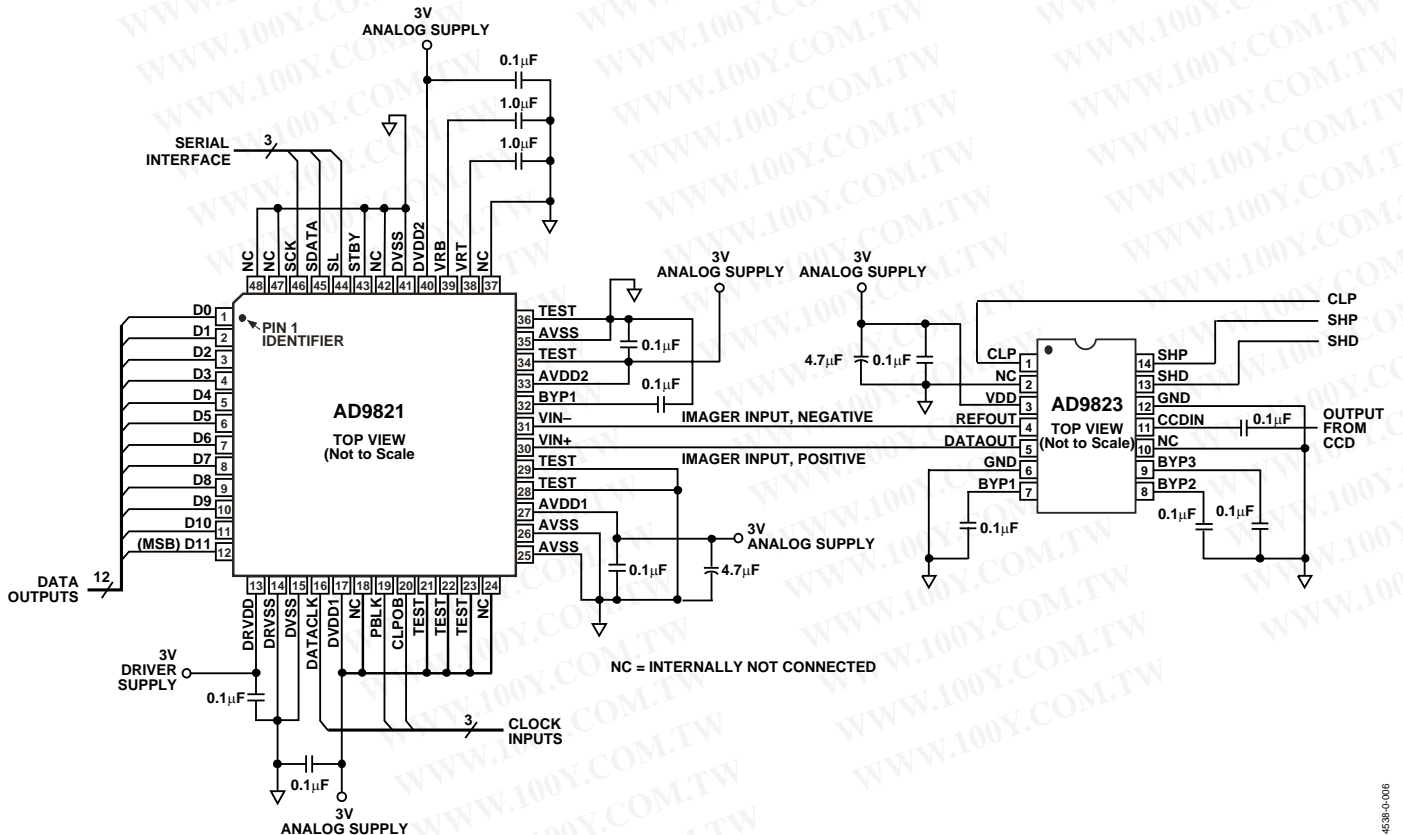


Figure 6. Circuit Configuration with the AD9821 12-Bit Image Signal Processor

AD9823

OUTLINE DIMENSIONS

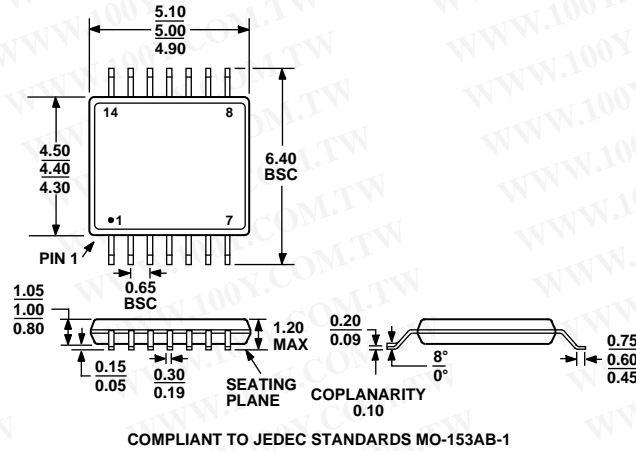


Figure 7. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------------------|-------------------|---------------------|----------------|
| AD9823BRUZ ¹ | -25°C to +85°C | TSSOP | RU-14 |

¹Z = Pb-free part.

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