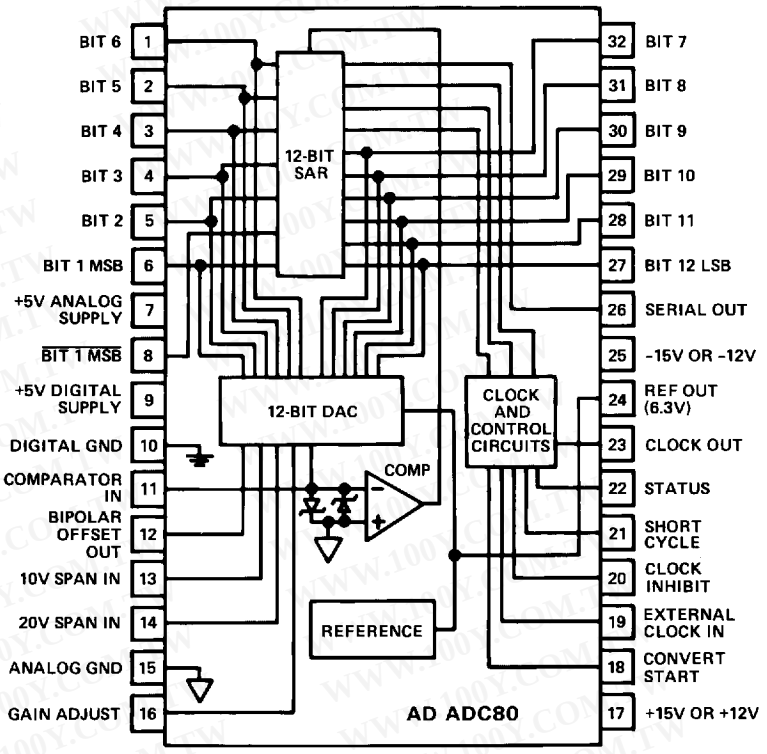
12-Bit Successive Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

- True 12-Bit Operation: Max Nonlinearity ±0.012%
- Low Gain T.C.: ±30ppm/°C max
- Low Power: 800mW
- Fast Conversion Time: 25μs
- Precision 6.3V Reference for External Application
- Short-Cycle Capability
- Serial or Parallel Data Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count—High Reliability
- Industry Standard Pinout
- "Z" Models for ±12V Supplies

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at +25°C of ±0.012%, max gain T.C. of 30ppm/°C, typical power dissipation of 800mW and max conversion time of 25μs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of -25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5, ±5.0, ±10, 0 to +5 or 0 to +10 volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the -25°C to +85°C temperature range and both are available in a 32-pin ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
6. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

REV. A

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AD ADC80—SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise specified)

MODEL	AD ADC80-12	AD ADC80-10
RESOLUTION	12 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	
Unipolar	0V to +5V, 0V to +10V	
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ	*
0V to +10V, ±5V	5kΩ	*
±10V	10kΩ	*
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100ns Wide (min) ("0" to "1" Initiates Conversion)	
Logic Loading	1TTL Load	
External Clock	1TTL Load	
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1% of FSR[3]	*
Offset Error[2]		
Unipolar	±0.05% of FSR	*
Bipolar	±0.1% of FSR	*
Linearity Error (max)[4]	±0.012% of FSR	±0.048% of FSR
Inherent Quantization Error	±1/2LSB	*
Differential Linearity Error	±1/2LSB	*
No Missing Codes Temperature Range	−25°C to +85°C	*
Power Supply Sensitivity		
±15V	±0.0030% of FSR/% V_S	*
+5V	±0.0015% of FSR/% V_S	*
DRIFT		
Specification Temperature Range	−25°C to +85°C	*
Gain (max)	±30ppm/°C	*
Offset		
Unipolar	±3ppm of FSR/°C	*
Bipolar (max)	±15ppm of FSR/°C	*
Linearity (max)	±3ppm of FSR/°C	*
Monotonicity	GUARANTEED	*
CONVERSION SPEED[5]	22μs typ, 25μs max	21μs max
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2TTL Loads	
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Status Output Drive	2TTL Loads	
Internal Clock		
Clock Output Drive	2TTL Loads	
Frequency[7]	575kHz	
INTERNAL REFERENCE VOLTAGE	6.3V ±10mV	
Max. External Current (with no degradation of specifications)	1.5mA	
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	
POWER REQUIREMENTS		
Rated Voltages	±15V, +5V	
Range for Rated Accuracy	4.75V to 5.25V and ±14.0V to ±16.0V	
Z Models[8]	4.75V to 5.25V and ±11.4V to ±16.0V	
Supply Drain +15V	+10mA	
−15V	−20mA	
+5V	+70mA	
TEMPERATURE RANGE		
Specification	−25°C to +85°C	
Operating (Derated Specs)	−55°C to +100°C	
Storage	−55°C to +125°C	
PACKAGE OPTION[9]		
DH-32D	AD ADC80-12	AD ADC80-10

NOTES
[1] DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital inputs, Logic "0" = +0.4V max and "1" = 2.4V min digital outputs.
[2] Adjustable to zero with external trimpots.
[3] FSR means Full Scale Range—for example, unit connected for ±10V range has 20V FSR.
[4] Error shown is the same as ±1/2LSB max for resolution of A/D converter.
[5] Conversion time with internal clock.
[6] See Table I. CSB – Complementary Straight Binary
COB – Complementary Offset Binary
CTC – Complementary Two's Complement
[7] For conversion speeds specified.
[8] For Z models order AD ADC80Z-12 or AD ADC80Z-10.
[9] For package outline information see Package Information section.

*Specifications same as AD ADC80-12.

Specifications subject to change withoutnoitice.

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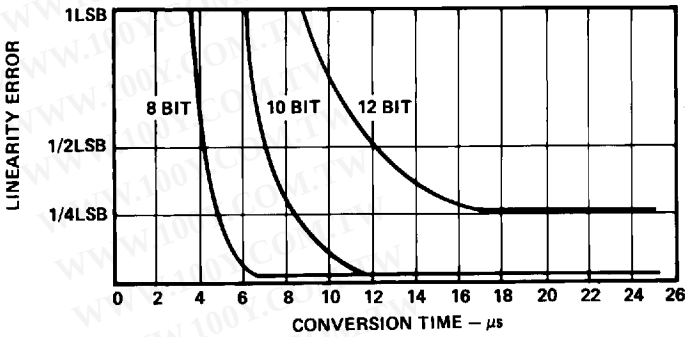


Figure 1. Linearity Error vs. Conversion Time (Normalized)

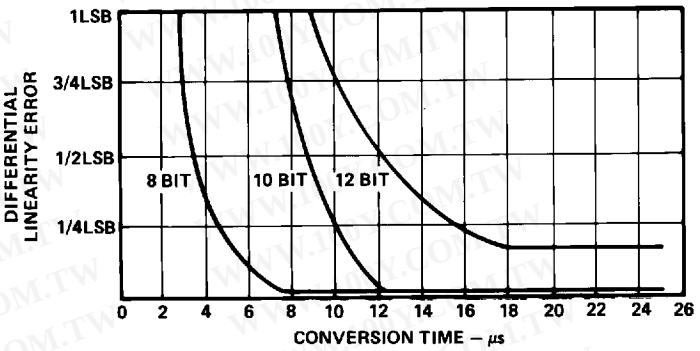


Figure 2. Differential Linearity Error vs. Conversion Time (Normalized)

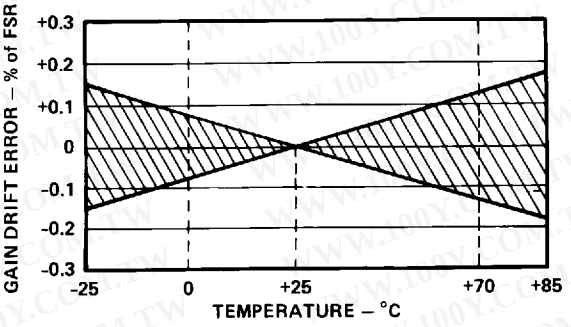


Figure 3. Maximum Gain Drift Error—% of FSR vs. Temperature

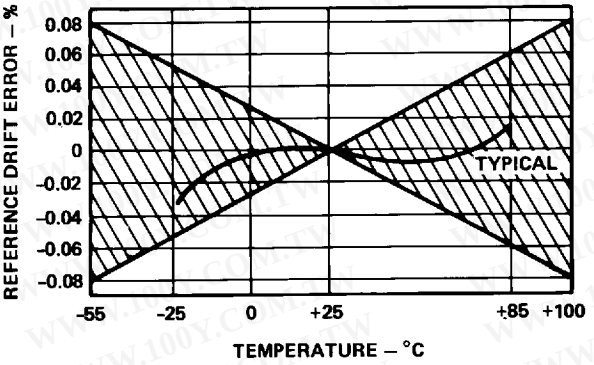


Figure 4. Reference Drift—% Error vs. Temperature

THEORY OF OPERATION

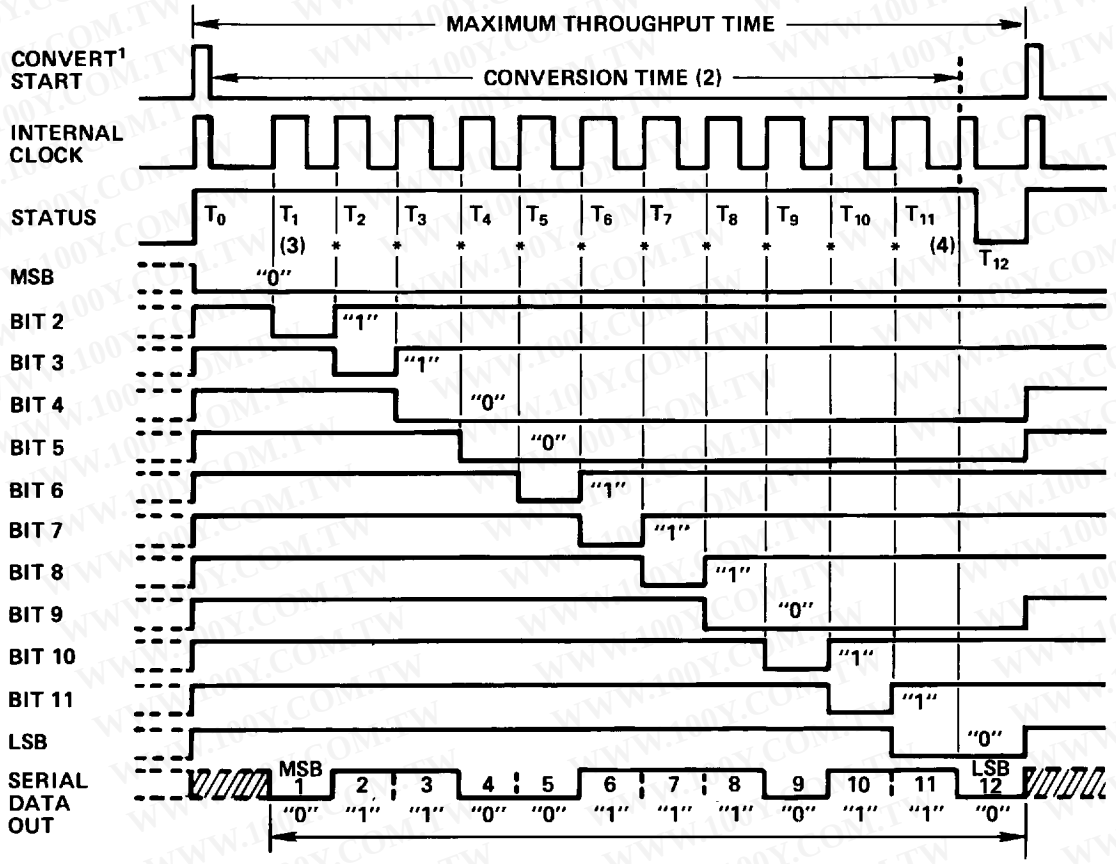
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 5. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 –B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 5).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 5. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse BIT 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 5. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 5). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9).

Connect Short Cycle Pin 21 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t_{12} +40ns
28	10	0.100	21	t_{10} +40ns
30	8	0.390	17	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 6 for circuit details.

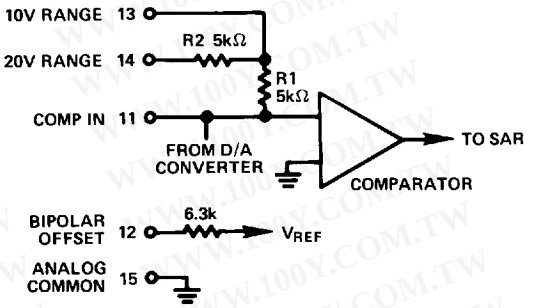


Figure 6. AD ADC80 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to +5V	CSB	15	Pin 11	13
0V to +10V	CSB	15	Open	13

Table II. AD ADC80 Input Scaling Connections

Binary (BIN) Output		INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

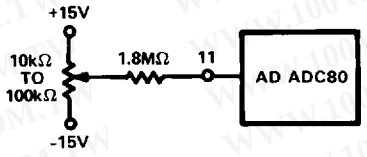


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 8.

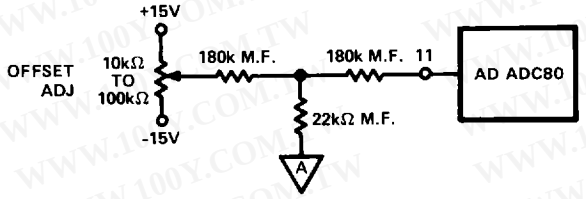


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 16 as shown in Figure 9.

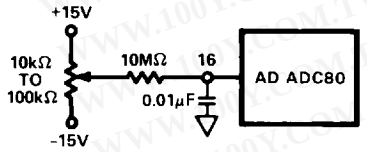


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 10.

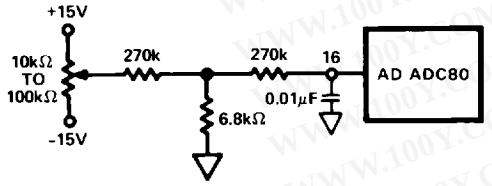


Figure 10. Low Tempco Gain Adjustment Circuit

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR −2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

−10V to +10V Range: Set analog input to −9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes," D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

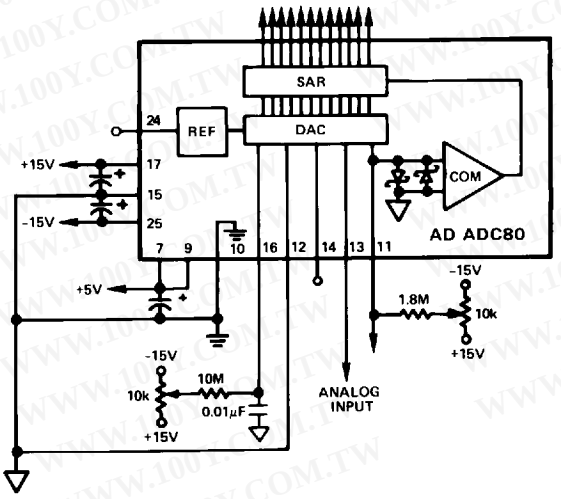


Figure 11. Analog and Power Connections for Unipolar 0–10V Input Range

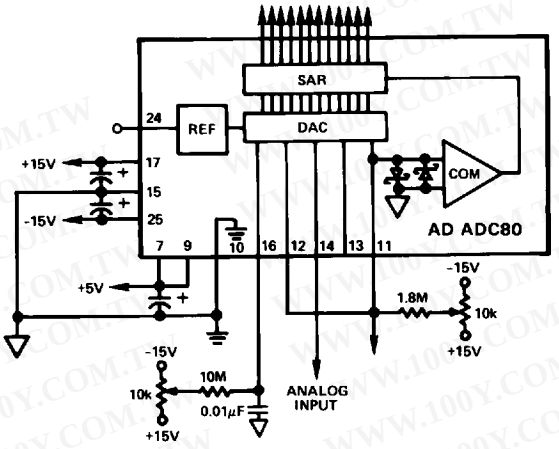


Figure 12. Analog and Power Connections for Bipolar ±10V Input Range

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point and the two device grounds should be tied together. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

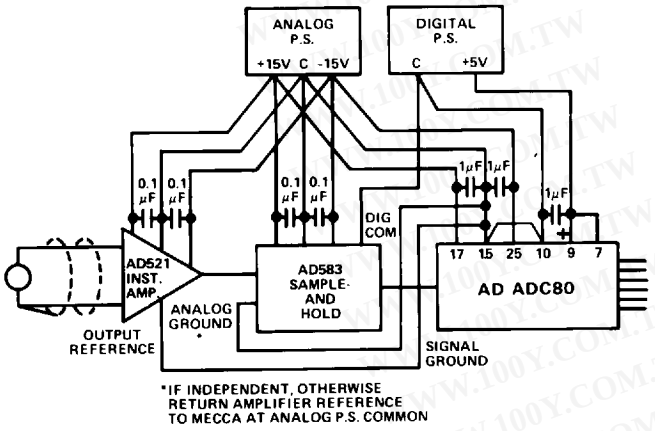


Figure 13. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14–16.

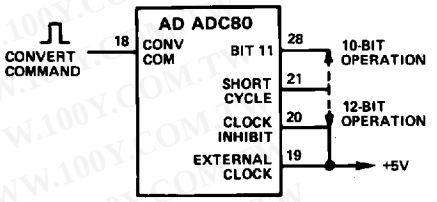


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

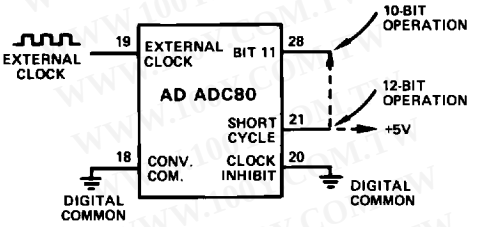


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

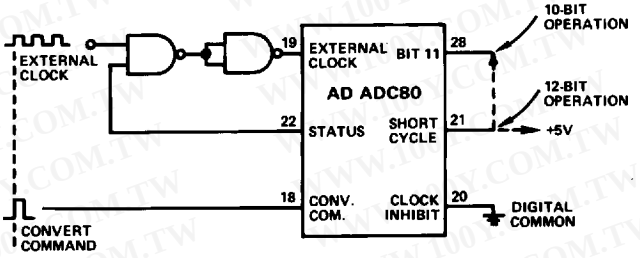


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).