# ADS823
# ADS826

# 10-Bit, 60MHz Sampling
# ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- **HIGH SNR: 60dB**
- **HIGH SFDR: 74dBFS**
- **LOW POWER: 265mW**
- **INTERNAL/EXTERNAL REFERENCE OPTION**
- **SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT**
- **PROGRAMMABLE INPUT RANGE**
- **LOW DNL: 0.25LSB**
- **SINGLE +5V SUPPLY OPERATION**
- **+3V/+5V LOGIC I/O COMPATIBLE (ADS826)**
- **POWER DOWN: 20mW**
- **SSOP-28 PACKAGE**

## APPLICATIONS

- **MEDICAL IMAGING**
- **COMMUNICATIONS**
- **CCD IMAGING**
- **VIDEO DIGITIZING**
- **TEST EQUIPMENT**

## DESCRIPTION

The ADS823 and ADS826 are pipeline, CMOS Analog-to-Digital Converters (ADCs) that operate from a single +5V power supply. These converters provide excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. These high-performance converters include a 10-bit quantizer, high-bandwidth track-and-hold, and a high-accuracy internal reference. They also allow for disabling the internal reference and utilizing external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where full-scale range adjustment is required.

The ADS823 and ADS826 employ digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Their low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS823 and ADS826 offer power dissipation of 265mW and also provide a power-down mode, thus reducing power dissipation to only 20mW.

The ADS823 and ADS826 are specified at a maximum sampling frequency of 60MHz and a single-ended input range of 1.5V to 3.5V. The ADS823 and ADS826 are available in an SSOP-28 package and are pin-compatible with the 10-bit, 40MHz ADS822 and ADS825, and the 10-bit, 75MHz ADS828.
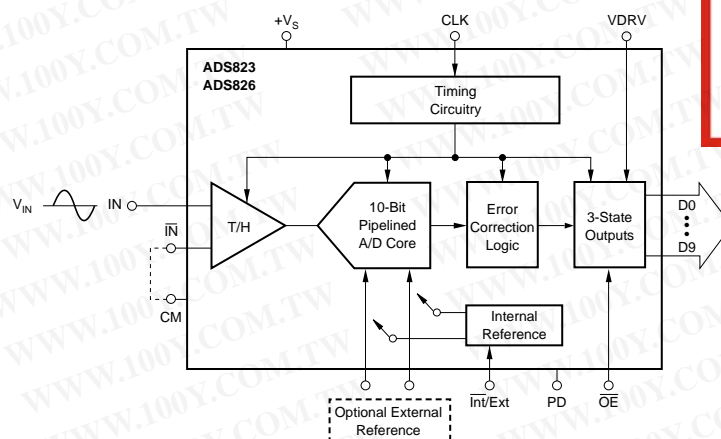
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# ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| +$V_S$ | +6V |
| Analog Input | −0.3V to (+$V_S$ + 0.3V) |
| Logic Input | −0.3V to (+$V_S$ + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

NOTE: (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions of extended periods may affect device reliability.

## EVALUATION MODULE ORDERING INFORMATION

| PRODUCT | EVALUATION MODULE |
|---|---|
| ADS823E | DEM-ADS823E |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[1] | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| ADS823E | SSOP-28 | DB | −40°C to +85°C | ADS823E | ADS823E | Rails |
| " | " | " | " | " | ADS823E/1K | Tape and Reel, 1000 |
| ADS826E | SSOP-28 | DB | −40°C to +85°C | ADS826E | ADS826E | Rails |
| " | " | " | " | " | ADS826E/1K | Tape and Reel, 1000 |

NOTE: (1) Fot the most current specifications and package information, refer to our web site at www.ti.com. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of ADS823E/1K" will get a single 1000-piece Tape and Reel.

# ELECTRICAL CHARACTERISTICS

At $T_A$ = full specified temperature range, $V_S$ = +5V single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

| | | ADS823E | | | ADS826E[1] | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | 10 Tested | | | 10 Tested | | Bits |
| **SPECIFIED TEMPERATURE RANGE** | Ambient Air | | −40 to +85 | | | −40 to +85 | | °C |
| **ANALOG INPUT** | | | | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | * | | * | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | * | | * | V |
| Common-Mode Voltage | | | 2.5 | | | * | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | * | | * | V |
| Analog Input Bias Current | | | 1 | | | * | | µA |
| Input Impedance | | | 1.25 ‖ 5 | | | * | | MΩ ‖ pF |
| Track-Mode Input Bandwidth | −3dBFS Input | | 300 | | | * | | MHz |
| **CONVERSION CHARACTERISTICS** | | | | | | | | |
| Sample Rate | | 10k | | 60M | * | | * | Samples/s |
| Data Latency | | | 5 | | | * | | Clk Cyc |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Differential Linearity Error (largest code error) | | | | | | | | |
|   f = 1MHz | | | ±0.25 | ±1.0 | | * | * | LSB |
|   f = 10MHz | | | ±0.25 | | | * | | LSB |
| No Missing Codes | | | Tested | | | Tested | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | | * | * | LSBs |
| Spurious-Free Dynamic Range[2] | | | | | | | | |
|   f = 1MHz | | | 74 | | | 73 | | dBFS[3] |
|   f = 10MHz | | 67 | 74 | | 65 | 73 | | dBFS |
| 2-Tone Intermodulation Distortion[4] | | | | | | | | |
|   f = 9.5MHz and 9.9MHz (−7dB each tone) | | | 64 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full-Scale Sinewave | | | | | | | |
|   f = 1MHz | | | 60 | | | 59 | | dB |
|   f = 10MHz | | 57 | 60 | | 56 | 59 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full-Scale Sinewave | | | | | | | |
|   f = 1MHz | | | 59 | | | 58 | | dB |
|   f = 10MHz | | 56 | 59 | | 55 | 58 | | dB |
| Effective Number of Bits[5], f = 1MHz | | | 9.5 | | | * | | Bits |
| Output Noise | Input Grounded | | 0.2 | | | * | | LSBs rms |
| Aperture Delay Time | | | 3 | | | * | | ns |
| Aperture Jitter | | | 1.2 | | | * | | ps rms |
| Over Voltage Recovery Time[5] | | | 2 | | | * | | ns |
| Full-Scale Step Acquisition Time | | | 5 | | | * | | ns |

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# ELECTRICAL CHARACTERISTICS (Cont.)

At $T_A$ = full specified temperature range, $V_S$ = +5V single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.
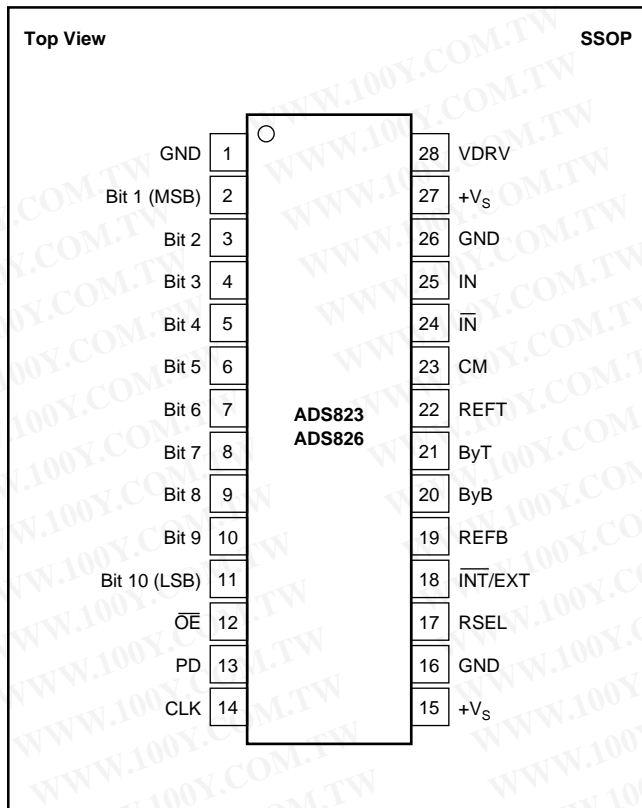
| | | ADS823E | | | ADS826E[1] | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Family | | CMOS-Compatible | | | TTL, +3V/+5V CMOS-Compatible | | | |
| Convert Command | Start Conversion | Rising Edge of Convert Clock | | | Rising Edge of Convert Clock | | | |
| High Level Input Current[6] ($V_{IN}$ = 5V) | | | | +100 | | | * | µA |
| Low Level Input Current ($V_{IN}$ = 0V) | | | | +10 | | | * | µA |
| High Level Input Voltage | | +3.5 | | | +2.0 | | | V |
| Low Level Input Voltage | | | | +1.0 | | | +0.8 | V |
| Input Capacitance | | | 5 | | | * | | pF |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Logic Family | | CMOS | | | CMOS | | | |
| Logic Coding | | Straight Offset Binary | | | Straight Offset Binary | | | |
| Low Output Voltage ($I_{OL}$ = 50µA to 1.6mA) | VDRV = 5V | | | +0.1 | | | * | V |
| High Output Voltage, ($I_{OH}$ = 50µA to 0.5mA) | | +4.9 | | | * | | | V |
| Low Output Voltage, ($I_{OL}$ = 50µA to 1.6mA) | VDRV = 3V | | | +0.1 | | | * | V |
| High Output Voltage, ($I_{OH}$ = 50µA to 0.5mA) | | +2.8 | | | * | | | V |
| 3-State Enable Time | $\overline{OE}$ = H to L | | 2 | 40 | | * | * | ns |
| 3-State Disable Time | $\overline{OE}$ = L to H | | 2 | 10 | | * | * | ns |
| Output Capacitance | | | 5 | | | * | | pF |
| **ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)** | $f_S$ = 2.5Mhz | | | | | | | |
| Zero Error (referred to –FS) | At 25°C | | ±1.0 | ±3.0 | | * | * | % FS |
| Zero Error Drift (referred to –FS) | | | 16 | | | * | | ppm/°C |
| Midscale Offset Error | At 25°C | | | | | ±0.29 | | % FS |
| Gain Error[7] | At 25°C | | ±1.5 | ±3.5 | | * | * | % FS |
| Gain Error Drift[7] | | | 66 | | | * | | ppm/°C |
| Gain Error[8] | At 25°C | | ±1.0 | ±2.5 | | * | * | % FS |
| Gain Error Drift[8] | | | 23 | | | * | | ppm/°C |
| Power-Supply Rejection of Gain | $\Delta V_S$ = ±5% | | 70 | | | * | | dB |
| REFT Tolerance | Deviation From Ideal 3.5V | | ±10 | ±25 | | * | * | mV |
| REFB Tolerance[9] | Deviation From Ideal 1.5V | | ±10 | ±25 | | * | * | mV |
| External REFT Voltage Range | | REFB + 0.8 | 3.5 | $V_S$ – 1.25 | * | * | * | V |
| External REFB Voltage Range | | 1.25 | 1.5 | REFT – 0.8 | * | * | * | V |
| Reference Input Resistance | REFT to REFB | | 1.6 | | | * | | kΩ |
| **POWER-SUPPLY REQUIREMENTS** | | | | | | | | |
| Supply Voltage: +$V_S$ | Operating | +4.75 | +5.0 | +5.25 | * | * | * | V |
| Supply Current: +$I_S$ | Operating | | 55 | | | * | | mA |
| Power Dissipation: VDRV = 5V | External Reference | | 275 | 335 | | * | * | mW |
| VDRV = 3V | External Reference | | 265 | | | * | | mW |
| VDRV = 5V | Internal Reference | | 295 | 350 | | * | * | mW |
| VDRV = 3V | Internal Reference | | 285 | | | * | | mW |
| Power-Down | Operating | | 20 | | | * | | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| SSOP-28 | | | 89 | | | * | | °C/W |

* Indicates the same specifications as the ADS823E.

NOTES: (1) ADS826 accepts a +3V clock input. (2) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS means dB relative to Full-Scale. (4) 2-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the 2-tone fundamental envelope. (5) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (6) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pin. (7) Includes internal reference. (8) Excludes internal reference. (9) Ensured by design.

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## PIN CONFIGURATION
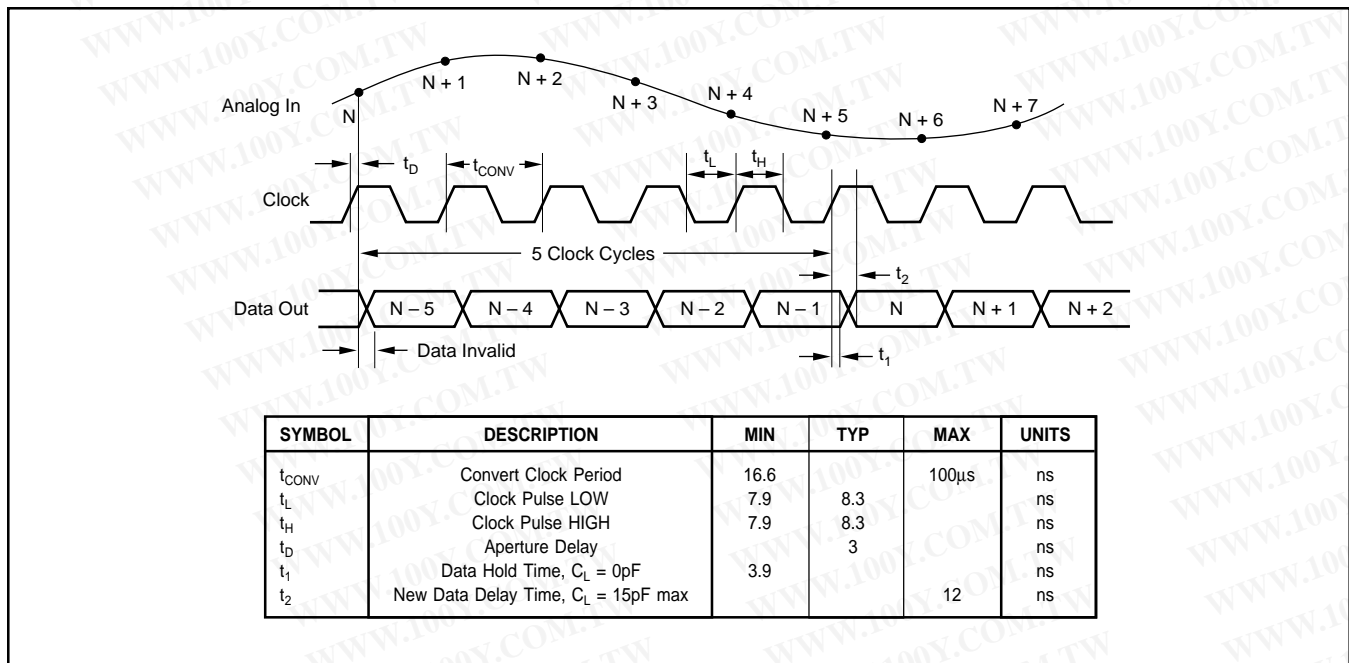
**Top View**    **SSOP**

```
              ADS823
              ADS826

GND        1          28   VDRV
Bit 1 (MSB) 2         27   +Vs
Bit 2      3          26   GND
Bit 3      4          25   IN
Bit 4      5          24   IN̄
Bit 5      6          23   CM
Bit 6      7          22   REFT
Bit 7      8          21   ByT
Bit 8      9          20   ByB
Bit 9      10         19   REFB
Bit 10 (LSB) 11       18   INT̄/EXT
OE̅         12         17   RSEL
PD         13         16   GND
CLK        14         15   +Vs
```

## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|-----|-----------|-------------|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D8) |
| 4 | Bit 3 | Data Bit 3 (D7) |
| 5 | Bit 4 | Data Bit 4 (D6) |
| 6 | Bit 5 | Data Bit 5 (D5) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 7 | Data Bit 7 (D3) |
| 9 | Bit 8 | Data Bit 8 (D2) |
| 10 | Bit 9 | Data Bit 9 (D1) |
| 11 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 12 | OE̅ | Output Enable. HI: High Impedance State. LO: Normal Operation (Internal Pull-Down Resistor) |
| 13 | PD | Power Down: HI = Power Down; LO = Normal |
| 14 | CLK | Convert Clock Input |
| 15 | +Vs | +5V Supply |
| 16 | GND | Ground |
| 17 | RSEL | Input Range Select: HI = 2V; LO = 1V |
| 18 | INT̄/EXT | Reference Select: HI = External; LO = Internal |
| 19 | REFB | Bottom Reference |
| 20 | ByB | Bottom Ladder Bypass |
| 21 | ByT | Top Ladder Bypass |
| 22 | REFT | Top Reference |
| 23 | CM | Common-Mode Voltage Output |
| 24 | IN̄ | Complementary Input (−) |
| 25 | IN | Analog Input (+) |
| 26 | GND | Ground |
| 27 | +Vs | +5V Supply |
| 28 | VDRV | Output Logic Driver Supply Voltage |

## TIMING DIAGRAM



| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|--------|-------------|-----|-----|-----|-------|
| $t_{CONV}$ | Convert Clock Period | 16.6 | | 100μs | ns |
| $t_L$ | Clock Pulse LOW | 7.9 | 8.3 | | ns |
| $t_H$ | Clock Pulse HIGH | 7.9 | 8.3 | | ns |
| $t_D$ | Aperture Delay | | 3 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12 | ns |

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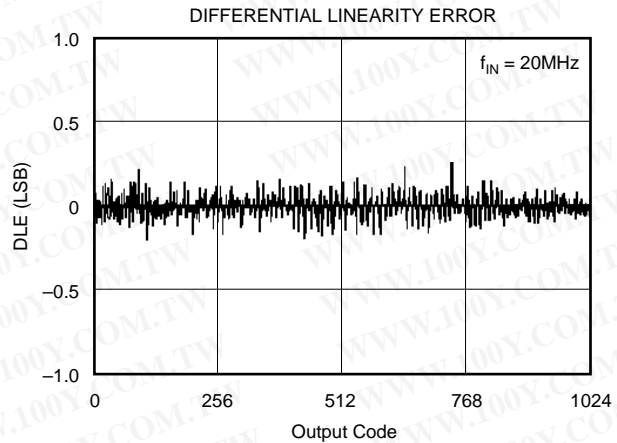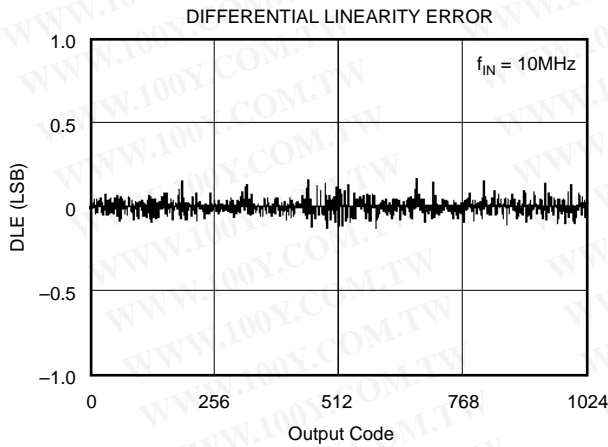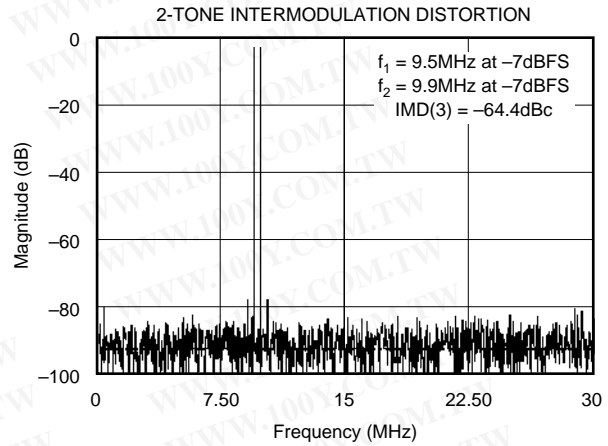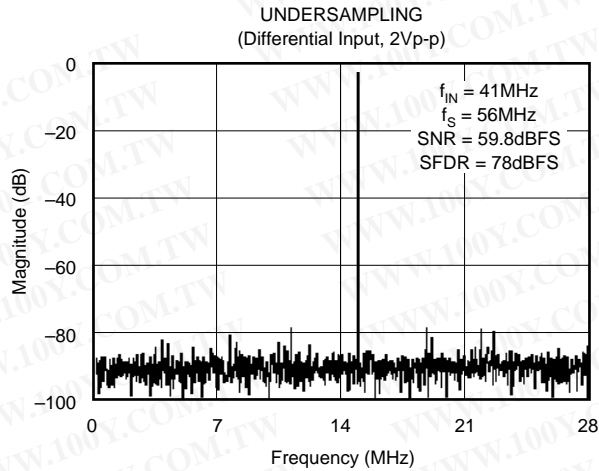www.ti.com

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# TYPICAL CHARACTERISTICS

At $T_A$ = full specified temperature range, $V_S$ = +5V single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

SPECTRAL PERFORMANCE

$f_{IN}$ = 1MHz
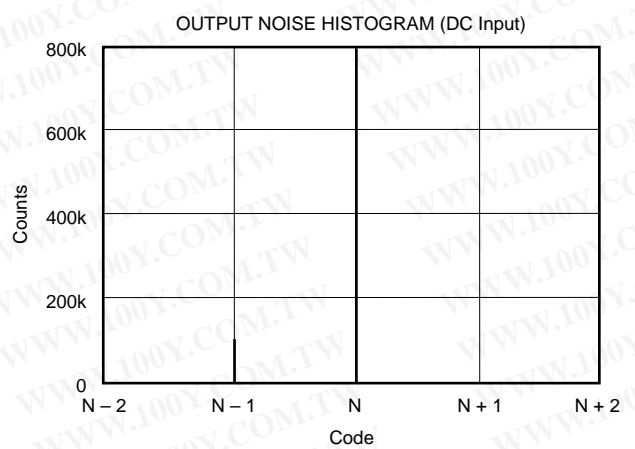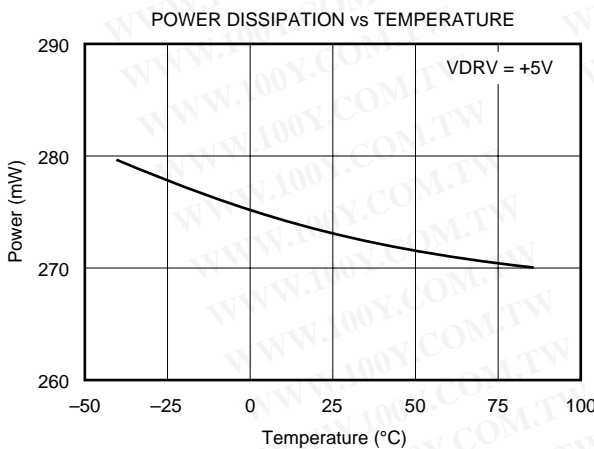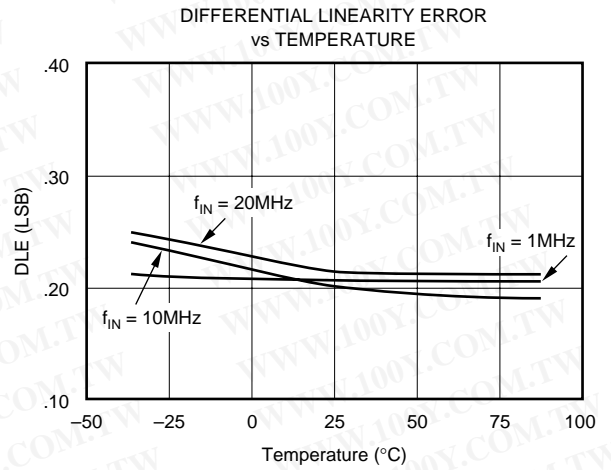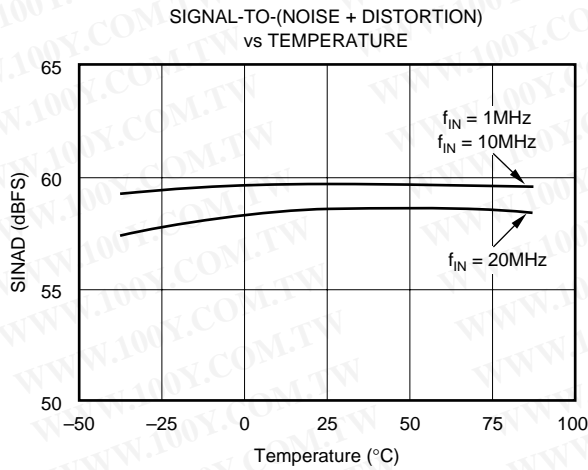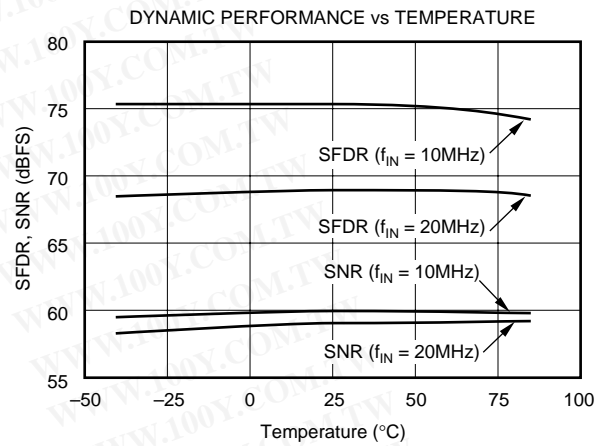SNR = 60dBFS
SFDR = 77dBFS

SPECTRAL PERFORMANCE

$f_{IN}$ = 10MHz
SNR = 60dBFS
SFDR = 76dBFS

SPECTRAL PERFORMANCE
(Single-Ended, 1Vp-p)

$f_{IN}$ = 10MHz
SNR = 56.6dBFS
SFDR = 74dBFS

SPECTRAL PERFORMANCE
(Differential Input, 2Vp-p)

$f_{IN}$ = 10MHz
SNR = 60dBFS
SFDR = 73dBFS

SPECTRAL PERFORMANCE
(Differential Input, 2Vp-p)

$f_{IN}$ = 20MHz
SNR = 60.4dBFS
SFDR = 72dBFS

SPECTRAL PERFORMANCE

$f_{IN}$ = 20MHz
SNR = 58.7dBFS
SFDR = 70dBFS

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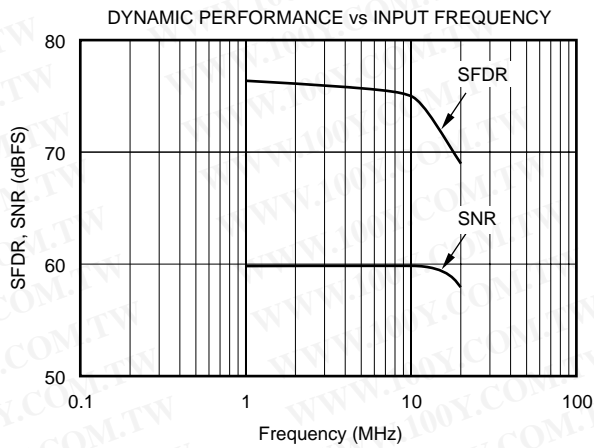# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = full specified temperature range, $V_S$ = +5V single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

UNDERSAMPLING
(Differential Input, 2Vp-p)

$f_{IN}$ = 41MHz
$f_S$ = 56MHz
SNR = 59.8dBFS
SFDR = 78dBFS

2-TONE INTERMODULATION DISTORTION

$f_1$ = 9.5MHz at −7dBFS
$f_2$ = 9.9MHz at −7dBFS
IMD(3) = −64.4dBc

DIFFERENTIAL LINEARITY ERROR

$f_{IN}$ = 10MHz

DIFFERENTIAL LINEARITY ERROR

$f_{IN}$ = 20MHz

INTEGRAL LINEARITY ERROR

$f_{IN}$ = 1MHz

SWEPT POWER SFDR

$f_{IN}$ = 10MHz

dBFS

dBc

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# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = full specified temperature range, $V_S$ = +5V single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, external reference, unless otherwise noted.

DYNAMIC PERFORMANCE vs INPUT FREQUENCY

DYNAMIC PERFORMANCE vs TEMPERATURE

SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

POWER DISSIPATION vs TEMPERATURE

OUTPUT NOISE HISTOGRAM (DC Input)

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# APPLICATION INFORMATION

## THEORY OF OPERATION

The ADS823 and ADS826 are high-speed CMOS ADCs which employ a pipelined converter architecture consisting of 9 internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 10-bit level. The output data becomes valid on the rising clock edge (see Timing Diagram on page 4). The pipeline architecture results in a data latency of 5 clock cycles.

The analog input of the ADS823 and the ADS826 is a differential track-and-hold, as shown in Figure 1. The differential topology along with tightly matched capacitors produce a high level of AC-performance while sampling at very high rates.

The ADS823 and ADS826 allows its analog inputs to be driven either single-ended or differentially. The typical configuration for the ADS823 and the ADS826 is for the single-ended mode in which the input track-and-hold performs a single-ended to differential conversion of the analog input signal.

Both inputs (IN, $\overline{IN}$) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

The following application discussion focuses on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS823 and ADS826 are characterized using the single-ended mode of operation.

## DRIVING THE ANALOG INPUT

The ADS823 and ADS826 achieve excellent AC performance either in the single-ended or differential mode of operation. The selection for 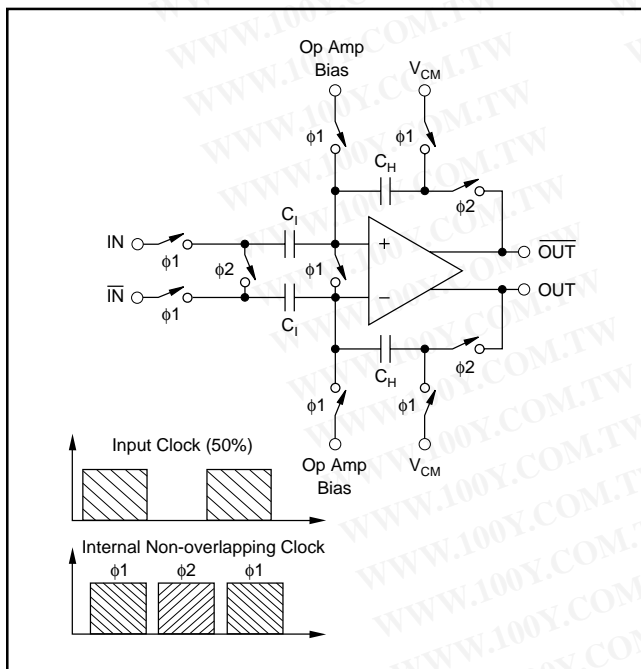the optimum interface configuration will depend on the individual application requirements and system structure. For example, communications applications often process a band of frequencies that does not include DC, whereas in imaging applications, the previously restored DC level must be maintained correctly up to the ADC. Features on the ADS823 and ADS826 like the input range select (RSEL pin) or the option for an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the ADS823 and ADS826 should be configured such that the application objectives are met while observing the headroom requirements of the driving amplifier in order to yield the best overall performance.

## INPUT CONFIGURATIONS

### AC-Coupled, Single-Supply Interface

See Figure 2 for the typical circuit for an AC-coupled analog input configuration of the ADS823 and ADS826 while all components are powered from a single +5V supply.

With the RSEL pin connected HIGH, the full-scale input range is set to 2Vp-p. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3.5V and +1.5V, respectively. Two resistors ( 2x 1.62kΩ) are used to create a common-mode voltage ($V_{CM}$) of approximately +2.5V to bias the inputs of the driving amplifier A1. Using the OPA680 on a single +5V supply, its ideal common-mode point is at +2.5V, which coincides with the recommended common-mode input level for the ADS823 and ADS826, thus obviating the need of a coupling capacitor between the amplifier and the converter. Even though the OPA680 has an AC gain of +2, the DC gain is only +1 due to the blocking capacitor at resistor $R_G$.

The addition of a small series resistor ($R_S$) between the output of the op amp and the input of the ADS823 and ADS826 will be beneficial in almost all interface configurations. This will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor in combination with the 10pF capacitor establishes a passive low-pass filter limiting the bandwidth for the wideband noise, thus helping improve the SNR performance.

### AC-Coupled, Dual-Supply Interface

See The circuit provided in Figure 3 for typical connections of the analog input in case the selected amplifier operates on dual supplies. This might be necessary to take full advantage of very low distortion operational amplifiers, like the OPA642. The advantage is that the driving amplifier can be operated with a ground referenced bipolar signal swing. This will keep the distortion performance at its lowest since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. By capacitively coupling the single-ended signal to the input of the ADS823 and ADS826, their common-mode requirements can easily be satisfied with two resistors connected between the top and bottom reference.
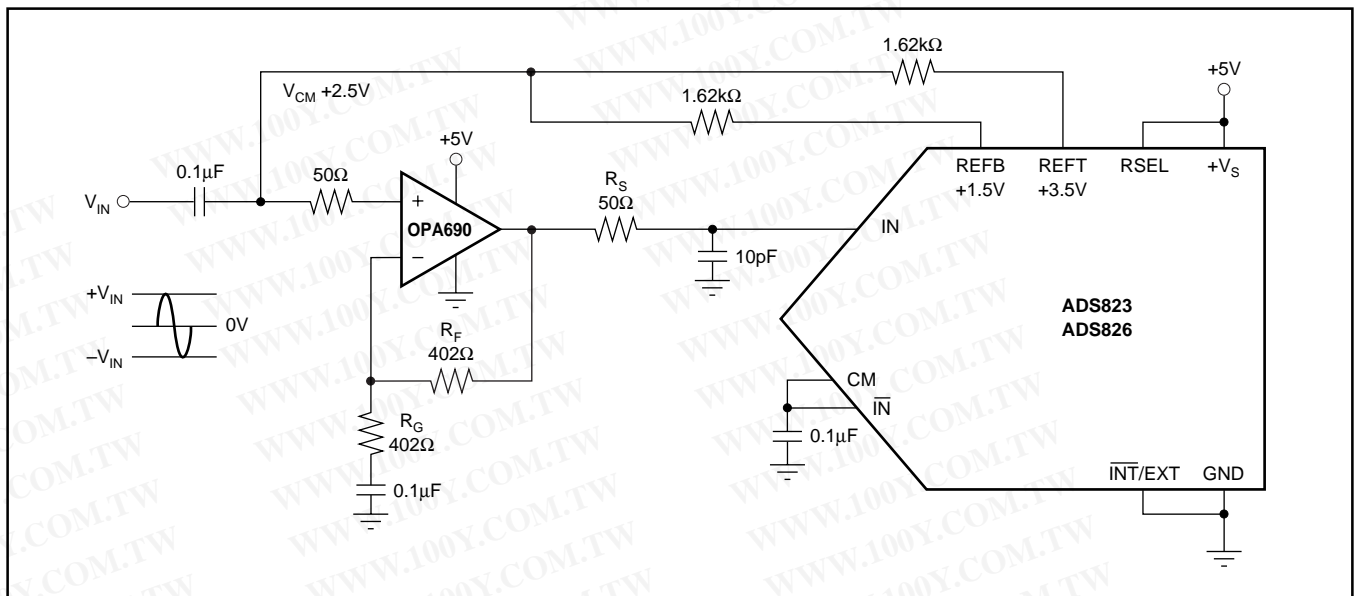


FIGURE 1. Simplified Circuit of Input Track-and-Hold with Timing Diagram.

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FIGURE 2. AC-Coupled Input Configuration for a 2Vp-p Full-Scale Range and a Common-Mode Voltage, $V_{CM}$, at +2.5V Derived from the Internal Top (REFT) and Bottom Reference (REFB).
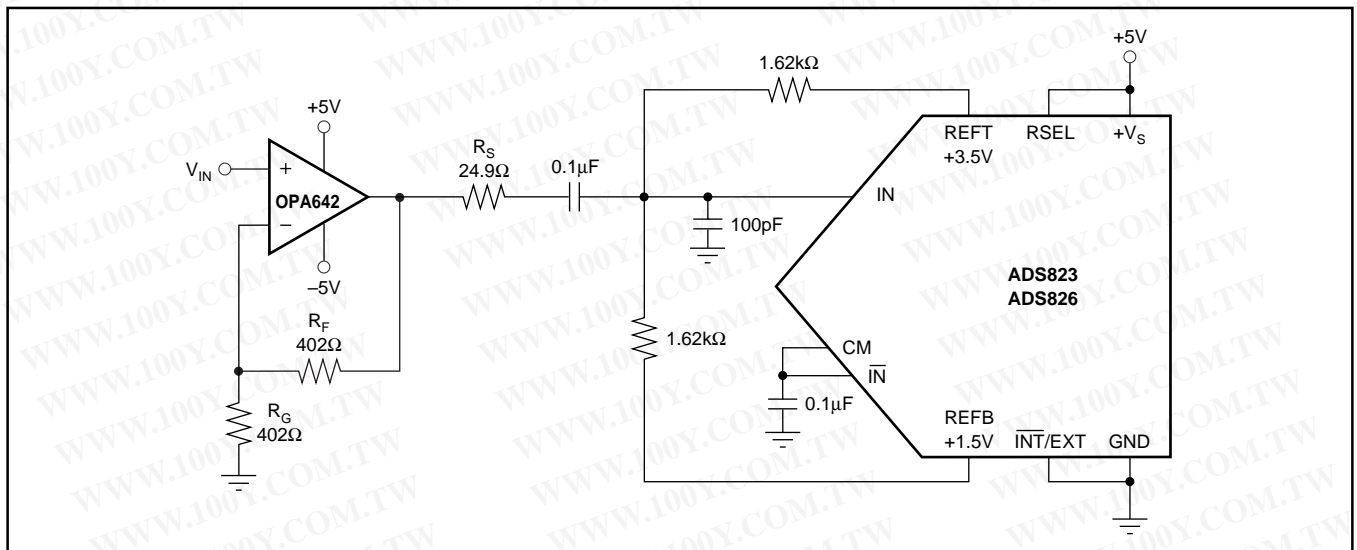


FIGURE 3. AC-Coupling the Dual-Supply Amplifier OPA642 to the ADS823 and ADS826 for a 2Vp-p Full-Scale Input Range.

For applications requiring the driving amplifier to provide a signal amplification, with a gain ≥ 5, consider using decompensated voltage-feedback op amps, like the OPA686, or current-feedback op amps like the OPA6901.

### DC-Coupled with Level Shift

Several applications may require that the bandwidth of the signal path includes DC, in which case the signal has to be DC-coupled to the ADC. In order to accomplish this, the interface circuit has to provide a DC level shift to the analog input signal. The circuit of in Figure 4 employs a dual op amp, A1, to drive the input of the ADS823 and ADS826, and level shift the signal to be compatible with the selected input range. With the RSEL pin tied to the supply and the INT/$\overline{EXT}$ pin to ground, the ADS823 and ADS826 are configured for a 2Vp-p input range and uses the internal references. The complementary input ($\overline{IN}$) may be appropriately biased using

the +2.5V common-mode voltage available at the CM pin. One half of amplifier A1 buffers the REFB pin and drives the voltage divider $R_1$, $R_2$. Due to the op amp's noise gain of +2V/V, assuming $R_F = R_{IN}$, the common-mode voltage ($V_{CM}$) has to be re-scaled to +1.25V. This results in the correct DC level of +2.5V for the signal input (IN). Any DC voltage differences between the IN and $\overline{IN}$ inputs of the ADS823 and ADS826 effectively produce an offset, which can be corrected for by adjusting the resistor values of the divider, $R_1$ and $R_2$. The selection criteria for a suitable op amp should include the supply voltage, input bias current, output voltage swing, distortion, and noise specification. Note that in this example the overall signal phase is inverted. To re-establish the original signal polarity, it is always possible to interchange the IN and $\overline{IN}$ connections.

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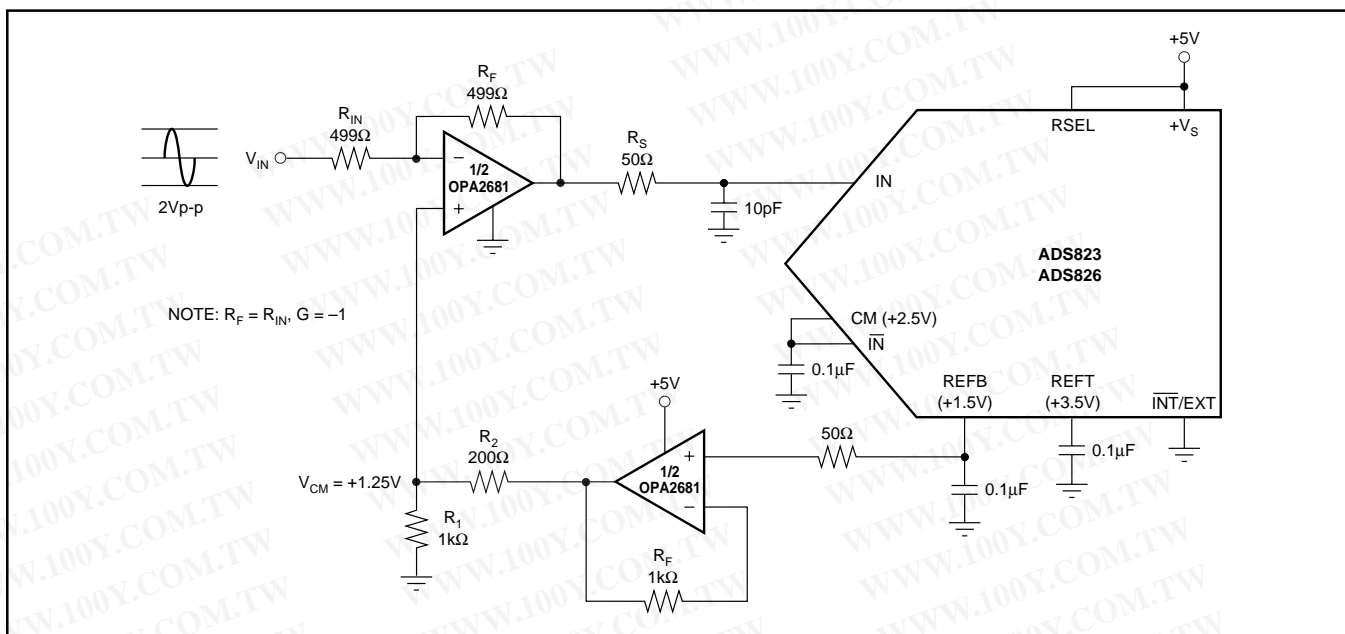TEXAS INSTRUMENTS
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FIGURE 4. DC-Coupled Interface Circuit with Level-Shifting, Dual Current-Feedback Amplifier OPA2681.

## SINGLE-ENDED TO DIFFERENTIAL CONFIGURATION (Transformer Coupled)

If the application requires a signal conversion from a single-ended source to feed the ADS823 and ADS826 differentially, a RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode, both inputs of the ADS823 and ADS826 see matched impedances, and the differential signal swing can be reduced to half of the swing required for single-ended drive. Figure 5 shows the schematic for the suggested transformer-coupled interface circuit.
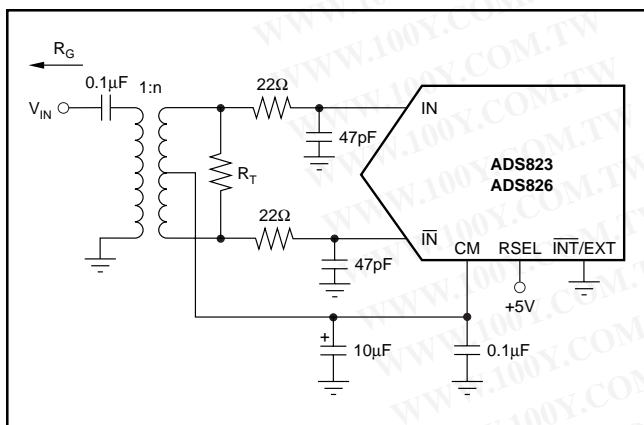


FIGURE 5. Transformer-Coupled Input.

The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side ($R_T$) should be calculated using the equation $R_T = n^2 \cdot R_G$ to match the source impedance ($R_G$) for good power transfer and VSWR.

## REFERENCE OPERATION

Figure 6 depicts the simplified model of the internal reference circuit. The internal blocks are the bandgap voltage reference, the drivers for the top and bottom reference, and the
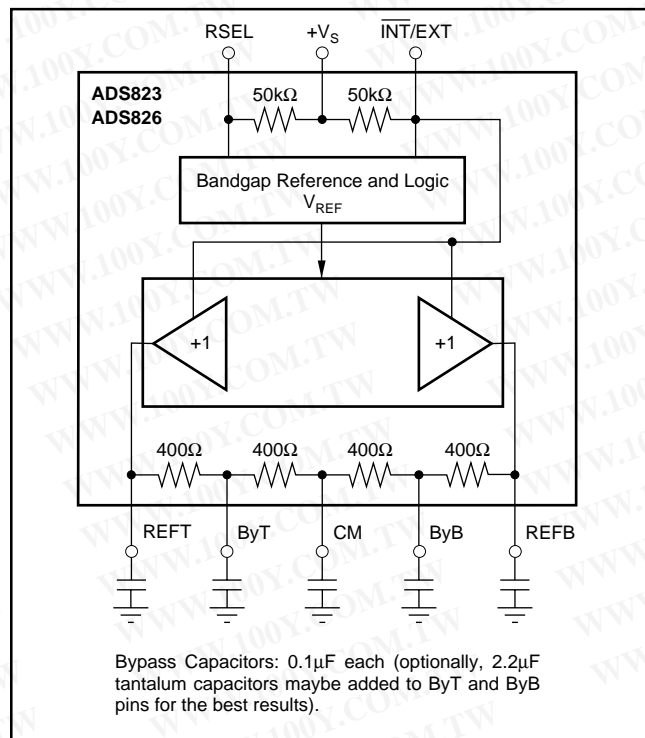


Bypass Capacitors: 0.1µF each (optionally, 2.2µF tantalum capacitors maybe added to ByT and ByB pins for the best results).

FIGURE 6. Equivalent Reference Circuit with Recommended Reference Bypassing.

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resistive reference ladder. The bandgap reference circuit includes logic functions that allow to set the analog input swing of the ADS823 and ADS826 to either a 1Vp-p or 2Vp-p full-scale range simply by tying the RSEL pin to a LOW or HIGH potential, respectively. While operating the ADS823 and ADS826 in the external reference mode, the buffer amplifiers for the REFT and REFB are disconnected from the reference ladder.

As shown, the ADS823 and ADS826 have internal 50kΩ pull-up resistors at the range select pin (RSEL) and reference select pin (INT/EXT). Leaving those pins open configures the ADS823 for a 2Vp-p input range and external reference operation. Setting the ADS823 up for internal reference mode requires bringing the INT/EXT pin LOW.

The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. The resistor ladders of the ADS823 and ADS826 are divided into several segments and have two additional nodes, ByT and ByB, which are brought out for external bypassing only (See Figure 6). To ensure proper operation with any reference configurations, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum. All bypassing capacitors should be located as close to their respective pins as possible.
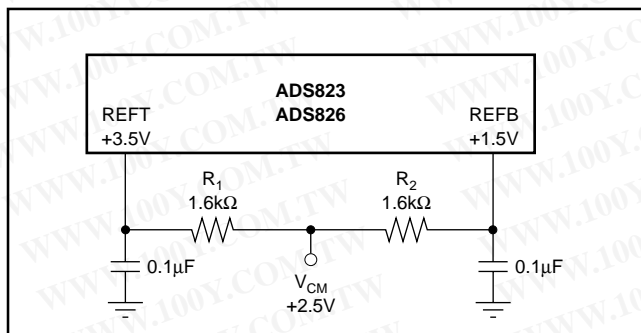


FIGURE 7. Alternative Circuit to Generate CM Voltage.

The common-mode voltage available at the CM pin may be used as a bias voltage to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternative way of generating a common-mode voltage is given in Figure 7. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode voltage, $V_{CM}$, will appear at the midpoint.

## EXTERNAL REFERENCE OPERATION

For even more design flexibility, the internal reference can be disabled and an external reference voltage be used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. Especially in multichannel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

The external references can vary as long as the value of the external top reference $REFT_{EXT}$ stays within the range of $(V_S - 1.25V)$ and $(REFB + 0.8V)$, and the external bottom reference $REFB_{EXT}$ stays within 1.25V and $(REFT - 0.8V)$, as shown in Figure 8.

## DIGITAL INPUTS AND OUTPUTS

### Clock Input Requirements

Clock jitter is critical to the SNR performance of high-speed, high-resolution ADCs. Clock jitter leads to aperture jitter ($t_A$), which adds noise to the signal being converted. The ADS823 and ADS826 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by
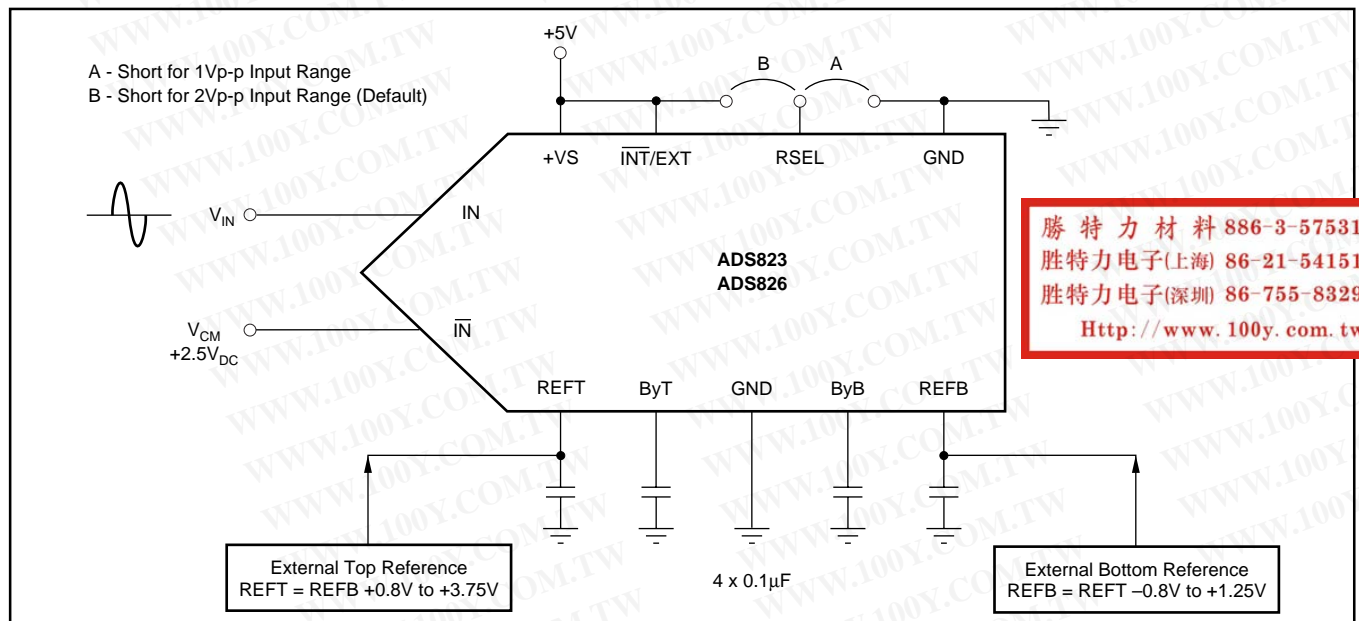


FIGURE 8. Configuration Example for External Reference Operation.

the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20 \log \frac{1}{2\pi f_{IN}\, t_A} \text{ rms signal to rms noise}$$

where: $f_{IN}$ is input signal frequency
$t_A$ is rms clock jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less. To estimate the typical performance deviation for clock duty cycles in the range of 50% ±7.5%, refer to Figure 9. The clock input of the ADS826 can be driven with either 3V or 5V logic levels. Using low-voltage logic (3V) may lead to improved AC performance of the converters.
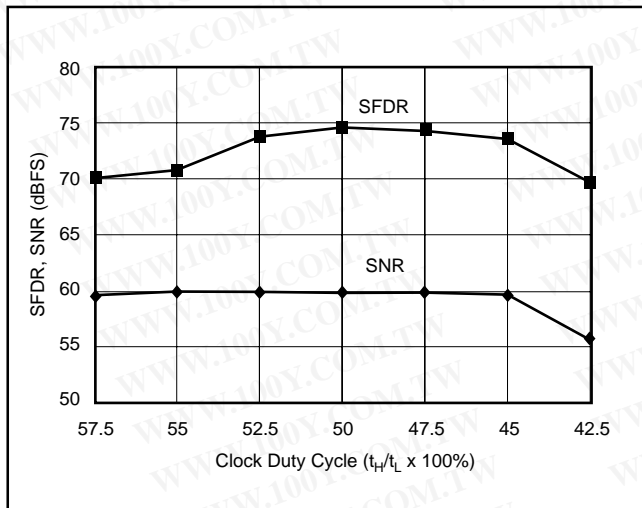


FIGURE 9. ADS823 and ADS826 Duty Cycle Sensitivity.

## Digital Outputs

The output data format of the ADS823 and ADS826 is in positive Straight Offset Binary code as shown in Tables I and II. This format can easily be converted into the Binary Two's Complement code by inverting the MSB.

| SINGLE-ENDED INPUT ($\overline{IN}$ = CMV) | STRAIGHT OFFSET BINARY (SOB) |
|---|---|
| +FS −1LSB (IN = REFT) | 1111111111 |
| +1/2 Full-Scale | 1100000000 |
| Bipolar Zero (IN = $V_{CM}$) | 1000000000 |
| −1/2 Full-Scale | 0100000000 |
| −FS (IN = REFB) | 0000000000 |

TABLE I. Coding Table for Single-Ended Input Configuration with $\overline{IN}$ tied to the Common-Mode Voltage ($V_{CM}$).

| DIFFERENTIAL INPUT | STRAIGHT OFFSET BINARY (SOB) |
|---|---|
| +FS −1LSB (IN = +3V, $\overline{IN}$ = +2V) | 1111111111 |
| +1/2 Full-Scale | 1100000000 |
| Bipolar Zero (IN = $\overline{IN}$ = $V_{CM}$) | 1000000000 |
| −1/2 Full-Scale | 0100000000 |
| −FS (IN = +2V, $\overline{IN}$ = +3V) | 0000000000 |

TABLE II. Coding Table for Differential Input Configuration and 2Vp-p Full-Scale Range.

It is recommended to keep the capacitive loading on the data lines as low as possible ($\leq$ 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS823 and ADS826 and affect performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS823 and ADS826 from any digital noise activities on the bus coupling back high frequency noise.

## Digital Output Driver (VDRV)

The ADS823 and ADS826 feature a dedicated supply pin for the output logic drivers, VDRV, which is not internally connected to the other supply pins. Setting the voltage at VDRV to +5V or +3V, the ADS823 and ADS826 produce corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS823 and ADS826 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line which may affect the AC-performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi-filter.

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## GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS823 and ADS826 should be treated as analog components. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS823 and ADS826 are internally joined together, obviating the design of split ground planes. The ground pins (1, 16, 26) should directly connect to an analog ground plane which covers the PC board area around the converter. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Due to the high sampling rate, the ADS823 and ADS826 generate high frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 10 shows the recommended decoupling scheme for the ADS823 and ADS826. In most cases 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor (1µF to 22µF) should be placed on the PC board in proximity of the converter circuit.



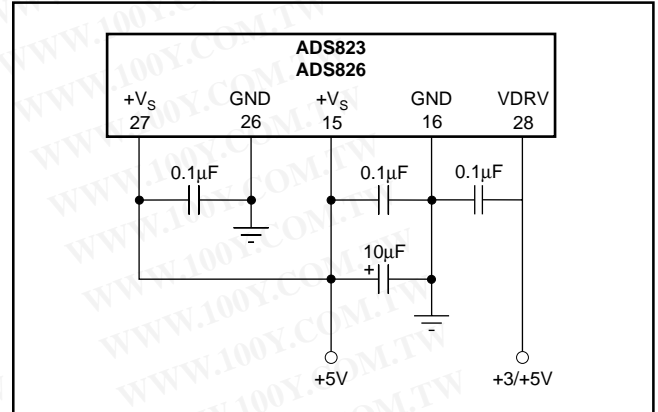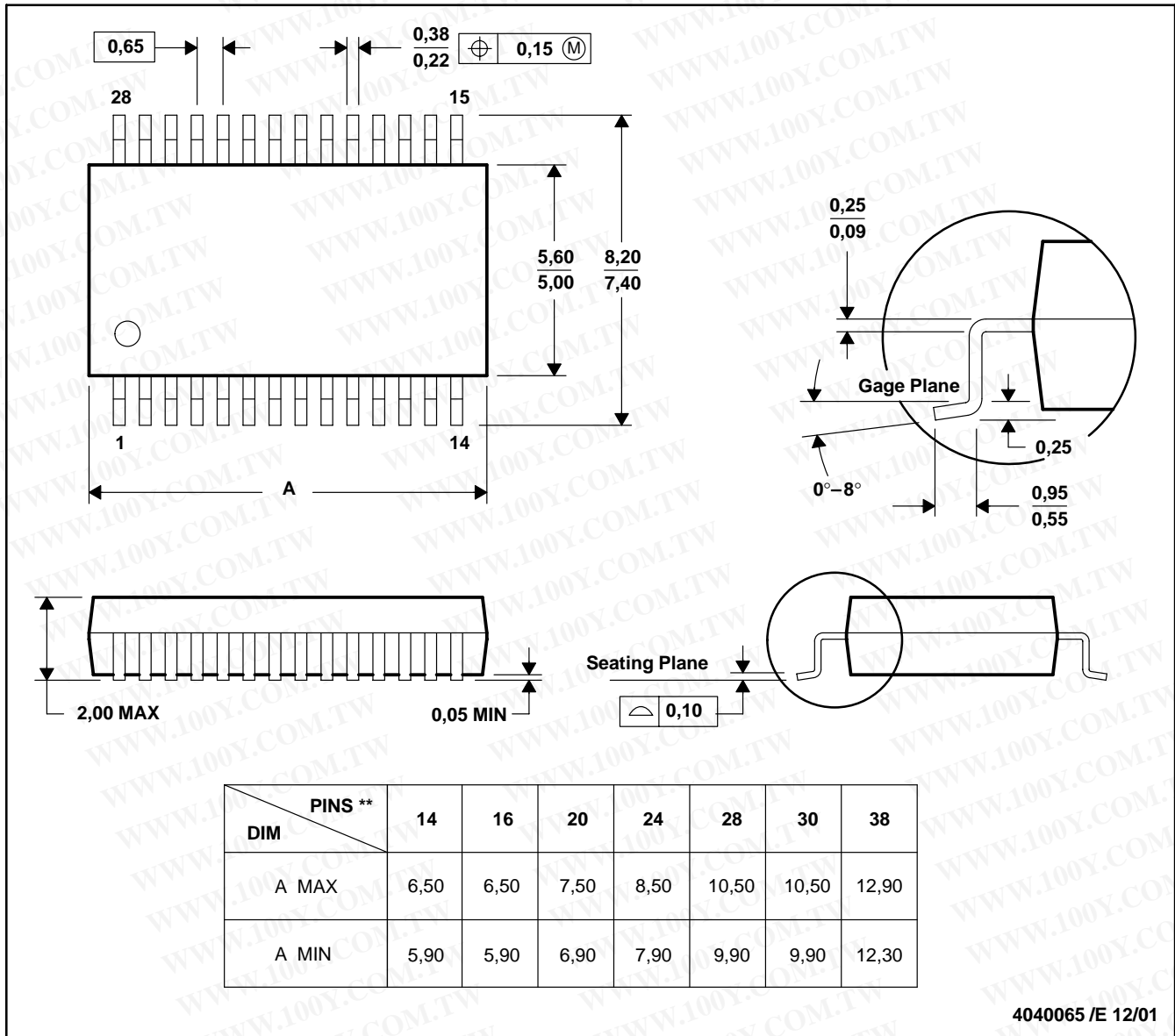FIGURE 10. Recommended Bypassing for the Supply Pins.

# PACKAGE DRAWING

**DB (R-PDSO-G\*\*)**            **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



| PINS \*\* DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A  MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A  MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES:  A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Body dimensions do not include mold flash or protrusion not to exceed 0,15.
         D.  Falls within JEDEC MO-150

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## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| ADS823E | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS823E/1K | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS823E/1KG4 | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS823EG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS826E | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS826E/1K | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS826E/1KG4 | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS826EG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
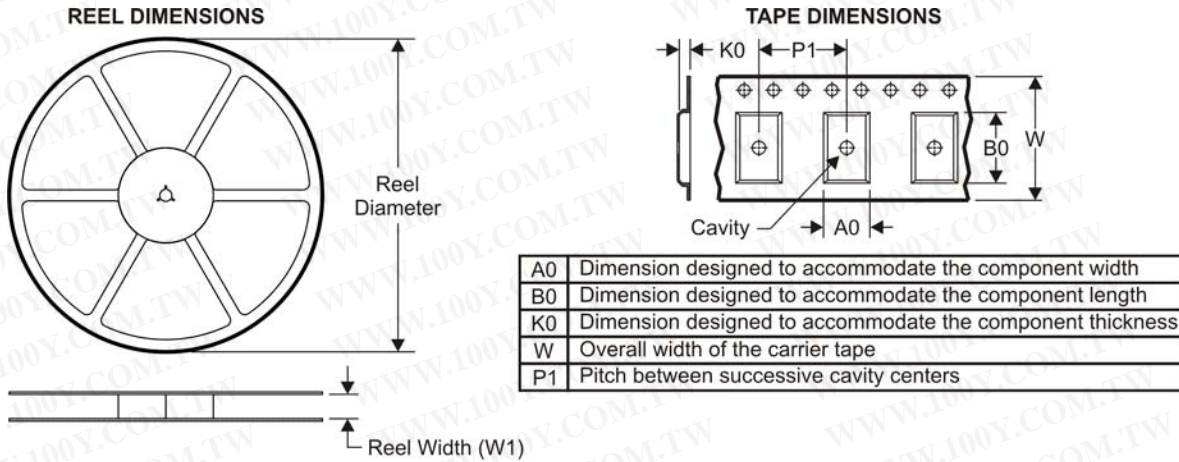
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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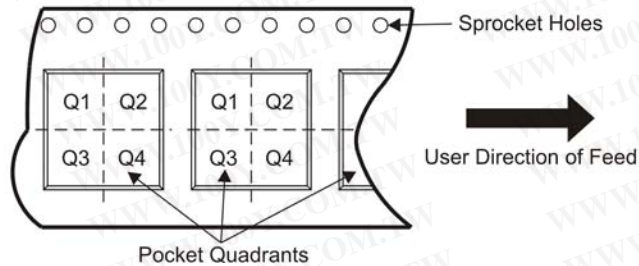
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**

K0 ← P1 →

B0  W

Cavity — A0

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

| Q1 | Q2 |
| Q3 | Q4 |

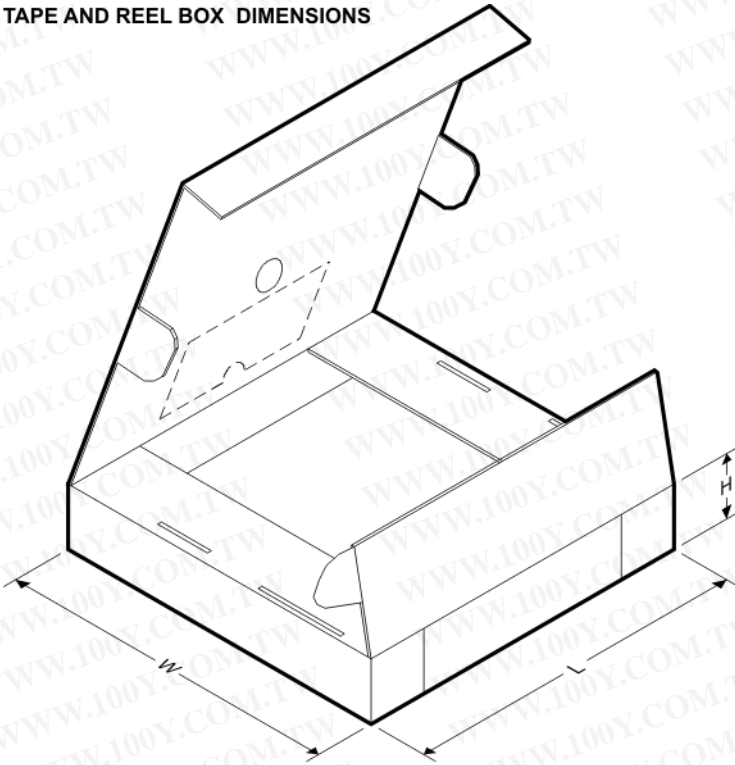| Q1 | Q2 |
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS823E/1K | SSOP | DB | 28 | 1000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| ADS826E/1K | SSOP | DB | 28 | 1000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| ADS823E/1K | SSOP | DB | 28 | 1000 | 346.0 | 346.0 | 33.0 |
| ADS826E/1K | SSOP | DB | 28 | 1000 | 346.0 | 346.0 | 33.0 |

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| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
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