勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw



CMOS Dual 8-Bit Buffered Multiplying DACs

General Description

The MX7528/MX7628 contains two 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors. The data load operation is similar to a static RAM write cycle. Data is loaded using only CS, WR, and DAC Select (DAC A/DAC B) inputs.

Each DAC has a separate reference input and internal feedback resistor which allow fully independent operation while maintaining excellent DAC-to-DAC matching.

The MX7528 operates from a single +5V to +15V power supply whereas the MX7628 operates from +12V to +15V. The MX7528 has TTL compatible inputs at +5V supply only and the MX7628 has TTL compatible inputs from +12V to +15V supplies.

The MX7528/MX7628 is supplied in 20-lead narrow DIP and Small Outline Packages.

Applications

Programmable Attenuators
Digitally Controlled Filters
X-Y Graphics
Motion Control Systems
Digital-to-Synchro Conversion
Disk Drives

____ Features

- Data Latches For Both DACs
- ♦ MX7528—+5V to +15V Single Supply Operation
- ♦ MX7628—+12V to +15V Single Supply Operation With TTL/CMOS Compatible Inputs
- ♦ ±½ LSB Linearity
- Microprocessor Compatible
- ♦ Four-Quadrant Multiplication
- ◆ DACs Matched to 1%

Ordering Information

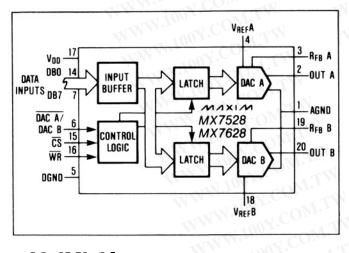
PART	TEMP. RANGE	PACKAGE*	ERROR
MX7528JN	0°C to +70°C	Plastic DIP	±1 LSB
MX7528KN	0°C to +70°C	Plastic DIP	±1/2 LSB
MX7528LN	0°C to +70°C	Plastic DIP	±1/2 LSB
MX7528JCWP	0°C to +70°C	Wide SO	±1 LSB
MX7528KCWP	0°C to +70°C	Wide SO	±1/2 LSB
MX7528LCWP	0°C to +70°C	Wide SO	±1/2 LSB
MX7528J/D	0°C to +70°C	Dice	±1 LŞB
MX7528AQ	-25°C to +85°C	CERDIP**	±1 LSB
MX7528BQ	-25°C to +85°C	CERDIP**	±1/2 LSB
MX7528CQ	-25°C to +85°C	CERDIP**	±1/2 LSB

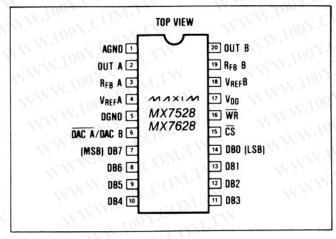
- * All devices 20 lead packages
- ** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages

Ordering Information continued on last page.

Functional Diagram

Pin Configuration





ABSOLUTE MAXIMUM RATINGS-MX7528, MX7628

V _{DD} to AGND		Operating Tempera
V _{DD} to DGND		MX7528JN, KN,
AGND to DGND	V _{DD}	KCWP, LCWP; N
DGND to AGND		MX7528AQ, BQ,
Digital Input Voltage to DGND	0.3V, V _{DD}	MX7528KE, LE
Pin 2, Pin 20 to AGND		MX7528SD, SQ.
VREFA, VREFB, to AGND	±25V	UD, UQ; MX7628
VRFBA, VRFBB, to AGND		Storage Temperatu
		Power Dissipation

Operating Temperature Ranges:	
MX7528JN, KN, LN, JCWP,	
KCWP, LCWP; MX7628KN, KCWP	0°C to +70°C
MX7528AQ, BQ, CQ; MX7628BQ	25°C to +85°C
MX7528KE, LE	40°C to +85°C
MX7528SD, SQ, TD, TQ,	
UD, UQ; MX7628TQ	55°C to +125°C
Storage Temperature Range	65°C to +160°C
Power Dissipation (any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MX7528, +5V Operation $(V_{DD} = +5V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} \text{ to } T_{MAX} \text{ unless otherwise noted)}$

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)	WWW	. TVI	MMM	ON.C	V-17	W	•
Resolution		N. Ina COM.	N. MAN.	8	COA	TW	Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U	WWW	N.1002	Y CON	±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.	TW WY	W.10	OY.CO	±1	LSB
MM.100X.COM.TM		J,A,S	$T_A = 25^{\circ}C$ $T_A = T_{MIN} \text{ to } T_{MAX}$		100 Y.C	±4 ±6	N
Gain Error (Note 2)		K,B,T	$T_A = 25^{\circ}C$ $T_A = T_{MIN} \text{ to } T_{MAX}$	WWW	.100 J.	±2 ±4	LSB
MMM.100 T. COM.	N	L,C,U	$T_A = 25^{\circ}C$ $T_A = T_{MIN} \text{ to } T_{MAX}$	WW	N.100	±1 ±3	WTI
Gain Temp. Coefficient (Note 2, 3)	TW	M.M. 100X	COM.TW	WW	±2	±70	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV _{DD} = ±5%	T _A = 25°C T _A = T _{MIN} to T _{MAX}	N.	0.001 0.001	0.02 0.04	%FSR/%
Output Leakage Current (OUTA)	M.IV	DAC A is 00000000	T _A = 25°C T _A = T _{MIN} to T _{MAX}	4	WWW.	±50 ±400	nA
Output Leakage Current (OUTB)	COM.T	DAC B is 00000000	T _A = 25°C T _A = T _{MIN} to T _{MAX}		MM	±50 ±400	nA
REFERENCE INPUT	·Mos	TW TIME	100 TOW.	« 1		IN .10	Z CC
R _{IN} (V _{REF} A, V _{REF} B)		IN W	N 100 Y. O.M.T	8	10	15	kΩ
V _{REF} A, V _{REF} B Input Resistance Match	A.CO	A.TW WW	W.100Y.COM			±1	%
DYNAMIC PERFORMANCE (N	Note 4)	WIN	MW.100 COM			TWW	Tan
Output Current Settling-Time to 1/2 LSB	1.700X.C	$\frac{DB0-DB7}{WR} = \frac{OV}{CS} = \frac{OV}{OV} $ OUTA = OUTB $\frac{DB0-DB7}{CS} = \frac{OV}{OV} $ OUTA = OUTB $\frac{DB0-DB7}{COV} = \frac{OV}{OV} $	T _A = 25°C T _A = T _{MIN} to T _{MAX}	M.TV M.TV	N	350 400	ns

ELECTRICAL CHARACTERISTICS—MX7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Co	entinued)	COM	TW		
Propagation Delay (from digital input to 90% of final analog output current)	MMM.	$\begin{array}{ll} \underline{DB0\text{-}DB7} = 0\text{V to V}_{DD} \text{ to 0V} \\ \overline{WR} = \overline{CS} = 0\text{V} \\ \text{OUTA} = \text{OUTB} \\ \text{Load} = 100\Omega, \\ C_{EXT} = 13\text{pF}; \end{array} \qquad \begin{array}{ll} T_{A} = 25^{\circ}\text{C} \\ T_{A} = T_{MIN} \text{ to } T_{MAX} \end{array}$	N.CO.	M.TV M.TV	220 270	ns
Digital to Analog Glitch Impulse	MMA	For code transition 00000000 to 11111111	100 Y.C	60	LM.	nV-se
AC Feedthrough (V _{REF} A to OUTA)	MA	$V_{REF}A = \pm 10V$ $100kHz$ Sinewave $V_{REF}B = 0V$ $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	N.1007		-70 -65	dB
AC Feedthrough (V _{REF} B to OUTB)	The state of the s	$V_{REF}B = \pm 10V$ $100kHz$ Sinewave $V_{REF}A = 0V$ $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	W.100	oy.cc	-70 -65	dB
Channel to Channel Isolation (V _{REF} A to OUTB)		V _{REF} A = ±10V 100kHz Sinewave V _{REF} B = 0V, both DACs loaded with 11111111		-90	COM.T	dB
Channel to Channel Isolation (V _{REF} B to OUTA)		V _{REF} B = ±10V 100kHz Sinewave V _{REF} A = 0V, both DACs loaded with 11111111	WWW	-90	CO_M	dB
Digital Crosstalk	LXX	Measured with code transition 0 to FS	WW	30	A'COA	nV-se
Harmonic Distortion	THD	V _{IN} = 6V rms @ 1kHz	-11/	-85	CO	dB
ANALOG OUTPUTS (Note 4)	1.17	W.100 - COM: 1	7	VW.10	0 ×	Mir
OUTA Capacitance	C _{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111	11	WW.	50 120	pF pF
OUTB Capacitance	Соитв	DAC latches loaded with 00000000 DAC latches loaded with 11111111		NWW	50 120	pF pF
DIGITAL INPUTS	COLL	N WWW. 100Y.CO. TW		MM.	100	Y.C.
Input High Voltage	V _{IH}	M MAN. CON.COM.	2.4	WW	14.2	V
Input Low Voltage	VIL	INW. Too COM.	N	**************************************	0.8	V
Input Current	J. JIN	T _A = 25°C T _A = T _{MIN} to T _{MAX}	W	N.	±1 ±10	μΑ
Input Capacitance (Note 4)	C _{IN}	DB0-DB7 WR, CS, DAC A/DAC B	TW		10 15	pF
POWER REQUIREMENTS	100 Y.C.	M. TW 1007.	TIN		W.	N 100
Supply Correct	V.100Y.C	Digital inputs V_{IL} or V_{IH} $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	M.TW	N.	1	mA
Supply Current	l _{DD}	Digital inputs 0V or V_{DD} $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	OM.1	W	100 500	μА
SWITCHING CHARACTERIST	TICS (Note	4) (See Timing Diagram)	COM	σW	1	MAN
Chip Select to Write Setup Time	t _{CS}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	200 230	LTW		ns
Chip Select to Write Hold Time	t _{CH}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	20 30			ns

Note 1: Specifications apply to both DACs in MX7528.

Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.

Note 3: Guaranteed, but not tested.

Note 4: These characteristics are for design guidance only and are not subject to test.

ELECTRICAL CHARACTERISTICS—MX7528, +5V Operation (Continued)

 $(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} \text{ to } T_{MAX} \text{ unless otherwise noted})$

PARAMETER	SYMBOL	CONDITIONS	MIN TYP	MAX UNITS
SWITCHING CHARACTER	RISTICS (Note	4) (See Timing Diagram) (Continued)	MITH	'
DAC Select to Write Setup Time	t _{AS}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	200 230	ns
DAC Select to Write Hold Time	t _{AH}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	20 30	ns
Write Pulse Width	t _{wR}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	180 200	ns
Data Setup Time	t _{DS}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	110 130	ns
Data Hold Time	t _{DH}	DOT: ONI.TH	N.100 0 OM.1	ns

ELECTRICAL CHARACTERISTICS—MX7528, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDI	MIN	TYP	MAX	UNITS	
DC ACCURACY (Note 1)	MIN	1100Y. COM.T	M. W.	1 100 X	Mon	IM	•
Resolution	WY	M. TODA CO.	LIN MM	8	Y.C.	ITW	Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U	TW WY	W.10	ON.CO	±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotoni	c Over Temp.	MAN	any.C	±1	LSB
WWW.1007.COM.1		J,A,S	T _A = 25°C T _A = T _{MIN} to T _{MAX}	WW.	1007.	±4 ±5	TW
Gain Error (Note 2)	ON	K,B,T	T _A = 25°C T _A = T _{MIN} to T _{MAX}	MM	N.100Y	±2 ±3	LSB
MM.100Y.COM	TIN	L,C,U	T _A = 25°C T _A = T _{MIN} to T _{MAX}	WV	W.100	±10	
Gain Temp. Coefficient (Note 2, 3)	WIN	WWW.100	N.COM.TW	W	±2	±35	ppm/°
Supply Rejection (Note 4)	PSR	ΔV _{DD} = ±5%	T _A = 25°C T _A = T _{MIN} to T _{MAX}	V	0.001 0.001	0.01 0.02	%FSR/
Output Leakage Current (OUTA)	COM.T.	DAC A is 00000000	T _A = 25°C T _A = T _{MIN} to T _{MAX}		WWV	±50 ±200	CnA
Output Leakage Current (OUTB)	COM	DAC B is 00000000	T _A = 25°C T _A = T _{MIN} to T _{MAX}		WW	±50 ±200	nA
REFERENCE INPUT	V.Co	IN WW	1100Y. ON.T	W	W	-xx1.1	001.
R _{IN} (V _{REF} A, V _{REF} B)	ox.COF	TW WY	1007.Co	8	10	15	kΩ
V _{REF} A, V _{REF} B Input Resistance Match	ON.CO	M.TW W	MM. 100A CON	TW		±1	%
DYNAMIC PERFORMANCE (Note 4)	WILLE	11007	1.77		MA	N.100
Output Current Settling-Time to 1/2 LSB	N.100X.	$\frac{DB0-DB7}{WR} = 0V \text{ to } V_{DD}$ $\frac{DB0-DB7}{WR} = 0V \text{ to } V_{DD}$ $OUTA = 0UTB$ $Load = 100\Omega,$ $C_{EXT} = 13pF;$	to 0V $T_{A} = 25^{\circ}C$ $T_{A} = T_{MIN} \text{ to } T_{MAX}$	M.TV OM.T	LM M	180 200	ns

ELECTRICAL CHARACTERISTICS—MX7528, +15V Operation (Continued)

 $(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} \text{ to } T_{MAX} \text{ unless otherwise noted})$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (N	Note 4) (Co	ntinued)	1 CON	TIN		
Propagation Delay (from digital input to 90% of final analog output current)	MMM.	$\begin{array}{ll} \underline{DB0\text{-}DB7} = 0V \text{ to } V_{DD} \text{ to } 0V \\ \overline{WR} = \overline{CS} = 0V \\ \text{OUTA} = \text{OUTB} \\ \text{Load} = 100\Omega, \\ C_{EXT} = 13pF; \end{array} \qquad \begin{array}{ll} T_A = 25^{\circ}C \\ T_A = T_{MIN} \text{ to } T_{MAX} \end{array}$	07.CO	M.TV OM.TV	80 100	ns
Digital to Analog Glitch Impulse	WW	For code transition 00000000 to 11111111		125		nV-se
AC Feedthrough (V _{REF} A to OUTA)	W	$V_{REF}A = \pm 10V$ $100kHz$ Sinewave $V_{REF}B = 0V$ $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	N.100	M.COJ	-70 -65	dB
AC Feedthrough (V _{REF} B to OUTB)		$V_{REF}B = \pm 10V$ $100kHz$ Sinewave $V_{REF}A = 0V$ $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	MAY 7	ooy.CC	-70 -65	dB
Channel to Channel Isolation (V _{REF} A to OUTB)	N	V _{REF} A = ±10V 100kHz Sinewave V _{REF} B = 0V, both DACs loaded with 11111111	WW.	-90		dB
Channel to Channel Isolation (V _{REF} B to OUTA)	N	V _{REF} B = ±10V 100kHz Sinewave V _{REF} A = 0V, both DACs loaded with 11111111		-90	COD	dB
Digital Crosstalk	LA	Measured with code transition 0 to FS	71	60	- c0	nV-se
Harmonic Distortion	THD	V _{IN} = 6V rms @ 1kHz		-85	01.	dB
ANALOG OUTPUTS (Note 4)	TW	MAM. OUN.CO. TAI	W	MAN	OOY.C	- A 1
OUTA Capacitance	C _{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111	1	MAN	50 120	pF pF
OUTB Capacitance	Соитв	DAC latches loaded with 00000000 DAC latches loaded with 11111111		MANA	50 120	pF pF
DIGITAL INPUTS	COM	M.Ing COM	1	TIN.	Witne	V CC
Input High Voltage	VIH	LAS M. 100 F. COW. I.	13.5		N.10	V
Input Low Voltage	V _{IL}	TH WY 100Y. ON.T	W		1.5	V
Input Current	IIN	T _A = 25°C T _A = T _{MIN} to T _{MAX}	TW	N	±1 ±10	μА
Input Capacitance (Note 4)	C _{IN}	DB0-DB7 WR, CS, DAC A/DAC B	ITW		10 15	pF
POWER REQUIREMENTS	TO C	OM. WANNIE ON CO.	TV		WW	M.
Supply Current	100X	Digital inputs V_{IL} or V_{IH} $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	MT	N	10	mA
Supply Current	I I _{DD}	Digital inputs 0V or V_{DD} $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	OM.	W	100 500	μΑ
SWITCHING CHARACTERIST	ICS (Note	4) (See Timing Diagram)	coM	T		MIN
Chip Select to Write Setup Time	t _{cs}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	60 80	LTW		ns
Chip Select to Write Hold Time	t _{CH}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	10 15	MIT	V	ns

Note 1: Specifications apply to both DACs in MX7528.

Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.

Note 3: Guaranteed but not tested

Note 3: Guaranteed, but not tested.

Note 4: These characteristics are for design guidance only and are not subject to test.

ELECTRICAL CHARACTERISTICS—MX7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP	MAX UNITS
SWITCHING CHARACTER	RISTICS (Note	4) (See Timing Diagram) (Continued)	M.T.W	
DAC Select to Write Setup Time	t _{AS}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	60 80	ns
DAC Select to Write Hold Time	t _{AH}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	10 15	ns
Write Pulse Width	t _{wa}	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	60 80	ns
Data Setup Time	t _{DS}	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	30 40	ns
Data Hold Time	t _{DH}	001. COM: IA. 10.	0	ns

ELECTRICAL CHARACTERISTICS—MX7628, +12V to +15V Operation

 $(V_{DD} = +10.8V \text{ to } +15.75V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} \text{ to } T_{MAX} \text{ unless otherwise noted})$

PARAMETER	SYMBOL	CONDI	MIN	TYP	MAX	UNITS	
DC ACCURACY (Note 1)	WW	1007.001.	M. M.	100%	Mo.	TW	
Resolution	WV	M. COL	LIN MIN	8	I.Co	WIT	Bits
Relative Accuracy	INL	MM. In COM.	TW WY	N.z	A'COD	±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotoni	c Over Temp.	M.In.	~ CO	±1	LSB
Gain Error (Note 2)		T _A = 25°C T _A = T _{MIN} to T _{MAX}	ALL MA	WW.I	OOY.C	±2 ±3	LSB
Gain Temp. Coefficient (Note 2, 3)		WWW.100Y.CC	OW.TW Y		±2	±35	ppm/° C
Supply Rejection (Note 4)	PSR	ΔV _{DD} = ±5%	T _A = 25°C T _A = T _{MIN} to T _{MAX}	MAL	0.001 0.001	0.01 0.02	%FSR/%
Output Leakage Current (OUTA)	TW	DAC A is 00000000	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	WV	W.100	±50 ±200	nA
Output Leakage Current (OUTB)	MIN	DAC B is 00000000	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}	W	NW.1	±50 ±200	nA
REFERENCE INPUT	WILLE	10	DY. CONT.TW		TAN.	100 1.	COM.
R _{IN} (V _{REF} A, V _{REF} B)		WWW	OOY.CO SALTY	8	10	15	kΩ
V _{REF} A, V _{REF} B Input Resistance Match	COM.T	M MMM.	100Y.COM.TW		MMA	±10	%
DYNAMIC PERFORMANCE (Note 4)	IN W	N 100 Y. OM.TV		All a	J.W.10	0
Output Current Settling-Time to 1/2 LSB	OX.COM	$\frac{DB0-DB7}{WR} = \frac{CS}{CS} = 0V$ OUTA = OUTB Load = $\frac{100\Omega}{CEXT}$	T to 0V $T_A = 25^{\circ}C$ $T_A = T_{MIN} \text{ to } T_{MAX}$	N TW TW	N	350 400	ns
Digital to Analog Glitch Impulse	100X.Ce	For code transition 00	0000000 to 11111111	LTY	125	WW	nV-sec
AC Feedthrough (V _{REF} A to OUTA)	A.100A.	V _{REF} A = ±10V 100kHz Sinewave V _{REF} B = 0V	T _A = 25°C T _A = T _{MIN} to T _{MAX}	oM.T	N	-70 -65	dB

Note 1: Specifications apply to both DACs in MX7628.

Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{RFF}.

Note 3: Guaranteed, but not tested.

Note 4: These characteristics are for design guidance only and are not subject to test.

ELECTRICAL CHARACTERISTICS—MX7628, +12V to +15V Operation (Continued) $(V_{DD} = +10.8V \text{ to } +15.75V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} \text{ to } T_{MAX} \text{ unless otherwise noted)}$

PARAMETER	SYMBOL		DITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Co		1/1/1/1007	M	TW		1
AC Feedthrough (V _{REF} B to OUTB)	WW.1	$V_{REF}B = \pm 10V$ 100kHz Sinewave $V_{REF}A = 0V$	T _A = 25°C T _A = T _{MIN} to T _{MAX}	Y.CO	M.TW	-70 -65	dB
Channel to Channel Isolation (V _{REF} A to OUTB)	WWW.	V _{REF} A = ±10V 100k V _{REF} B = 0V, both D	Hz Sinewave ACs loaded with 11111111	OV.CC	-90	N	dB
Channel to Channel Isolation (V _{REF} B to OUTA)	MM	V _{REF} B = ±10V 100k V _{REF} A = 0V, both D	Hz Sinewave ACs loaded with 11111111	1001	-90	W.	dB
Digital Crosstalk		Measured with code	e transition 0 to FS	100	60	·	nV-sec
Harmonic Distortion	THD	V _{IN} = 6V rms @ 1kl	Hz	N.100	-85	Vira	dB
ANALOG OUTPUTS (Note 4)	W.	M. 1007.Co.	WIN WW	1100	N.C.	MIN	
OUTA Capacitance	C _{OUTA}	DAC latches loaded DAC latches loaded		NW.10	10Y.Co	25 60	pF pF
OUTB Capacitance	Соитв	DAC latches loaded DAC latches loaded		WW.	007.	25 60	pF pF
DIGITAL INPUTS	- 1	MAIN	COM	NWW	To OA	COAr	TW
Input High Voltage	V _{IH}	A. 100.	COM.	2.4	V.Ino.	CON	V
Input Low Voltage	V _{IL}	MAI 100	I.O.M.TW	MA	W.100	0.8	V
Input Current	I	T _A = 25°C T _A = T _{MIN} to T _{MAX}	DY.COM.TW		NW.10	±1 ±10	μА
Input Capacitance (Note 4)	C _{IN}	DB0-DB7				10 15	pF
POWER REQUIREMENTS	OMP.	MW.	CON CON		MANA	YOUN	Co
Supply Current	I _{DD}	Digital inputs V _{IL} or V _{IH}	$T_A = 25^{\circ}C$ $T_A = T_{MIN} \text{ to } T_{MAX} K$ $T_A = T_{MIN} \text{ to } T_{MAX} B,T$		WWW	2 2 2.5	mA
WWW.100	.com	Digital inputs 0V or V _{DD}	T _A = 25°C T _A = T _{MIN} to T _{MAX}	N	WV	100 500	μΑ
SWITCHING CHARACTERIST	ICS (Note	4) (See Timing Diagr	am)	W	W	1	1001.
Chip Select to Write Setup Time	t _{cs}	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX} $T_A = T_{MIN}$ to T_{MAX}	K,B	160 160 210		MMA	ns
Chip Select to Write Hold Time	t _{CH}	OM. TW	WWW.100Y.CO	10		WW	ns
DAC Select to Write Setup Time	t _{AS}	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX} $T_A = T_{MIN}$ to T_{MAX}	K,B	160 160 210	M	W	ns
DAC Select to Write Hold Time	t _{AH}	Y.COM.TW	WW.100X	10	TW		ns
Write Pulse Width	t _{WR}	$T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX} $T_A = T_{MIN}$ to T_{MAX}	K,B T	150 170 210	W.TW	s1	ns
Data Setup Time	t _{DS}	$T_A = 25^{\circ}C$ $T_A = T_{MIN} \text{ to } T_{MAX}$ $T_A = T_{MIN} \text{ to } T_{MAX}$	K,B T	160 160 210	$_{\rm U,WC}$	N	ns
Data Hold Time	t _{DH}	1007.	UN MAN	10			ns

Interface Logic Information

DAC Selection

Both DAC latches <u>share</u> a common 8-Bit input port. The control input DAC A/DAC B selects which DAC will accept data from the input port.

Mode Selection

The inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table.

Mode Selection Table

DAC A/DAC B	CS	WR	DAC A	DAC B
COME	L	L	WRITE	HOLD
COH	L	L	HOLD	WRITE
X	Н	X	HOLD	HOLD
X	Х	H	HOLD	HOLD

L = Low state, H = High state, X = Don't care

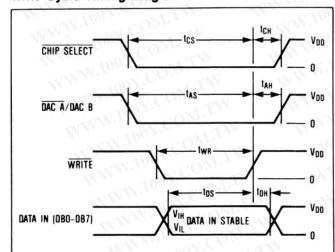
Write Mode

When \overline{CS} and \overline{WR} are both low, the selected DAC is in the write mode. The input latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0-DB7.

Hold Mode

The selected DAC latch retains the data that was present on DB0-DB7 just prior to CS or WR assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Write Cycle Timing Diagram



Note 1: For the MX7528, all input signal rise and fall times are measured from 10% to 90% of V_{DD} . V_{DD} = +5V, t_r = t_f = 20ns; V_{DD} = +15V, t_r = t_f = 40ns.

Note 2: For the MX7628, all input signal rise and fall times are measured from 10% to 90% of +5V. t_r = t_f = 20ns; V_{DD} = +10.8V to +15.75V.

Note 3: Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Detailed Description

The MX7528/MX7628 contains two identical 8-Bit multiplying digital-to-analog converters (DAC). Each DAC circuit consists of a thin-film R-2R resistor array with CMOS current steering switches. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at the OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The DAC OUT and analog ground terminals must be maintained at the same potential for proper operation.

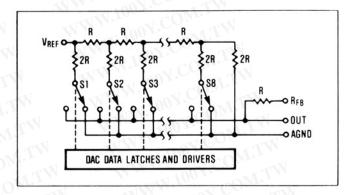


Figure 1. Simplified DAC Schematic

Equivalent-Circuit Analysis

The DAC equivalent-circuit, typical of both DACs, is shown in figure 2. Each DAC shares the analog ground pin 1. When all the digital inputs are high, 255/256 of the reference current flows to OUT A. A small junction leakage current ($I_{LEAKAGE}$), which doubles every 10° C, also flows to the output. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF} . C_{OUT} is the parallel combination of the capacitance associated with the individual NMOS current steering switches. The value of output capacitance is input code dependent and lies in the range 20pF to 30pF. The equivalent output resistance, R_{O} , also varies with input code in the range 0.8R to 3R, where R is the nominal ladder resistance.

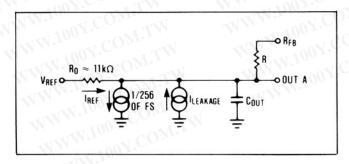


Figure 2. DAC Equivalent Circuit. All Digital Inputs High

Circuit Information—Digital Section

The MX7528's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region of 1.0 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

The MX7528 may be operated with any supply voltage in the range 5V < V $_{\rm DD}$ < 15V. With V $_{\rm DD}$ = +15V, the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The MX7628's digital inputs are TTL and CMOS compatible with any supply voltage in the range of +12V to +15V.

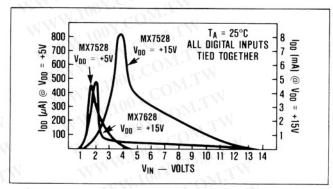


Figure 3. Typical Plots of Supply Current, IDD vs. Logic Input Voltage V_{IN} , for $V_{DD} = +5V$ and +15V

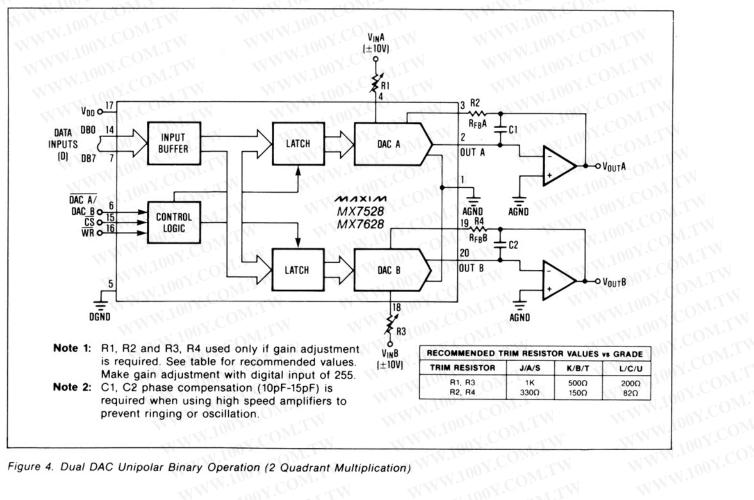


Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication)

Applications Information

To ensure system performance consistent with the MX7528/MX7628 specifications, careful attention must be given to the following points:

1. General Ground Management:

AC or transient voltages between the MX7528/MX7628 AGND and DGND can cause noise injection into the analog output. Therefore, whenever possible, the analog and digital ground pins should be tied together at the MX7528/MX7628.

2. Output Amplifier Offset:

CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The result is a code-dependent differential nonlinearity term at the amplifier output which depends on the amplifier's offset voltage, V_{OS}. The offset dependent nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier offset voltage should be no more than 1/10 LSB over the operating temperature range.

3. High Frequency Considerations:

The combination of DAC output capacitance and the amplifier's feedback resistance adds a pole to the open-loop response which can cause ringing or oscillation in severe cases. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

4. Dynamic Performance:

The dynamic performance of the two DACs in the MX7528/MX7628 depends on the gain and phase

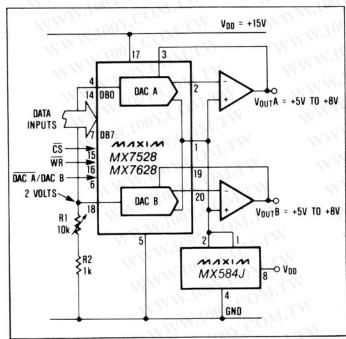


Figure 5. MX7528/MX7628 Single Supply Operation

characteristics of the output amplifiers, together with the stray capacitance contributed by the PC layout, and the power supply decoupling components. A $0.1\mu F$ decoupling capacitor is recommended between V_{DD} and DGND.

5. Circuit Layout Suggestions:

Analog and digital ground traces should be routed between the package pins to reduce coupling between the digital inputs and the analog output. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, and 4-5 to minimize reference feedthrough to the output in multiplying applications.

Single Supply Operation

The MX7528/MX7628 R-2R ladder termination resistors are internally connected to AGND. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between V_{DD} and DGND. Figure 5 shows a circuit which provides dual +5V to +8V analog outputs by biasing AGND 5V above DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the stable matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1, and R1 is adjusted until V_{REF}A and V_{REF}B inputs are at +2V. DAC codes from 000000000 to 111111111 adjust the analog output voltages from +5V to +8V in 11.7mV steps.

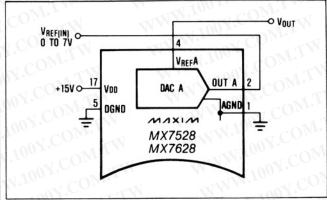


Figure 6. MX7528/MX7628 in Single Supply, Voltage Switching Mode

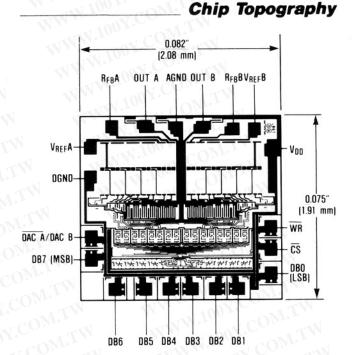
Figure 6 shows one DAC of the MX7528/MX7628 connected in the voltage switching mode which uses a positive reference voltage. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to maintain linearity, V_{IN} must be limited to approximately +7V (V_{DD} = +15V), and the output must be buffered or loaded with a high impedance. In the voltage switching mode, the output resistance is independent of the digital input code and is typically $10k\Omega$.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7528KEPP	-40°C to +85°C	Plastic DIP	±1/2 LSB
MX7528LEPP	-40°C to +85°C	Plastic DIP	±1/2 LSB
MX7528KEWP	-40°C to +85°C	Wide SO	±1/2 LSB
MX7528LEWP	-40°C to +85°C	Wide SO	±1/2 LSB
MX7528SD	-55°C to +125°C	Ceramic	±1 LSB
MX7528TD	-55°C to +125°C	Ceramic	±1/2 LSB
MX7528UD	-55°C to +125°C	Ceramic	±1/2 LSB
MX7528SQ	-55°C to +125°C	CERDIP**	±1 LSB
MX7528TQ	-55°C to +125°C	CERDIP**	±1/2 LSB
MX7528UQ	-55°C to +125°C	CERDIP**	±1/2 LSB
MX7628KN	0°C to +70°C	Plastic DIP	±1/2 LSB
MX7628KCWP	0°C to +70°C	Wide SO	±1/2 LSB
MX7628KC/D	0°C to +70°C	Dice	±1/2 LSB
MX7628BQ	-25°C to +85°C	CERDIP	±1/2 LSB
MX7628TQ	-55°C to +125°C	CERDIP	±1/2 LSB
			W. W. A

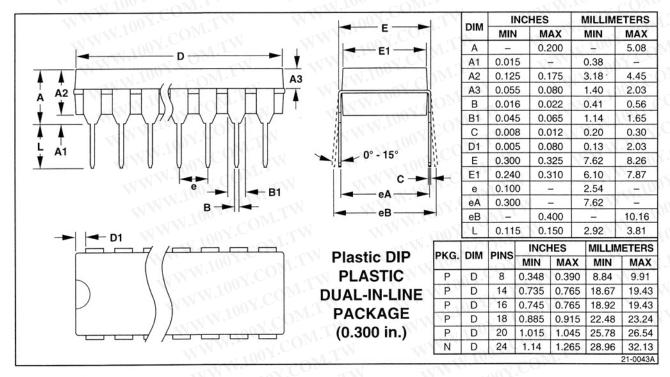
^{*} All devices - 20 lead packages

Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages



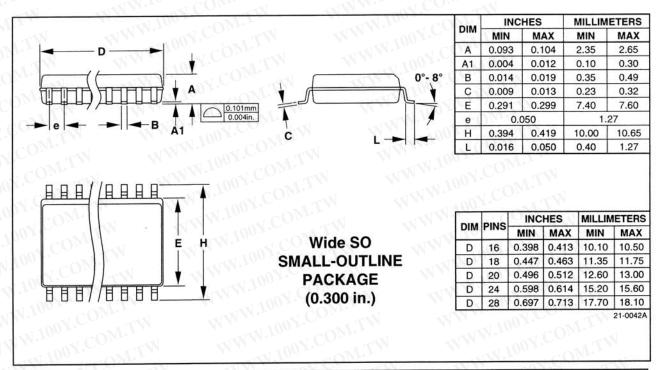
Package Information

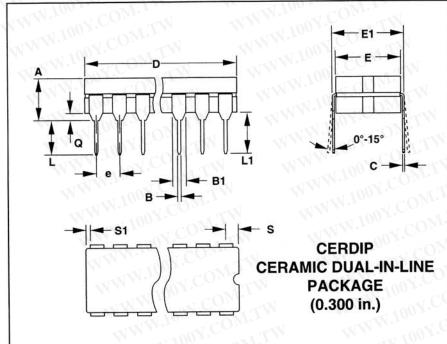
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
Α	-	0.200	Cally	5.08
В	0.014	0.023	0.36	0.58
В1	0.038	0.065	0.97	1.65
С	0.008	0.015	0.20	0.38
Е	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
е	0.1	00	2.54	
L	0.125	0.200	3.18	5.08
L1	0.150		3.81	
Q	0.015	0.070	0.38	1.78
S		0.098	1.12	2.49
S1	0.005		0.13	1 - 2

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	-	0.405	-	10.29
D	14	-	0.785		19.94
D	16	-	0.840	-	21.34
D	18	1-1	0.960	TV	24.38
D	20	-	1.060	-	26.92
D	24	\ -	1.280	14	32.51
	1.1				21-0045A

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600