MCP4728

12-Bit, Quad Digital-to-Analog Converter with EEPROM Memory

Features

- 12-Bit Voltage Output DAC with 4 Buffered Outputs
- On-Board Non-Volatile Memory (EEPROM) for DAC Codes and I^2C^{TM} Address Bits
- Internal or External Voltage Reference Selection
- Output Voltage Range:
  - Using Internal V_{REF} (2.048V):
    0.000V to 2.048V with Gain Setting = 1
    0.000V to 4.096V with Gain Setting = 2
  - Using External V_{REF} (V_{DD}): 0.000V to V_{DD}
- ±0.2 LSB DNL (typical)
- Fast Settling Time: 6 µs (typical)
- Normal or Power-Down Mode
- Low Power Consumption
- Single-Supply Operation: 2.7V to 5.5V
- I^2C Interface:
  - Address bits: User Programmable to EEPROM
  - Standard (100 kbps), Fast (400 kbps) and High Speed (3.4 Mbps) Modes
- 10-Lead MSOP Package
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Adjustment
- Sensor Calibration
- Closed-Loop Servo Control
- Low Power Portable Instrumentation
- PC Peripherals
- Programmable Voltage and Current Source
- Industrial Process Control
- Instrumentation

Description

The MCP4728 device is a quad, 12-bit voltage output Digital-to-Analog Convertor (DAC) with non-volatile memory (EEPROM). Its on-board precision output amplifier allows it to achieve rail-to-rail analog output swing.

The DAC input codes, device configuration bits, and I^2C address bits are programmable to the non-volatile memory (EEPROM) by using I^2C serial interface commands. The non-volatile memory feature enables the DAC device to hold the DAC input codes during power-off time, allowing the DAC outputs to be available immediately after power-up with the saved settings. This feature is very useful when the DAC device is used as a supporting device for other devices in applications network.

The MCP4728 device has a high precision internal voltage reference (V_{REF} = 2.048V). The user can select the internal reference or external reference (V_{DD}) for each channel individually.

Each channel can be operated in normal mode or power-down mode individually by setting the configuration register bits. In power-down mode, most of the internal circuits in the powered down channel are turned off for power-savings and the output amplifier can be configured to present a known low, medium, or high resistance output load.

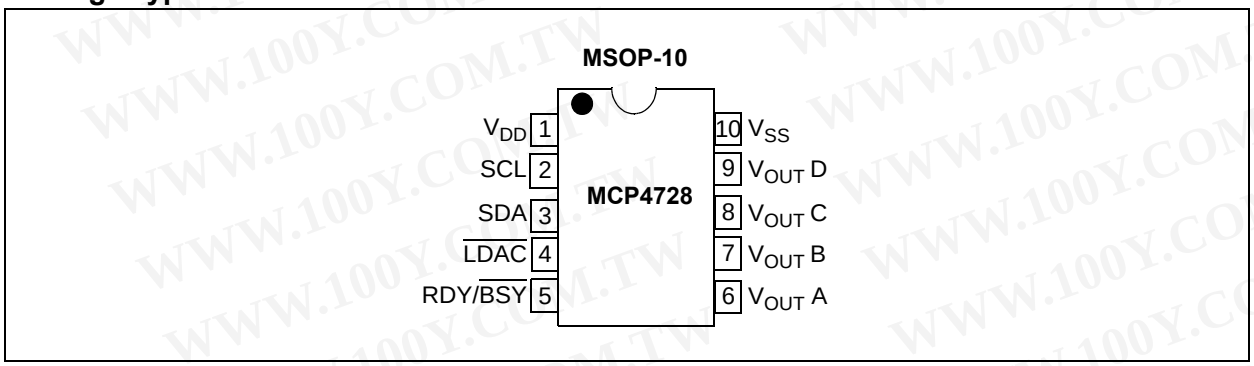
The MCP4728 device includes a Power-On-Reset (POR) circuit to ensure reliable power-up and an on-board charge pump for the EEPROM programming voltage.

The MCP4728 has a two-wire I^2C compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

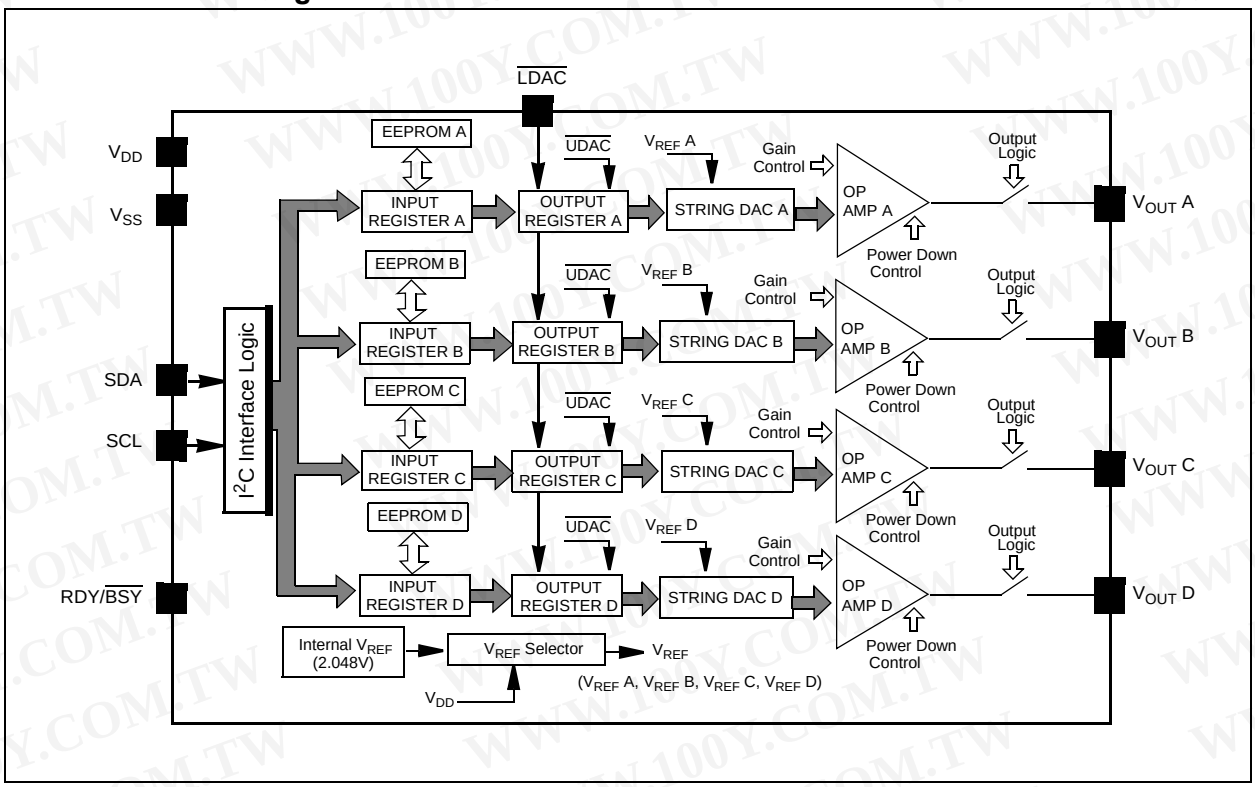
The MCP4728 DAC is an ideal device for applications requiring design simplicity with high precision, and for applications requiring the DAC device settings to be saved during power-off time.

The MCP4728 device is available in a 10-lead MSOP package and operates from a single 2.7V to 5.5V supply voltage.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....6.5V
All inputs and outputs w.r.t V_{SS} .....–0.3V to V_{DD}+0.3V
Current at Input Pins .....±2 mA
Current at Supply Pins .....±110 mA
Current at Output Pins .....±25 mA
Storage Temperature .....-65°C to +150°C
Ambient Temp. with Power Applied .....-55°C to +125°C
ESD protection on all pins .....≥ 4 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T_J) .....+150°C

† Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, V_{IH} = V_{DD}, V_{IL} = V_{SS}.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Supply Current with External Reference (V_{REF} = V_{DD}) **(Note 1)**	I_{DD_EXT}	—	800	1400	µA	V_{REF} = V_{DD}, V_{DD} = 5.5V All 4 channels are in normal mode.
		—	600	—	µA	3 channels are in normal mode, 1 channel is powered down.
		—	400	—	µA	2 channels are in normal mode, 2 channel are powered down.
		—	200	—	µA	1 channel is in normal mode, 3 channels are powered down.
Power-Down Current with-External Reference	I_{PD_EXT}	—	40	—	nA	All 4 channels are powered down. (V_{REF} = V_{DD})
Supply Current with Internal Reference (V_{REF} = Internal) **(Note 1)**	I_{DD_INT}	—	800	1400	µA	V_{REF} = Internal Reference V_{DD} = 5.5V All 4 channels are in normal mode.
		—	600	—	µA	3 channels are in normal mode, 1 channel is powered down.
		—	400	—	µA	2 channels are in normal mode, 2 channels are powered down.
		—	200	—	µA	1 channel is in normal mode, 3 channels are powered down.
Power-Down Current with Internal Reference	I_{PD_INT}	—	45	60	µA	All 4 channels are powered down. V_{REF} = Internal Reference

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to “High”, Output pins are unloaded, code = 0x000.
2: The power-up ramp rate measures the rise of V_{DD} over time.
3: This parameter is ensured by design and not 100% tested.
4: This parameter is ensured by characterization and not 100% tested.
5: Test code range: 100 - 4000 codes, V_{REF} = V_{DD}, V_{DD} = 5.5V.
6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.
7: This parameter is indirectly tested by Offset and Gain error testing.
8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.
9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, V_{IH} = V_{DD}, V_{IL} = V_{SS}.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Power-On-Reset Threshold Voltage	V_{POR}	—	2.2	—	V	All circuits including EEPROM are ready to operate.
Power-Up Ramp Rate	V_{RAMP}	1	—	—	V/s	**Note 2**, **Note 4**
DC Accuracy						
Resolution	n	12	—	—	Bits	Code Change: 000h to FFFh
INL Error	INL	—	±2	±13	LSB	**(Note 5)**
DNL Error	DNL	-0.75	±0.2	±0.75	LSB	**(Note 5)**
Offset Error	V_{OS}	—	0.02	0.75	% of FSR	Code = 000h
Offset Error Drift	ΔV_{OS}/°C	—	±0.16	—	ppm/°C	-45°C to 25°C
		—	±0.44	—	ppm/°C	+25°C to +125°C
Gain Error	G_E	-3	-0.1	3	% of FSR	V_{REF} = Internal, Gain = x1 Code = FFFh, Offset error is not included.
		-3	-0.1	3	% of FSR	V_{REF} = Internal, Gain = x2 Code = FFFh, Offset error is not included.
		-2	-0.1	2	% of FSR	V_{REF} = V_{DD} Code = FFFh, Offset error is not included.
Gain Error Drift	ΔG_E/°C	—	-3	—	ppm/°C	
Internal Voltage Reference (V_{REF}), (Note 3)						
Internal Voltage Reference	V_{REF}	2.007	2.048	2.089	V	
Temperature Coefficient	ΔV_{REF}/°C	— —	125 0.25	— —	ppm/°C LSB/°C	-40 to 0°C -40 to 0°C
		— —	45 0.09	— —	ppm/°C LSB/°C	0 to +125°C 0 to +125°C
Reference Output Noise	E_{NREF}	—	290	—	μV_{p-p}	Code = FFFh, 0.1 - 10 Hz, G_X=1
Output Noise Density	e_{NREF}	—	1.2	—	$\mu V/\sqrt{Hz}$	Code = FFFh, 1 kHz, G_X=1
		—	1.0	—		Code = FFFh, 10 kHz, G_X=1
1/f Corner Frequency	f_{CORNER}	—	400	—	Hz	
Analog Output (Output Amplifier)						
Output Voltage Swing	V_{OUT}	—	FSR	—	V	**(Note 7)**

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to "High", Output pins are unloaded, code = 0x000.

2: The power-up ramp rate measures the rise of V_{DD} over time.

3: This parameter is ensured by design and not 100% tested.

4: This parameter is ensured by characterization and not 100% tested.

5: Test code range: 100 - 4000 codes, V_{REF} = V_{DD}, V_{DD} = 5.5V.

6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.

7: This parameter is indirectly tested by Offset and Gain error testing.

8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.

9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, V_{IH} = V_{DD}, V_{IL} = V_{SS}.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Full Scale Range **(Note 7)**	FSR	—	V_{DD}	—	V	V_{REF} = V_{DD} FSR = from 0.0V to V_{DD}
		—	V_{REF}	—	V	V_{REF} = Internal, G_X =1, FSR = from 0.0 V to V_{REF}
		—	2 * V_{REF}	—	V	V_{REF} = Internal, G_X =2, FSR = from 0.0V to 2*V_{REF}
Output Voltage Settling Time	$T_{SETTLING}$	—	6	—	µs	**(Note 8)**
Analog Output Time Delay from Power-Down Mode	Td_{EXPD}	—	4.5	—	µs	V_{DD} = 5V, **(Note 4)**, **(Note 9)**
Time delay to settle to new reference **(Note 4)**	Td_{REF}	—	26	—	µs	From External to Internal Reference
		—	44	—	µs	From Internal to External Reference
Power Supply Rejection	PSRR	—	-57	—	dB	V_{DD} = 5V± 10%, V_{REF} = Internal
Capacitive Load Stability	C_L	—	—	1000	pF	R_L = 5 kΩ, No Oscillation, **(Note 4)**
Slew Rate	SR	—	0.55	—	V/µs	
Phase Margin	p_M	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Short Circuit Current	I_{SC}	—	15	24	mA	V_{DD} = 5V, All V_{OUT} Pins = Grounded. Tested at room temperature.
Short Circuit Current Duration	T_{SC_DUR}	—	Infinite	—	hours	**(Note 4)**
DC Output Impedance **(Note 4)**	R_{OUT}	—	1	—	Ω	Normal mode
		—	1	—	kΩ	Power-Down Mode 1 (PD1:PD0 = 0:1), V_{OUT} to V_{SS}
		—	100	—	kΩ	Power-Down Mode 2 (PD1:PD0 = 1:0), V_{OUT} to V_{SS}
		—	500	—	kΩ	Power-Down Mode 3 (PD1:PD0 = 1:1), V_{OUT} to V_{SS}
Dynamic Performance (Note 4)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSB code change around major carry (from 7FFh to 800h)
Digital Feedthrough		—	<10	—	nV-s	
Analog Crosstalk		—	<10	—	nV-s	
DAC-to-DAC Crosstalk		—	<10	—	nV-s	

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to "High", Output pins are unloaded, code = 0x000.

2: The power-up ramp rate measures the rise of V_{DD} over time.

3: This parameter is ensured by design and not 100% tested.

4: This parameter is ensured by characterization and not 100% tested.

5: Test code range: 100 - 4000 codes, V_{REF} = V_{DD}, V_{DD} = 5.5V.

6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.

7: This parameter is indirectly tested by Offset and Gain error testing.

8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.

9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, V_{IH} = V_{DD}, V_{IL} = V_{SS}.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA SDA and RDY/$\overline{BSY}$ pins
Schmitt Trigger Low Input Threshold Voltage	V_{IL}	—	—	$0.3V_{DD}$	V	V_{DD} > 2.7V. SDA, SCL, $\overline{LDAC}$ pins
		—	—	$0.2V_{DD}$	V	$V_{DD} \leq$ 2.7V. SDA, SCL, $\overline{LDAC}$ pins
Schmitt Trigger High Input Threshold Voltage	V_{IH}	$0.7V_{DD}$	—	—	V	SDA, SCL, $\overline{LDAC}$ pins
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = $\overline{LDAC}$ = V_{DD}, SCL = SDA = $\overline{LDAC}$ = V_{SS}
Pin Capacitance	C_{PIN}	—	—	3	pF	**(Note 4)**
EEPROM						
EEPROM Write Time	TWRITE	—	25	50	ms	EEPROM write time
Data Retention		—	200	—	Years	At +25°C, **(Note 3)**
$\overline{LDAC}$ Input						
$\overline{LDAC}$ Low Time	$T_{\overline{LDAC}}$	210	—	—	ns	Updates analog outputs **(Note 3)**

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to "High", Output pins are unloaded, code = 0x000.

2: The power-up ramp rate measures the rise of V_{DD} over time.

3: This parameter is ensured by design and not 100% tested.

4: This parameter is ensured by characterization and not 100% tested.

5: Test code range: 100 - 4000 codes, V_{REF} = V_{DD}, V_{DD} = 5.5V.

6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.

7: This parameter is indirectly tested by Offset and Gain error testing.

8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.

9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

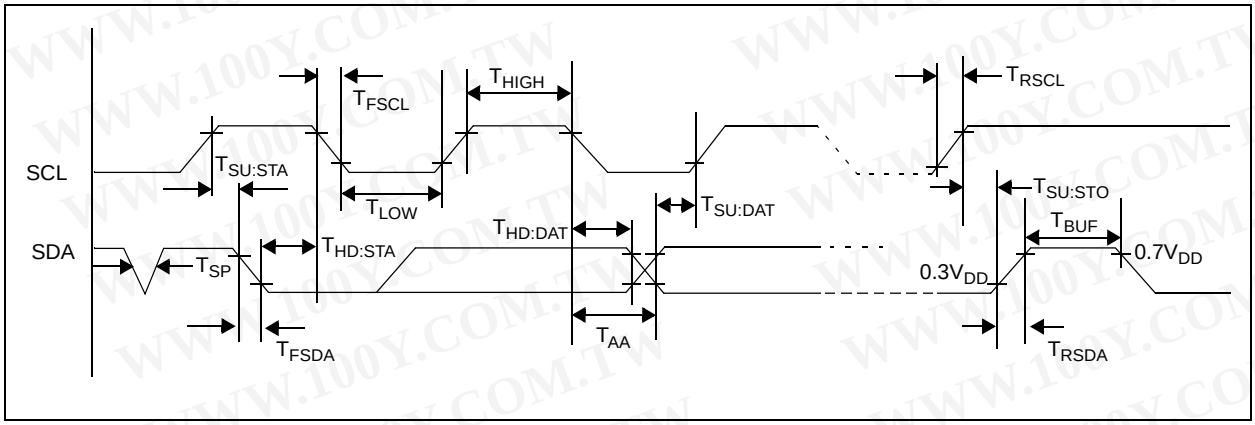


FIGURE 1-1: *I^2C Bus Timing Data.*

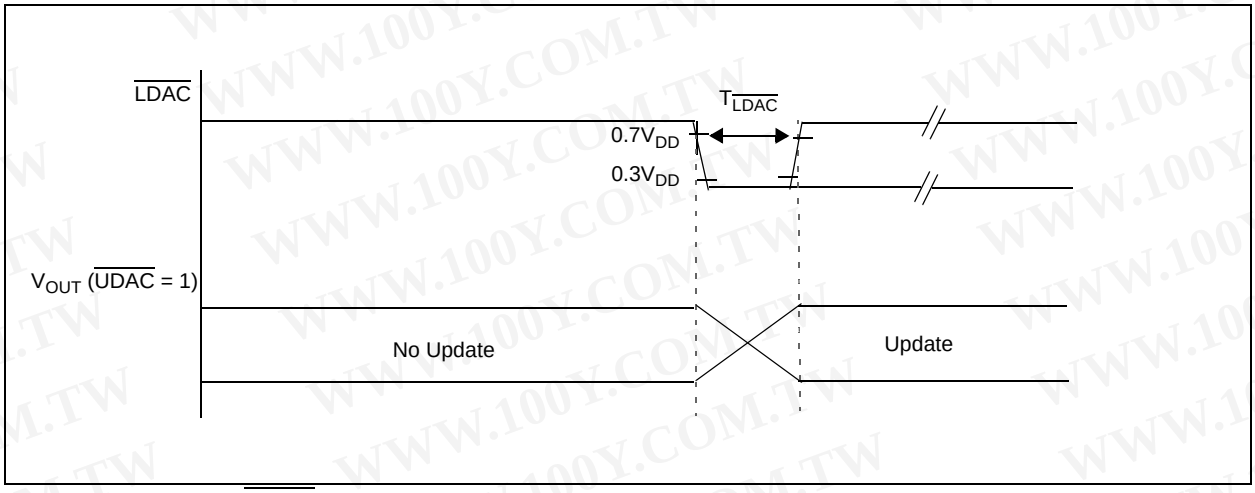


FIGURE 1-2: *$\overline{LDAC}$ Pin Timing vs. V_{OUT} Update.*

TABLE 1-2: I²C SERIAL TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +125°C, V_{SS} = 0V,
Standard and Fast Mode: V_{DD} = +2.7V to +5.5V
High Speed Mode: V_{DD} = +4.5V to +5.5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	f_{SCL}	0	—	100	kHz	Standard Mode C_b = 400 pF, 2.7V - 5.5V
		0	—	400	kHz	Fast Mode C_b = 400 pF, 2.7V - 5.5V
		0	—	1.7	MHz	High Speed Mode 1.7 C_b = 400 pF, 4.5V - 5.5V
		0	—	3.4	MHz	High Speed Mode 3.4 C_b = 100 pF, 4.5V - 5.5V
Bus Capacitive Loading	Cb	—	—	400	pF	Standard Mode 2.7V - 5.5V
		—	—	400	pF	Fast Mode 2.7V - 5.5V
		—	—	400	pF	High Speed Mode 1.7 4.5V - 5.5V
		—	—	100	pF	High Speed Mode 3.4 4.5V - 5.5V
Start Condition Setup Time (Start, Repeated Start)	$T_{SU:STA}$	4700		—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		160	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4
Start Condition Hold Time	$T_{HD:STA}$	4000		—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		160	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4
Stop Condition Setup Time	$T_{SU:STO}$	4000		—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		160	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4
Clock High Time	T_{HIGH}	4000	—	—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		120	—	—	ns	High Speed Mode 1.7
		60	—	—	ns	High Speed Mode 3.4
Clock Low Time	T_{LOW}	4700	—	—	ns	Standard Mode
		1300	—	—	ns	Fast Mode
		320	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4

Note 1: This parameter is ensured by characterization and is not 100% tested.

2: After a Repeated Start condition or an Acknowledge bit.

3: If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

4: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (OR T_{RSDA}).

5: Time between Start and Stop conditions.

TABLE 1-2: I²C SERIAL TIMING SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +125°C, V_{SS} = 0V,
Standard and Fast Mode: V_{DD} = +2.7V to +5.5V
High Speed Mode: V_{DD} = +4.5V to +5.5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
SCL Rise Time **(Note 1)**	T_{RSCL}	—	—	1000	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	80	ns	High Speed Mode 1.7
		20	—	160	ns	High Speed Mode 1.7 **(Note 2)**
		10	—	40	ns	High Speed Mode 3.4
		10	—	80	ns	High Speed Mode 3.4 **(Note 2)**
SDA Rise Time **(Note 1)**	T_{RSDA}	—	—	1000	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	80	ns	High Speed Mode 1.7
		10	—	40	ns	High Speed Mode 3.4
SCL Fall Time **(Note 1)**	T_{FSCL}	—	—	300	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	160	ns	High Speed Mode 1.7
		10	—	80	ns	High Speed Mode 3.4
SDA Fall Time **(Note 1)**	T_{FSDA}	—	—	300	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	160	ns	High Speed Mode 1.7
		10	—	80	ns	High Speed Mode 3.4
Data Input Setup Time	$T_{SU:DAT}$	250	—	—	ns	Standard Mode
		100	—	—	ns	Fast Mode
		10	—	—	ns	High Speed Mode 1.7
		10	—	—	ns	High Speed Mode 3.4
Data Hold Time (Input, Output) **(Note 3)**	$T_{HD:DAT}$	0	—	3450	ns	Standard Mode
		0	—	900	ns	Fast Mode
		0	—	70	ns	High Speed Mode 1.7
		0	—	150	ns	High Speed Mode 3.4
Output Valid from Clock **(Note 4)**	T_{AA}	0	—	3750	ns	Standard Mode
		0	—	1200	ns	Fast Mode
		0	—	150	ns	High Speed Mode 1.7
		0	—	310	ns	High Speed Mode 3.4
Bus Free Time **(Note 5)**	T_{BUF}	4700	—	—	ns	Standard Mode
		1300	—	—	ns	Fast Mode
		—	—	—	ns	High Speed Mode 1.7
		—	—	—	ns	High Speed Mode 3.4
Input Filter Spike Suppression (SDA and SCL) **(Not Tested)**	T_{SP}	—	—	—	ns	Standard Mode, (Not Applicable)
		—	50	—	ns	Fast Mode
		—	10	—	ns	High Speed Mode 1.7
		—	10	—	ns	High Speed Mode 3.4

Note 1: This parameter is ensured by characterization and is not 100% tested.

2: After a Repeated Start condition or an Acknowledge bit.

3: If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

4: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (OR T_{RSDA}).

5: Time between Start and Stop conditions.

TABLE 1-3: TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Symbol**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

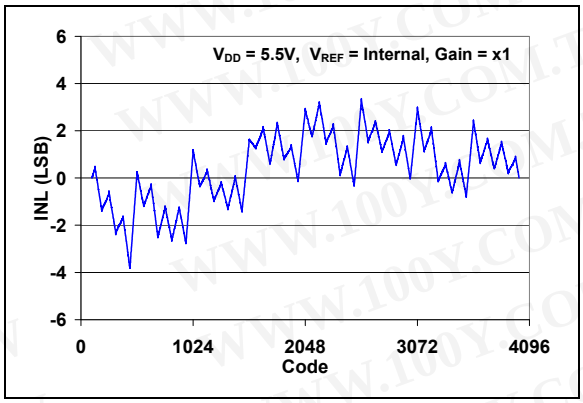


FIGURE 2-1: *INL vs. Code (T_A = +25°C).*

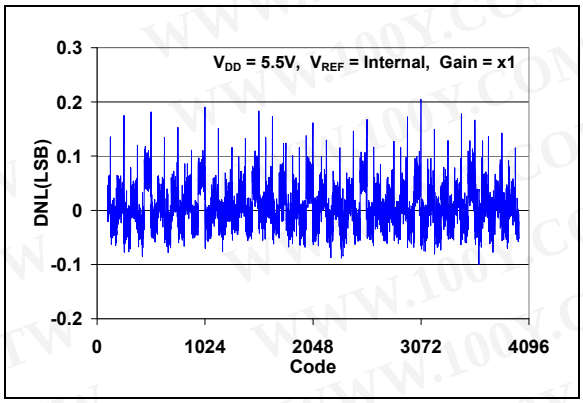


FIGURE 2-4: *DNL vs. Code (T_A = +25°C).*

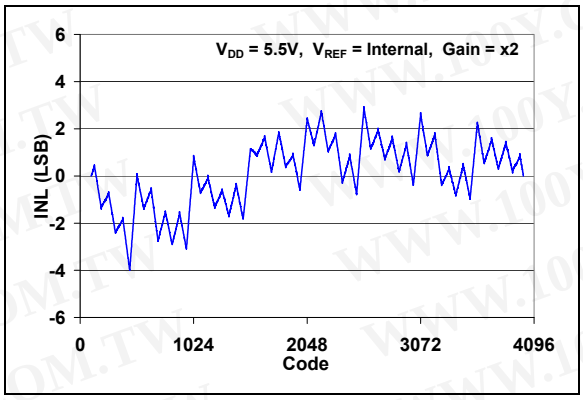


FIGURE 2-2: *INL vs. Code (T_A = +25°C).*

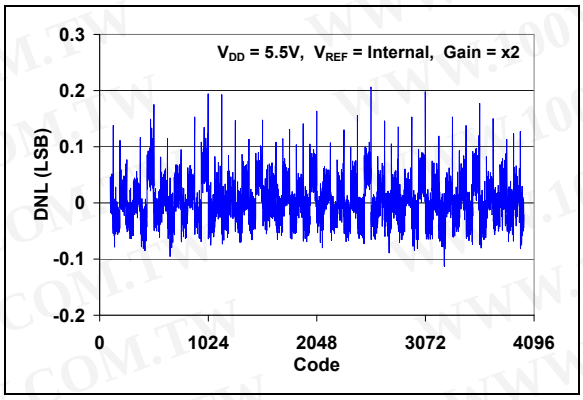


FIGURE 2-5: *DNL vs. Code (T_A = +25°C).*

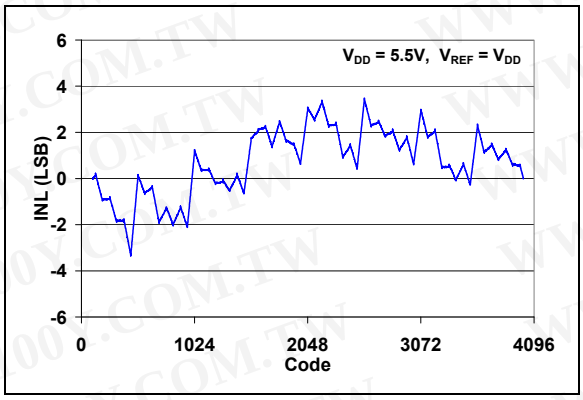


FIGURE 2-3: *INL vs. Code (T_A = +25°C).*

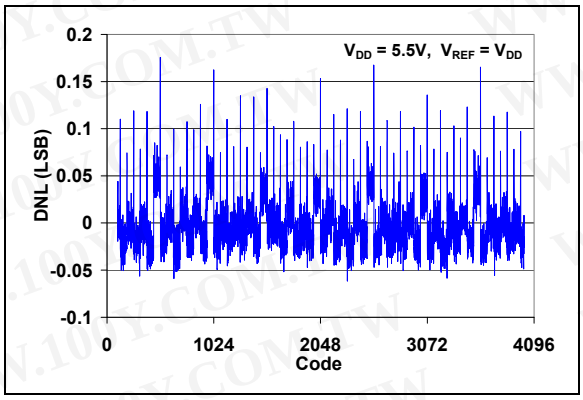


FIGURE 2-6: *DNL vs. Code (T_A = +25°C).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

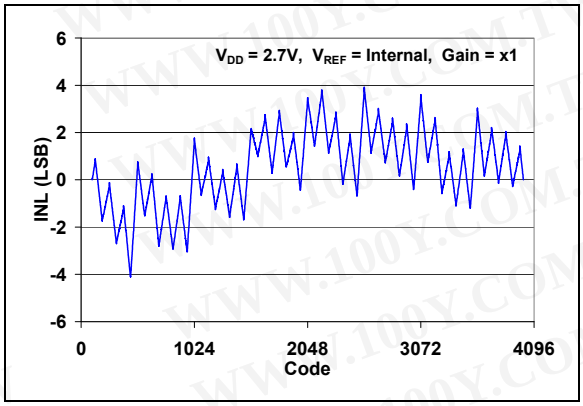


FIGURE 2-7: *INL vs. Code (T_A = +25°C).*

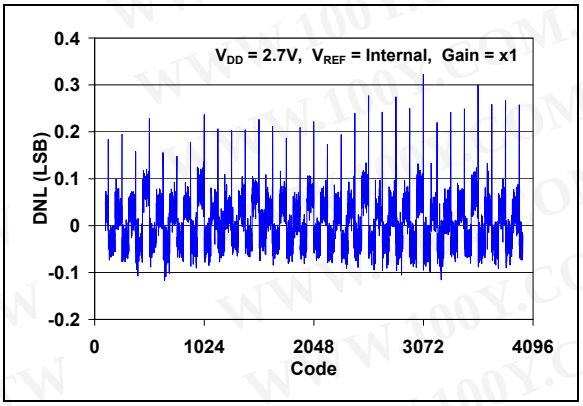


FIGURE 2-10: *DNL vs. Code (T_A = +25°C).*

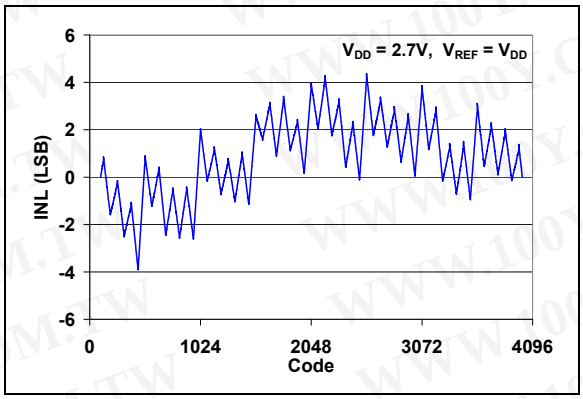


FIGURE 2-8: *INL vs. Code (T_A = +25°C).*

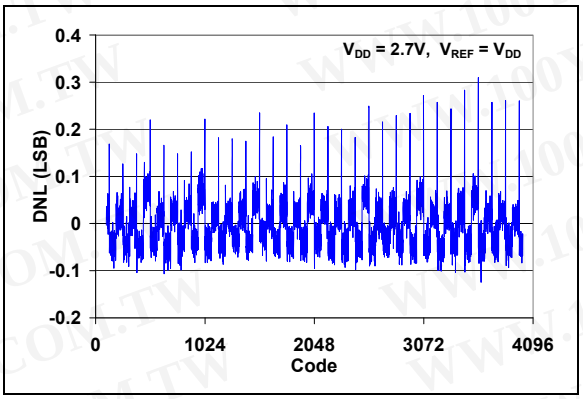


FIGURE 2-11: *DNL vs. Code (T_A = +25°C).*

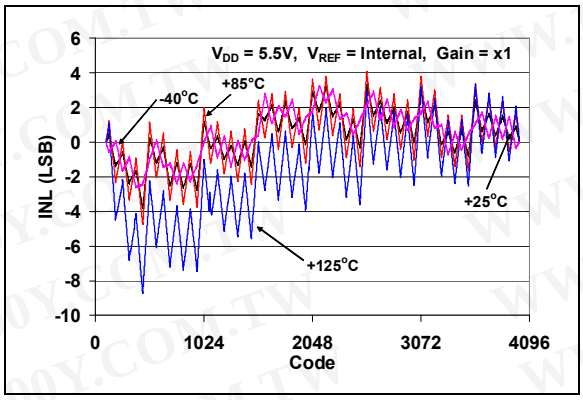


FIGURE 2-9: *INL vs. Code and Temperature.*

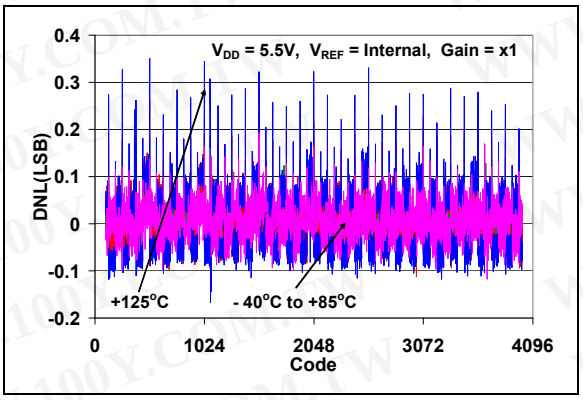


FIGURE 2-12: *DNL vs. Code and Temperature.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

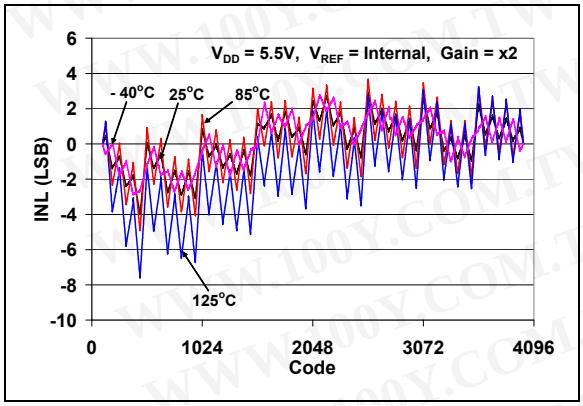


FIGURE 2-13: *INL vs. Code and Temperature.*

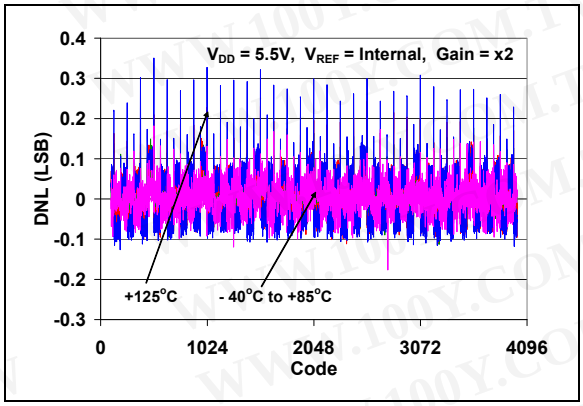


FIGURE 2-16: *DNL vs. Code and Temperature.*

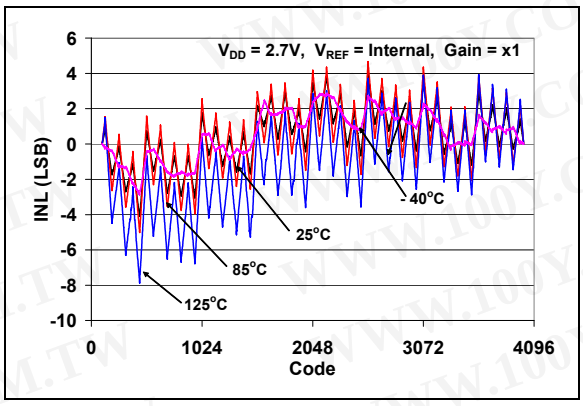


FIGURE 2-14: *INL vs. Code and Temperature.*

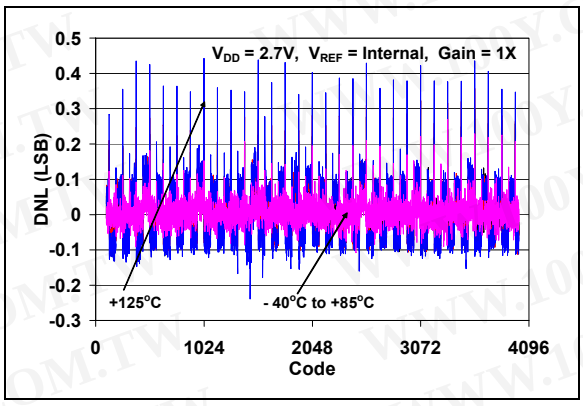


FIGURE 2-17: *DNL vs. Code and Temperature.*

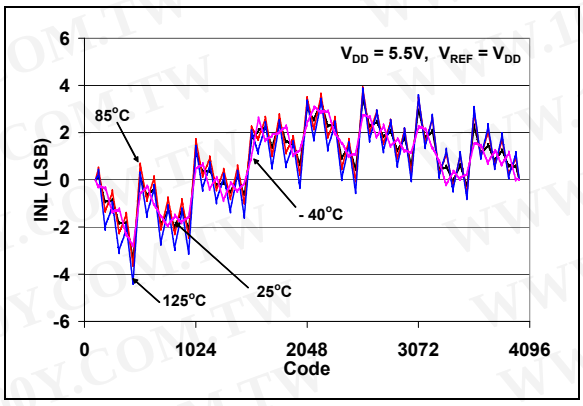


FIGURE 2-15: *INL vs. Code and Temperature.*

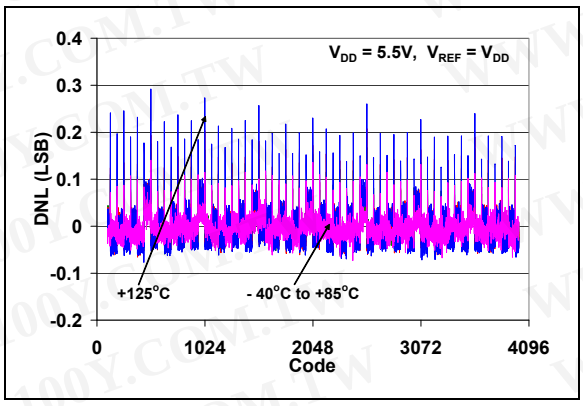


FIGURE 2-18: *DNL vs. Code and Temperature.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

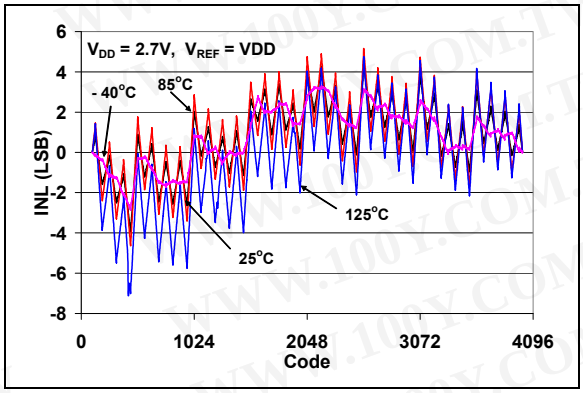


FIGURE 2-19: *INL vs. Code and Temperature.*

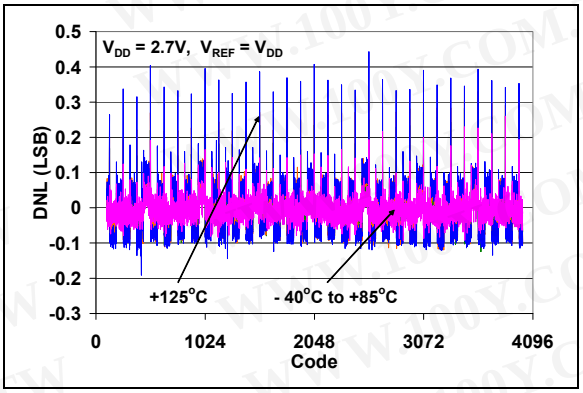


FIGURE 2-22: *DNL vs. Code and Temperature.*

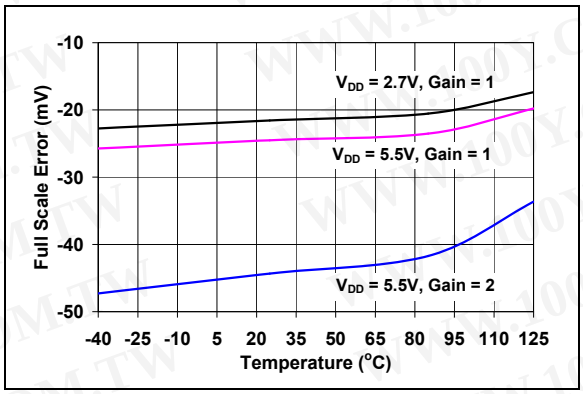


FIGURE 2-20: *Full Scale Error vs. Temperature (Code = FFFh, V_{REF} = Internal).*

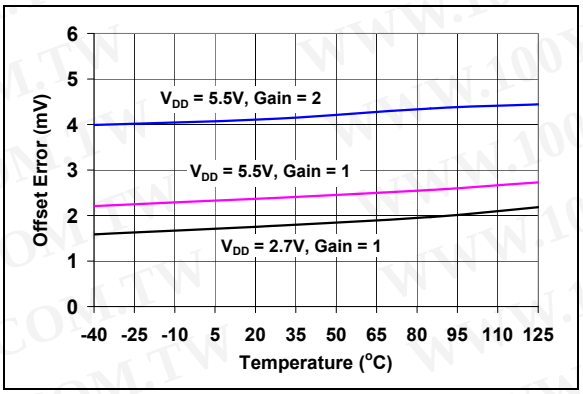


FIGURE 2-23: *Zero Scale Error vs. Temperature (Code = 000h, V_{REF} = Internal).*

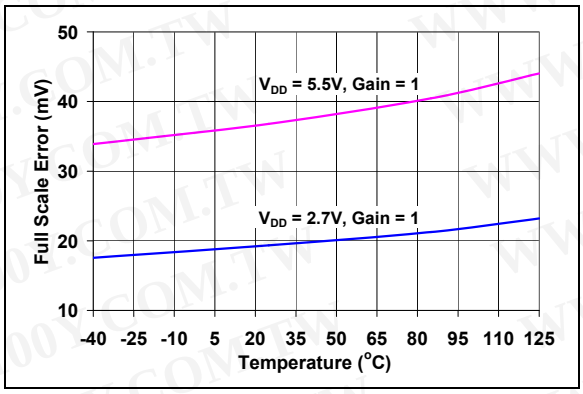


FIGURE 2-21: *Full Scale Error vs. Temperature (Code = FFFh, V_{REF} = V_{DD}).*

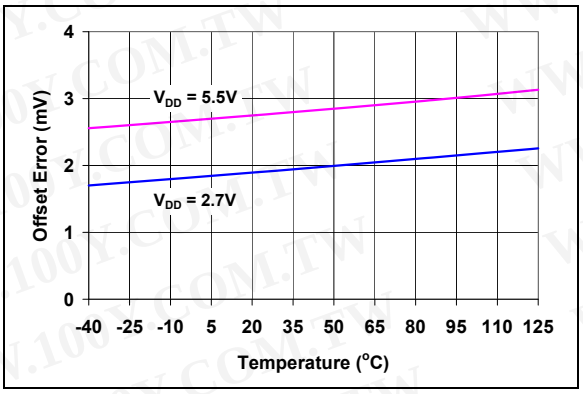


FIGURE 2-24: *Zero Scale Error vs. Temperature (Code = 000h, V_{REF} = V_{DD}).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

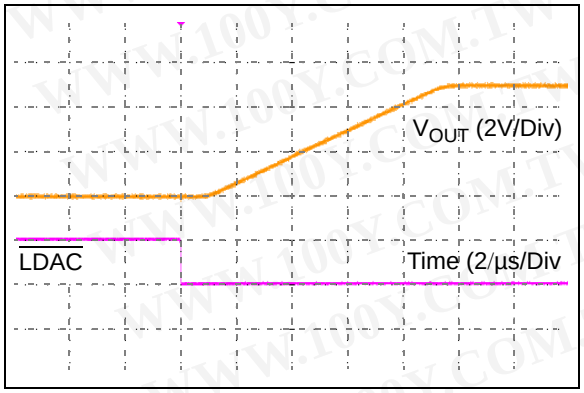


FIGURE 2-25: *Full Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 000h to FFFh).*

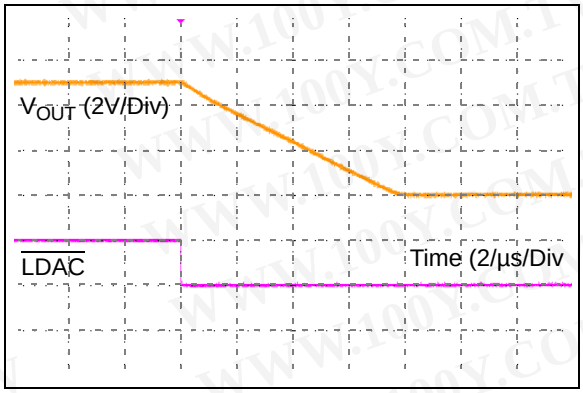


FIGURE 2-28: *Full Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: FFFh to 000h).*

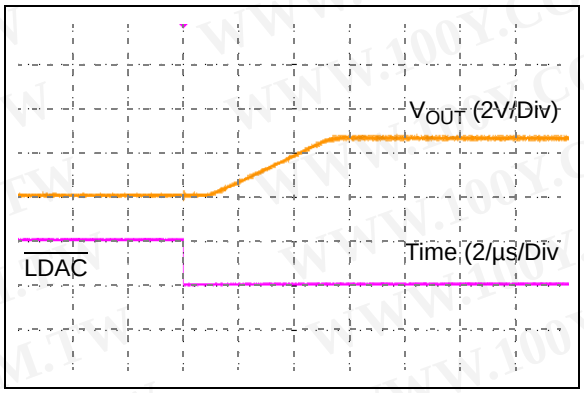


FIGURE 2-26: *Half Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 000h to 7FFh).*

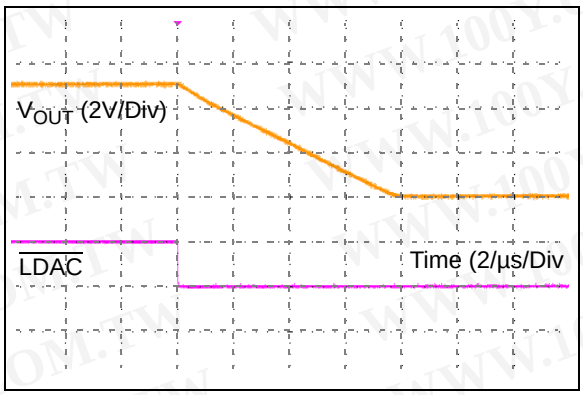


FIGURE 2-29: *Half Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: FFFh to 000h).*

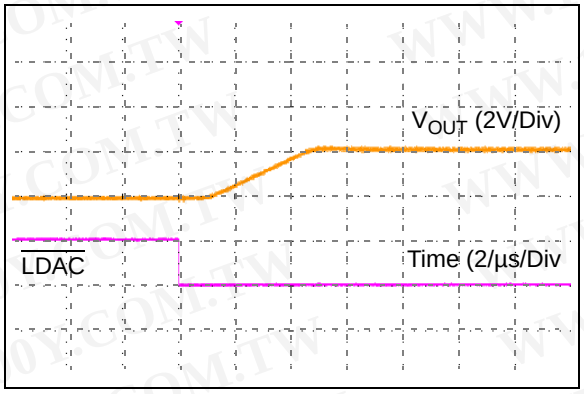


FIGURE 2-27: *Full Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 000h to FFFh).*

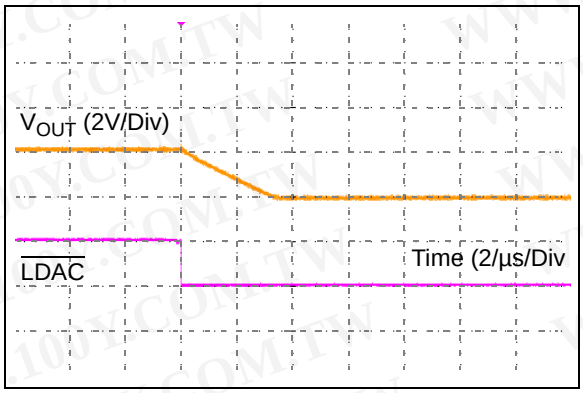


FIGURE 2-30: *Full Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: FFFh to 000h).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

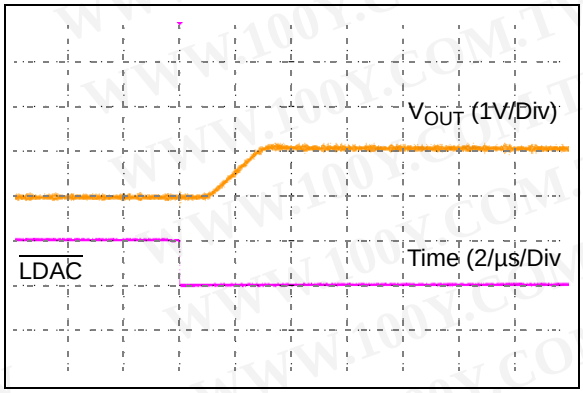


FIGURE 2-31: *Half Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 000h to 7FFh).*

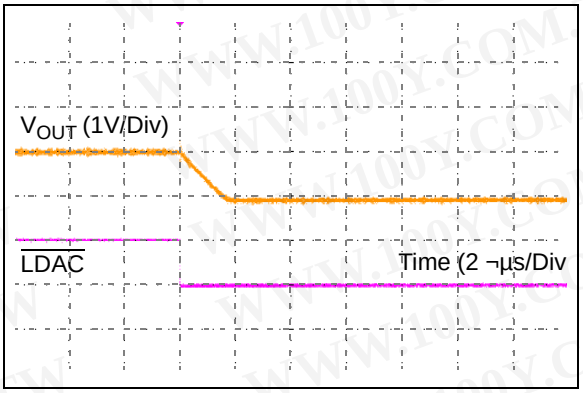


FIGURE 2-34: *Half Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1), Code Change: 7FFh to 000h.*

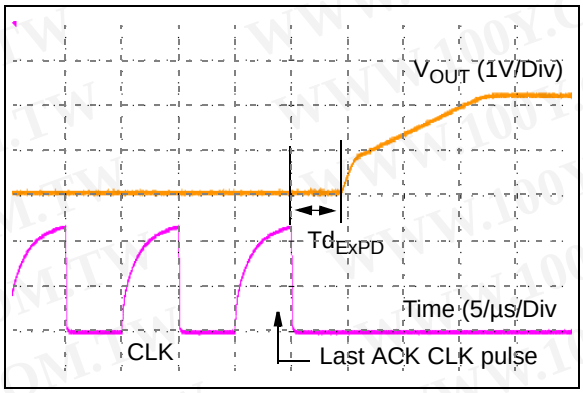


FIGURE 2-32: *Exiting Power Down Mode (Code : FFFh, V_{REF} = Internal, V_{DD} = 5V, for all Channels.).*

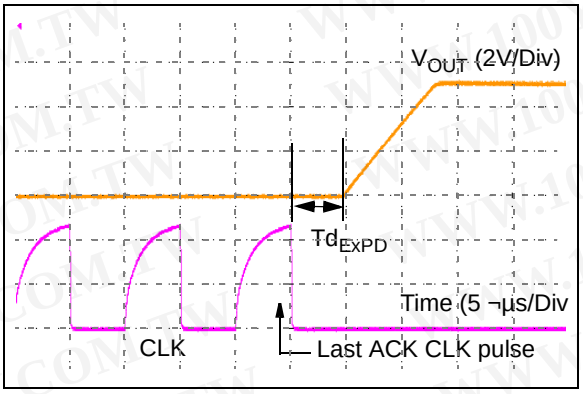


FIGURE 2-35: *Exiting Power Down Mode (Code : FFFh, V_{REF} = V_{DD}, V_{DD} = 5V, for all Channels).*

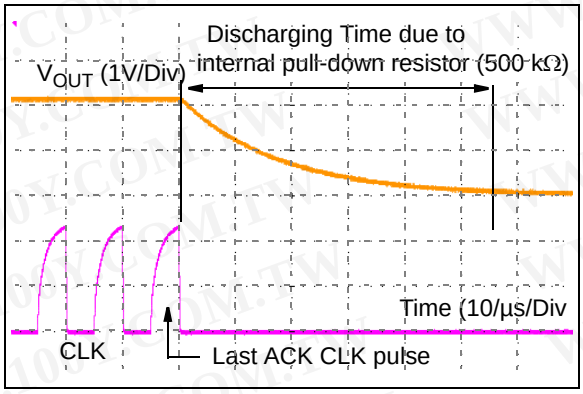


FIGURE 2-33: *Entering Power Down Mode (Code : FFFh, V_{REF} = Internal, V_{DD} = 5V, PD1= PD0 = 1, No External Load).*

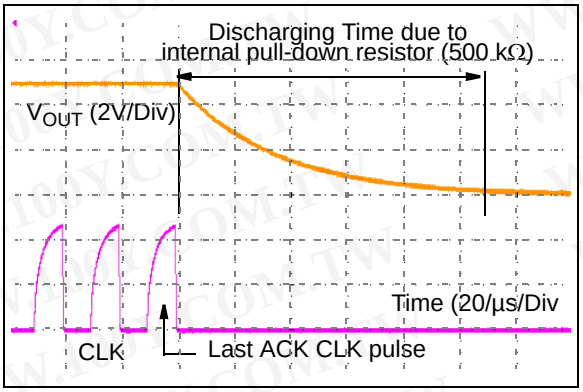


FIGURE 2-36: *Entering Power Down Mode (Code : FFFh, V_{REF} = V_{DD}, V_{DD} = 5V, PD1= PD0 = 1, No External Load).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

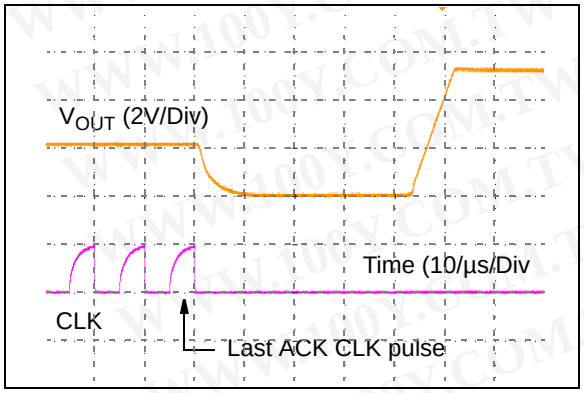


FIGURE 2-37: *V_{OUT} Time Delay when V_{REF} changes from Internal Reference to V_{DD}.*

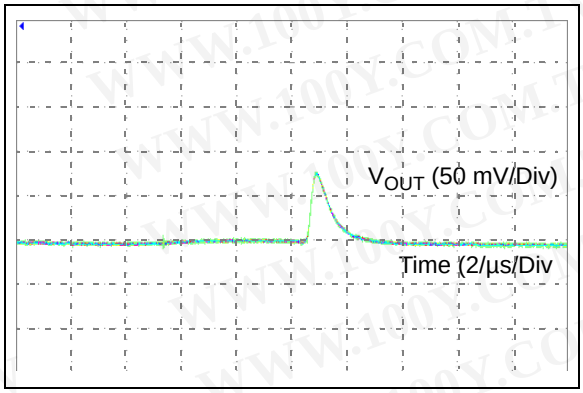


FIGURE 2-40: *Code Change Glitch (V_{REF} = External, V_{DD} = 5V, No External Load), Code Change: 800h to 7FFh.*

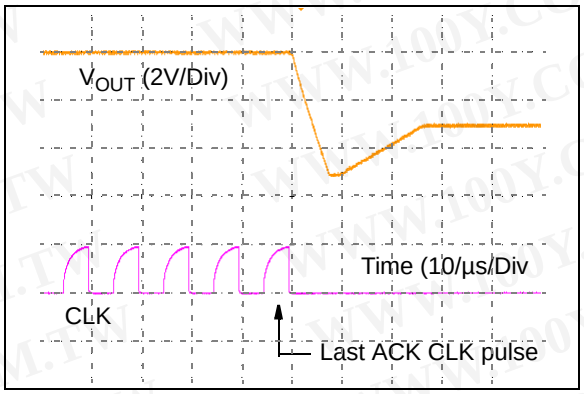


FIGURE 2-38: *V_{OUT} Time Delay when V_{REF} changes from V_{DD} to Internal Reference.*

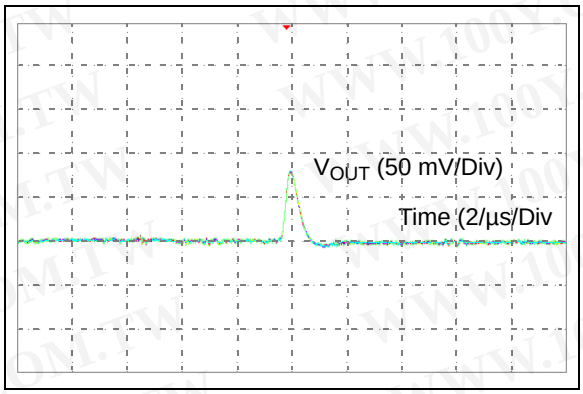


FIGURE 2-41: *Code Change Glitch (V_{REF} = Internal, V_{DD} = 5V, Gain = 1, No External Load), Code Change: 800h to 7FFh.*

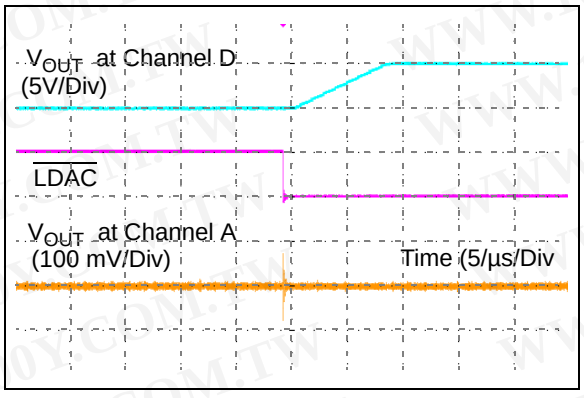


FIGURE 2-39: *Channel Cross Talk (V_{REF} = V_{DD}, V_{DD} = 5V).*

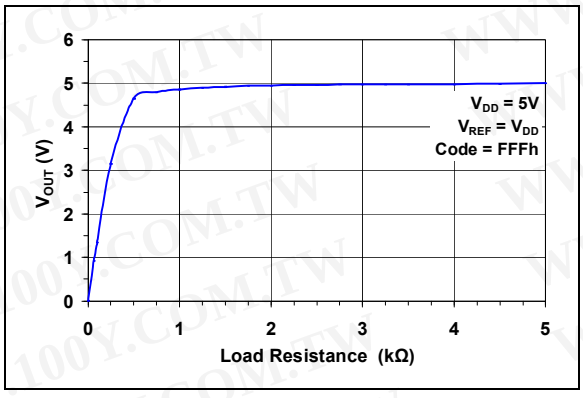


FIGURE 2-42: *V_{OUT} vs. Resistive Load.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

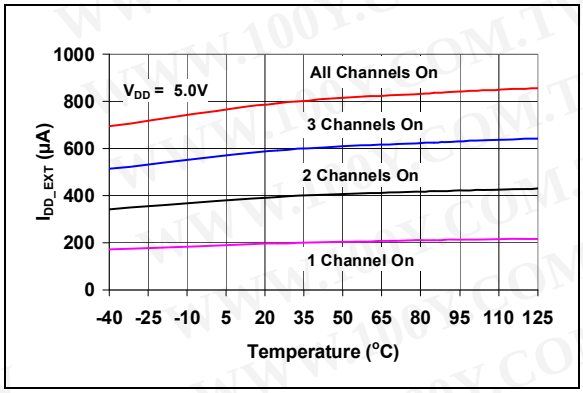


FIGURE 2-43: *I_{DD} vs. Temperature (V_{REF} = V_{DD}, V_{DD} = 5V, Code = FFFh).*

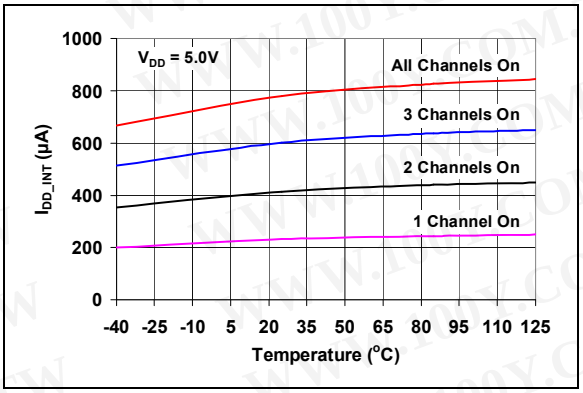


FIGURE 2-46: *I_{DD} vs. Temperature (V_{REF} = Internal, V_{REF} = 5V, Code = FFFh).*

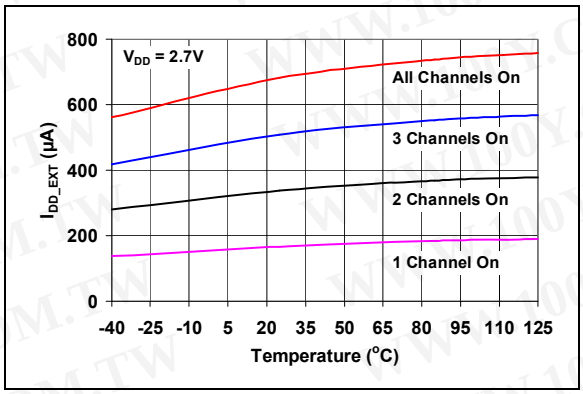


FIGURE 2-44: *I_{DD} vs. Temperature (V_{REF} = V_{DD}, V_{DD} = 2.7V, Code = FFFh).*

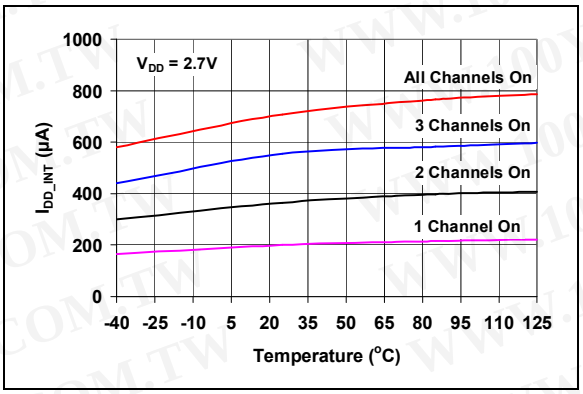


FIGURE 2-47: *I_{DD} vs. Temperature (V_{REF} = Internal, V_{DD} = 2.7V, Code = FFFh).*

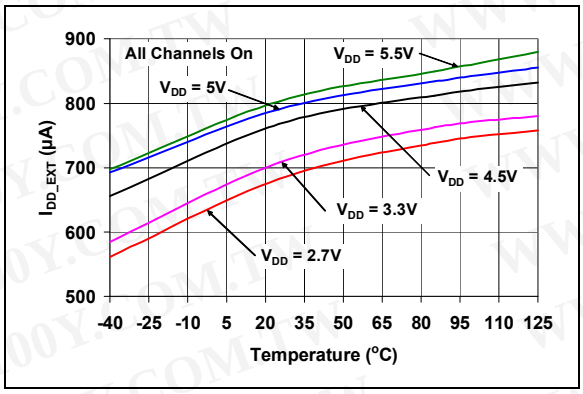


FIGURE 2-45: *I_{DD} vs. Temperature (V_{REF} = V_{DD}, All channels are in Normal Mode, Code = FFFh).*

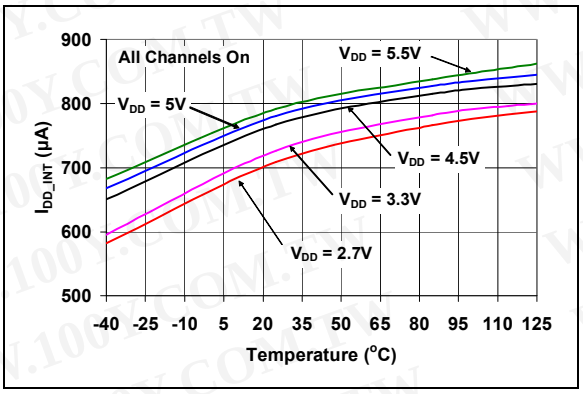


FIGURE 2-48: *I_{DD} vs. Temperature (V_{REF} = Internal , All Channels are in Normal Mode, Code = FFFh).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

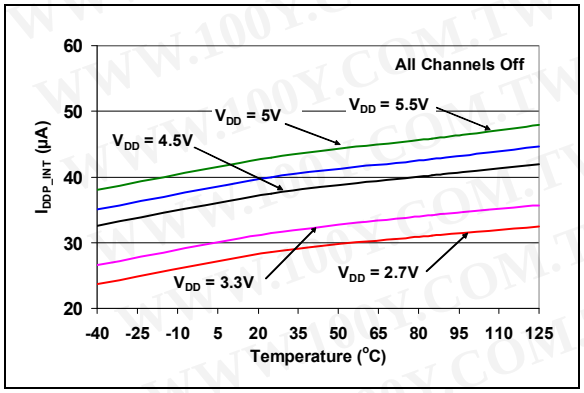


FIGURE 2-49: *I_{DD} vs. Temperature (V_{REF} = Internal , All Channels are in Powered Down).*

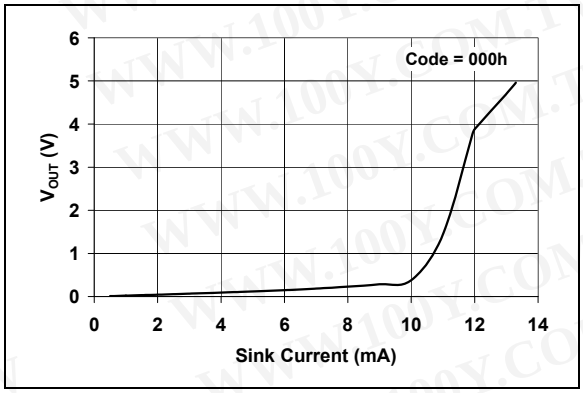


FIGURE 2-51: *Sink Current Capability (V_{REF} = V_{DD}, Code = 000h).*

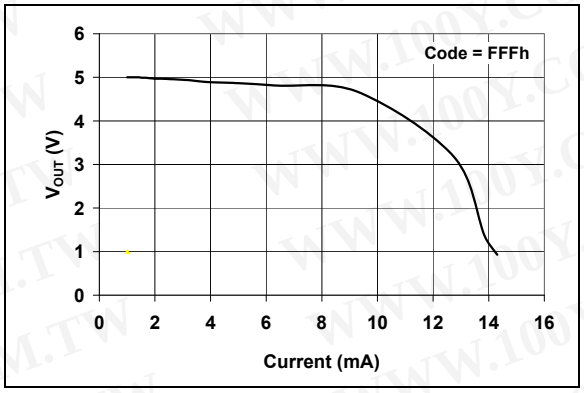


FIGURE 2-50: *Source Current Capability (V_{REF} = V_{DD}, Code = FFFh).*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Name	Pin Type	Function
1	V_{DD}	P	Supply Voltage
2	SCL	OI	I^2C Serial Clock Input. **(Note 1)**
3	SDA	OI/OO	I^2C Serial Data Input and Output. **(Note 1)**
4	$\overline{LDAC}$	ST	This pin is used for two purposes: (a) Synchronization Input. It is used to transfer the contents of the DAC input registers to the output registers (V_{OUT}). (b) Select the device for reading and writing I^2C address bits. **(Note 2)**
5	RDY/$\overline{BSY}$	OO	This pin is a status indicator of EEPROM programming activity. An external pull-up resistor (about 100 kΩ) is needed from RDY/$\overline{BSY}$ pin to V_{DD} line. **(Note 1)**
6	V_{OUT} A	AO	Buffered analog voltage output of channel A. The output amplifier has rail-to-rail operation.
7	V_{OUT} B	AO	Buffered analog voltage output of channel B. The output amplifier has rail-to-rail operation.
8	V_{OUT} C	AO	Buffered analog voltage output of channel C. The output amplifier has rail-to-rail operation.
9	V_{OUT} D	AO	Buffered analog voltage output of channel D. The output amplifier has rail-to-rail operation.
10	V_{SS}	P	Ground reference.

Legend: P = Power, OI = Open-Drain Input, OO = Open-Drain Output, ST = Schmitt Trigger Input Buffer, AO = Analog Output

Note 1: This pin needs an external pull-up resistor from V_{DD} line.

2: This pin can be driven by MCU.

3.1 Analog Output Voltage Pins ($V_{OUT}A$, $V_{OUT}B$, $V_{OUT}C$, $V_{OUT}D$)

The device has four analog voltage output (V_{OUT}) pins. Each output is driven by its own output buffer with a gain of 1 or 2 depending on the gain and V_{REF} selection bit settings. In normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to 1 kΩ, 100 kΩ, or 500 kΩ, depending on the Power-Down selection bit settings.

The V_{OUT} pin can drive up to 1000 pF of capacitive load. It is recommended to use a load with R_L greater than 5 kΩ.

3.2 Supply Voltage Pins (V_{DD}, V_{SS})

V_{DD} is the power supply pin for the device. The voltage at the V_{DD} pin is used as the power supply input as well as the DAC external reference. The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance.

It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in application boards. The supply voltage (V_{DD}) must be maintained in the 2.7V to 5.5V range for specified operation.

V_{SS} is the ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC register and EEPROM data. Except for start and stop conditions, the data on the SDA pin must be stable during the high duration of the clock pulse. The High or Low state of the SDA pin can only change when the clock signal on the SCL pin is Low.

The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin.

Refer to **Section 5.0 "I^2C Serial Interface Communications"** for more details of the I^2C Serial Interface communication.

3.4 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP4728 device acts only as a slave and the SCL pin accepts only external input serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP4728 occurs at the falling edges of the SCL clock.

The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin.

Refer to **Section 5.0 "I^2C Serial Interface Communications"** for more details of I^2C Serial Interface communication.

Typical range of the pull-up resistor value for SCL and SDA is from 5 kΩ to 10 kΩ for standard (100 kHz) and fast (400 kHz) modes, and less than 1 kΩ for high speed mode (3.4 MHz).

3.5 $\overline{\text{LDAC}}$ Pin

This pin can be driven by an external control device such as an MCU I/O pin. This pin is used (a) to transfer the contents of the input registers to their corresponding DAC output registers and (b) to select a device of interest when reading or writing I^2C address bits. See sections **Section 5.4.4 "General call Read Address Bits"** and **Section 5.6.8 "Write Command: Write I2C Address bits (C2=0, C1=1, C0=1)"** for more details of the reading and writing the device I^2C address bits, respectively.

When the logic status of the $\overline{\text{LDAC}}$ pin changes from "High" to "Low", the contents of all input registers (Channels A - D) are transferred to their corresponding output registers and all analog voltage outputs are updated simultaneously.

If this pin is permanently tied to "Low", the content of the input register is transferred to its output register (V_{OUT}) immediately at the last input data byte's acknowledge pulse.

The user can also use the $\overline{\text{UDAC}}$ bit instead. However, the $\overline{\text{UDAC}}$ bit updates a selected channel only. See **Section 4.8 "Output Voltage Update"** for more information on the $\overline{\text{LDAC}}$ pin and $\overline{\text{UDAC}}$ bit functions.

3.6 RDY/$\overline{\text{BSY}}$ Status Indicator Pin

This pin is a status indicator of EEPROM programming activity. This pin is "High" when the EEPROM has no programming activity and "Low" when the EEPROM is in programming mode. It goes "High" when the EEPROM program is completed.

The RDY/$\overline{\text{BSY}}$ pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor (about 100 kΩ) from the V_{DD} line to the RDY/$\overline{\text{BSY}}$ pin.

4.0 THEORY OF DEVICE OPERATION

The MCP4728 device is a 12-bit 4-channel buffered voltage output DAC with non-volatile memory (EEPROM). The user can program the EEPROM with I^2C address bits, configuration and DAC input data of each channel. The device has an internal charge pump circuit to provide the programming voltage of the EEPROM.

When the device is first powered-up, it automatically loads the stored data in its EEPROM to the DAC input and output registers, and provides analog outputs with the saved settings immediately. This event does not require LDAC or UDAC bit condition. After the device is powered-up, the user can update the input registers using I^2C write commands. The analog outputs can be updated with new register values if LDAC pin or UDAC bit is low. The DAC output of each channel is buffered with a low power and precision output amplifier. This amplifier provides a rail-to-rail output with low offset voltage and low noise.

The device uses a resistor string architecture. The resistor ladder DAC can be driven from V_{DD} or internal V_{REF} depending on the reference selection. The user can select internal (2.048V) or external reference (V_{DD}) for each DAC channel individually by software control. The V_{DD} is used as the external reference. Each channel is controlled and operated independently.

The device has a Power-Down mode feature. Most of the circuit in each powered down channel are turned off. Therefore, operating power can be saved significantly by putting any unused channel to the Power-Down mode.

4.1 Power-On-Reset (POR)

The device contains an internal Power-On-Reset (POR) circuit that monitors power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

If the power supply voltage is less than the POR threshold (V_{POR} = 2V, typical), all circuits are disabled and there will be no analog output. When the V_{DD} increases above the V_{POR}, the device takes a reset state. During the reset period, each channel uploads all configuration and DAC input codes from EEPROM, and analog output (V_{OUT}) will be available accordingly. This enables the device to return to the same state that it was at the last write to the EEPROM before it was powered off. The POR status is monitored by the POR status bit by using the I^2C read command. See Figure 5-15 for the details of the POR status bit.

The POR circuit is also powered off if all channels are powered down during the Power-Down mode.

4.2 Reset Conditions

The device can be reset by two independent events: (a) by Power-On-Reset or (b) by I^2C General Call Reset Command. Under the reset conditions, the device uploads the EEPROM data into both of the DAC input and output registers simultaneously. The analog output voltage of each channel is available immediately regardless of the LDAC and UDAC bit conditions.

The factory default settings for the EEPROM prior to the device shipment are shown in Table 4-2.

4.3 Output Amplifier

The DAC output is buffered with a low power precision amplifier. This amplifier provides low offset voltage and low noise, as well as rail-to-rail output.

The output amplifier can drive the resistive and high capacitive loads without oscillation. The amplifier can provide a maximum load current of 24 mA which is enough for most of programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

4.3.1 PROGRAMMABLE GAIN BLOCK

The rail-to-rail output amplifier of each channel has configurable gain option. When the internal voltage reference is selected, the output amplifier gain has two selection options: gain of 1 or gain of 2.

When the external reference is selected ($V_{REF} = V_{DD}$), the gain of 2 option is disabled, and only the gain of 1 is used by default.

4.3.1.1 Resistive and Capacitive Loads

The analog output (V_{OUT}) pin is capable of driving capacitive loads up to 1000 pF in parallel with 5 kΩ load resistance. Figure 2-42 shows the V_{OUT} vs. Resistive Load.

4.4 DAC Input Registers and Non-Volatile EEPROM Memory

Each channel has its own volatile DAC input register and EEPROM. The details of the input registers and EEPROM are shown in Table 4-1 and Table 4-2, respectively.

TABLE 4-1: INPUT REGISTER MAP (VOLATILE)

	Configuration Bits										DAC Input Data (12 bits)											
Bit Name	RDY /BSY	A2	A1	A0	VREF	DAC1	DAC0	PD1	PD0	Gx	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	**(Note 1)**	I^2C Address Bits **(Note 2)**			Ref. Select **(Note 2)**	DAC Channel **(Note 2)**		Power-Down Select **(Note 2)**		Gain Select **(Note 2)**	**(Note 2)**											
CH. A																						
CH. B																						
CH. C																						
CH. D																						

Note 1: EEPROM write status indication bit (flag).

2: Loaded from EEPROM during power-up, or can be updated by the user.

TABLE 4-2: EEPROM MEMORY MAP AND FACTORY DEFAULT SETTINGS

	Configuration Bits							DAC Input Data (12 bits)											
Bit Name	A2	A1	A0	VREF	PD1	PD0	Gx	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	I^2C Address Bits **(Note 1)**			Ref. Select **(Note 2)**	Power-Down Select		Gain Select **(Note 3)**												
CH. A	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH. B				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH. C				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH. D				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note 1: Device I^2C address bits. The user can also specify these bits during the device ordering process. The factory default setting is “000”. These bits can be reprogrammed by the user using the I^2C Address Write command.

2: Voltage Reference Select: **0 =** External V_{REF} (V_{DD}), **1 =** Internal V_{REF} (2.048V).

3: Gain Select: **0 =** Gain of 1, **1 =** Gain of 2.

TABLE 4-3: CONFIGURATION BITS

Bit Name	Functions
RDY/$\overline{BSY}$	This is a status indicator (flag) of EEPROM programming activity: **1 =** EEPROM is not in programming mode **0 =** EEPROM is in programming mode **Note:** RDY/$\overline{BSY}$ status can also be monitored at the RDY/$\overline{BSY}$ pin.
(A2, A1, A0)	Device I^2C address bits. See **Section 5.3 "MCP4728 Device Addressing"** for more details.
V_{REF}	Voltage Reference Selection bit: **0 =** V_{DD} **1 =** Internal voltage reference (2.048V) **Note:** Internal voltage reference circuit is turned off if all channels select external reference ($V_{REF} = V_{DD}$).
DAC1, DAC0	DAC Channel Selection bits: **00 =** Channel A **01 =** Channel B **10 =** Channel C **11 =** Channel D
PD1, PD0	Power-Down selection bits: **00 =** Normal Mode **01 =** V_{OUT} is loaded with 1 kΩ resistor to ground. Most of the channel circuits are powered off. **10 =** V_{OUT} is loaded with 100 kΩ resistor to ground. Most of the channel circuits are powered off. **11 =** V_{OUT} is loaded with 500 kΩ resistor to ground. Most of the channel circuits are powered off. **Note:** See Table 4-7 and Figure 4-1 for more details.
G_X	Gain selection bit: **0 =** x1 (gain of 1) **1 =** x2 (gain of 2) **Note:** Applicable only when internal V_{REF} is selected. If $V_{REF} = V_{DD}$, the device uses a gain of 1 regardless of the gain selection bit setting.
$\overline{UDAC}$	DAC latch bit. Upload the selected DAC input register to its output register (V_{OUT}): **0 =** Upload. Output (V_{OUT}) is updated. **1 =** Do not upload. **Note:** $\overline{UDAC}$ bit affects the selected channel only.

4.5 Voltage Reference

The device has a precision internal voltage reference which provides a nominal voltage of 2.048V. The user can select the internal voltage reference or V_{DD} as the voltage reference source of each channel using the V_{REF} configuration bit. The internal voltage reference circuit is turned off when all channels select V_{DD} as their references. However, it stays turned on if any one of the channels selects the internal reference.

4.6 LSB Size

The LSB is defined as the ideal voltage difference between two successive codes. LSB sizes of the MCP4728 device are shown in Table 4-4.

TABLE 4-4: LSB SIZES (EXAMPLE)

V_{REF}	Gain (G_X) Selection	LSB Size	Condition
Internal V_{REF} (2.048V)	x1	0.5 mV	2.048V/4096
	x2	1 mV	4.096V/4096
V_{DD}	x1	V_{DD}/4096	**(Note 1**

Note 1: LSB size varies with the V_{DD} range. When V_{REF} = V_{DD}, the device uses G_X = 1 by default. G_X = 2 option is ignored.

4.7 DAC Output Voltage

Each channel has an independent output associated with its own configuration bit settings and DAC input code. When the internal voltage reference is selected (V_{REF} = internal), it supplies the internal V_{REF} voltage to the resistor string DAC of the channel. When the external reference (V_{REF}=V_{DD}) is selected, V_{DD} is used for the channel's resistor string DAC.

The V_{DD} needs to be as clean as possible for accurate DAC performance. When the V_{DD} is selected as the voltage reference, any variation or noises on the V_{DD} line can directly affect on the DAC output.

The analog output of each channel has a programmable gain block. The rail-to-rail output amplifier has a configurable gain of 1 or 2. But the gain of 2 is not applicable if V_{DD} is selected for the voltage reference. The formula for the analog output voltage is given in Equation 4-1 and Equation 4-2.

4.7.1 OUTPUT VOLTAGE RANGE

The DAC output voltage range varies depending on the voltage reference selection.

- When the internal reference (V_{REF}=2.048V) is selected:

V_{OUT} = 0.000V to 2.048V * 4095/4096 for Gain of 1
= 0.000V to 4.096V * 4095/4096 for Gain of 2

- When the external reference (V_{REF}=V_{DD}) is selected:

V_{OUT} = 0.000V to V_{DD}

Note that the gain selection bit is not applicable for V_{REF} = V_{DD}. Gain of 1 is used regardless of the gain selection bit setting.

EQUATION 4-1: V_{OUT} FOR V_{REF} = INTERNAL REFERENCE

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{4096} G_x \leq V_{DD}$$

Where:

V_{REF} = 2.048V for internal reference selection
D_n = DAC input code
G_x = Gain Setting

EQUATION 4-2: VOUT FOR VREF = V_{DD}

$$V_{OUT} = \frac{(V_{DD} \times D_n)}{4096}$$

Where:

D_n = DAC input code

4.8 Output Voltage Update

The following events update the output registers (V_{OUT}):

a. $\overline{LDAC}$ pin to "Low": Updates all DAC channels.
b. $\overline{UDAC}$ bit to "Low": Updates a selected channel only.
c. General Call Software Update Command: Updates all DAC channels.
d. Power-On-Reset or General Call Reset command: Both input and output registers are updated with EEPROM data. All channels are affected.

4.8.1 $\overline{LDAC}$ PIN AND $\overline{UDAC}$ BIT

The user can use the $\overline{LDAC}$ pin or $\overline{UDAC}$ bit to upload the input DAC register to output DAC register (V_{OUT}). However, the $\overline{UDAC}$ affects only the selected channel while the $\overline{LDAC}$ affects all channels. The $\overline{UDAC}$ bit is not used in the Fast Mode Writing.

Table 4-5 shows the output update vs. $\overline{LDAC}$ pin and $\overline{UDAC}$ bit conditions.

TABLE 4-5: $\overline{\text{LDAC}}$ AND $\overline{\text{UDAC}}$ CONDITIONS VS. OUTPUT UPDATE

$\overline{\text{LDAC}}$ Pin	$\overline{\text{UDAC}}$ Bit	DAC Output (V_{OUT})
0	0	Update all DAC channel outputs.
0	1	Update all DAC channel outputs.
1	0	Update a selected DAC channel output.
1	1	No update

4.9 Analog Output Vs. DAC Input Code

Table 4-6 shows an example of the DAC input data code vs. analog output. The MSB of the input data is always transmitted first and the format is unipolar binary.

TABLE 4-6: DAC INPUT CODE VS. ANALOG OUTPUT (V_{OUT})

DAC Input Code	V_{REF} = Internal (2.048 V)		V_{REF} = V_{DD}	
	Gain Selection	Nominal Output Voltage (V) (See Note 1)	Gain Selection	Nominal Output Voltage (V)
111111111111	x1	V_{REF} - 1 LSB	Ignored	V_{DD} - 1 LSB
	x2	2*V_{REF} - 1 LSB		
111111111110	x1	V_{REF} - 2 LSB		V_{DD} - 2 LSB
	x2	2*V_{REF} - 2 LSB		
000000000010	x1	2 LSB		2 LSB
	x2	2 LSB		
000000000001	x1	1 LSB		1 LSB
	x2	1 LSB		
000000000000	x1	0		0
	x2	0		

Note 1: (a) LSB with gain of 1 = 0.5 mV, and (b) LSB with gain of 2 = 1 mV.

4.10 Normal and Power-Down Modes

Each channel has two modes of operation: (a) Normal mode where analog voltage is available and (b) Power-Down mode which turns off most of the internal circuits for power savings.

The user can select the operating mode of each channel individually by setting the Power-Down selection bits (PD1 and PD0). For example, the user can select channel A for normal mode while selecting all other channels for power-down mode.

See **Section 5.6 "Write Commands for DAC Registers and EEPROM"** for more details on the writing the power-down bits.

Most of the internal circuit in the powered down channel are turned off. However, the internal voltage reference circuit is not affected by the Power-Down mode. The internal voltage reference circuit is turned off only if all channels select external reference ($V_{REF} = V_{DD}$).

Device actions during Power-Down mode:

- The powered down channel stays in a power saving condition by turning off most of its circuits.
- No analog voltage output at the powered down channel.
- The output (V_{OUT}) pin of the powered down channel is switched to a known resistive load. The value of the resistive load is determined by the state of the Power-Down bits (PD1 and PD0). Table 4-7 shows the outcome of the Power-Down bit settings.
- The contents of both the DAC registers and EEPROM are not changed.
- Draws less than 40 nA (typical) when all four channels are powered down and V_{DD} is selected as the voltage reference.

Circuits that are not affected during Power-Down Mode:

- The I^2C serial interface circuits remain active in order to receive any command from the Master.
- The internal voltage reference circuit stays turned-on if it is selected as reference by at least one channel.

Exiting Power-Down Mode:

The device exits Power-Down mode immediately by the following commands:

- Any write command for normal mode. Only selected channel is affected.
- I^2C General Call Wake-Up Command. All channels are affected.
- I^2C General Call Reset Command. This is a conditional case. The device exits Power-Down mode depending on the Power-Down bit settings in EEPROM as the configuration bits and DAC input codes are uploaded from EEPROM. All channels are affected.

When the DAC operation mode is changed from the Power-Down to normal mode, there will be a time delay until the analog output is available. Typical time delay for the output voltage is approximately 4.5 µs. This time delay is measured from the acknowledge pulse of the I^2C serial communication command to the beginning of the analog output (V_{OUT}). This time delay is not included in the output settling time specification. See **Section 2.0 "Typical Performance Curves"** for more details.

TABLE 4-7: POWER-DOWN BITS

PD1	PD0	Function
0	0	Normal Mode
0	1	1 kΩ resistor to ground **(Note 1)**
1	0	100 kΩ resistor to ground **(Note 1)**
1	1	500 kΩ resistor to ground (Note 1)

Note 1: In Power-Down mode: V_{OUT} is off and most of internal circuits in the selected channel are disabled.

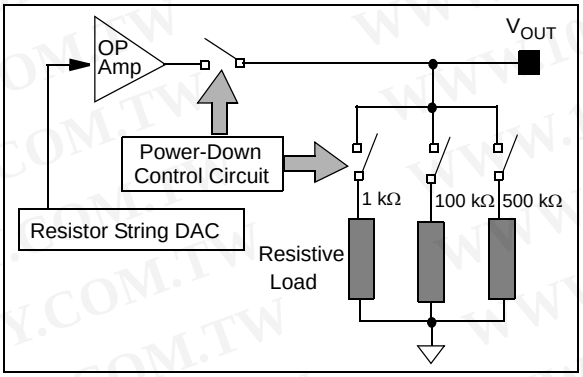


FIGURE 4-1: *Output Stage for Power-Down Mode.*

5.0 I²C SERIAL INTERFACE COMMUNICATIONS

The MCP4728 device uses a two-wire I²C serial interface. When the device is connected to the I²C bus line, the device works as a slave device. The device supports standard, fast and high speed modes.

The following sections describes how to communicate the MCP4728 device using the I²C serial interface commands.

5.1 Overview of I²C Serial Interface Communications

An example of hardware connection diagram is shown in Figure 7-1. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master (MCU) device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions. Both master (MCU) and slave (MCP4728) can operate as transmitter or receiver, but the master device determines which mode is activated.

Communication is initiated by the master (MCU) which sends the START bit, followed by the slave (MCP4728) address byte. The first byte transmitted is always the slave (MCP4728) address byte, which contains the device code (1100), the address bits (A2, A1, A0), and the R/$\overline{W}$ bit. The device code for the MCP4728 device is 1100, and the address bits are user-writable.

When the MCP4728 device receives a read command (R/$\overline{W}$ = 1), it transmits the contents of the DAC input registers and EEPROM sequentially. When writing to the device (R/$\overline{W}$ = 0), the device will expect write command type bits in the following byte. The reading and various writing commands are explained in the following sections.

The MCP4728 device supports all three I²C serial communication operating modes:

- Standard Mode: bit rates up to 100 kbit/s
- Fast Mode: bit rates up to 400 kbit/s
- High Speed Mode (HS mode): bit rates up to 3.4 Mbit/s

Refer to the Philips I²C document for more details of the I²C specifications.

5.1.1 HIGH-SPEED (HS) MODE

The I²C specification requires that a high-speed mode device must be 'activated' to operate in high-speed (3.4 Mbit/s) mode. This is done by sending a special address byte of 00001XXX following the START bit. The XXX bits are unique to the high-speed (HS) mode Master. This byte is referred to as the high-speed (HS) Master Mode Code (HSMMC). The MCP4728 device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode and can communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I²C modes, please refer to the Philips I²C specification.

5.2 I²C BUS CHARACTERISTICS

The specification of the I²C serial communication defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined using Figure 5-1.

5.2.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

5.2.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition.

All commands must be preceded by a START condition.

5.2.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

5.2.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

5.2.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must send an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave.

In this case, the slave (MCP4728) will leave the data line HIGH to enable the master to generate the STOP condition.

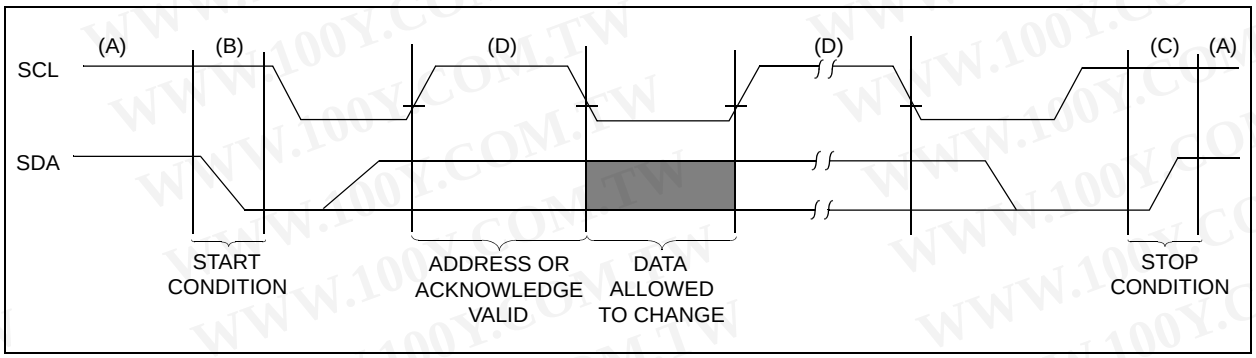


FIGURE 5-1: *Data Transfer Sequence On The Serial Bus.*

5.3 MCP4728 Device Addressing

The address byte is the first byte received following the START condition from the master device. The first part of the address byte consists of a 4-bit device code which is set to `1100` for the MCP4728 device. The device code is followed by three I²C address bits (A2, A1, A0) which are programmable by the users. Although the three address bits are programmable at the user's application PCB, the user can also specify the address bits during the product ordering process. If there is no user's request, the factory default setting of the three address bits is "000" which is programmed into the EEPROM. The three address bits allows eight unique addresses.

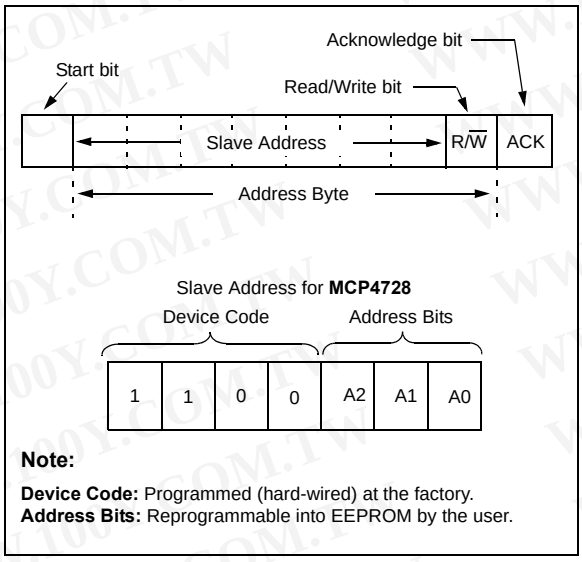


FIGURE 5-2: *Device Addressing.*

5.3.1 PROGRAMMING OF I²C ADDRESS BITS

When the customer first receives any new MCP4728 device, its default address bit setting is "`000`". The customer can reprogram the I²C address bits into the EEPROM by using "Write Address Bit" command. This write command needs current address bits. If the address bits are unknown, the user can find them by sending "General Call Read Address" Command. The $\overline{\text{LDAC}}$ pin is also used to select the device of interest to be programmed or to read the current address.

The following steps are needed for the I²C address programming.

(a) Read the address bits using "General Call Read Address" Command. (This is the case when the address is unknown.)

(b) Write I²C address bits using "Write I²C Address Bits" Command.

The write address command will replace the current address with a new address in both input registers and EEPROM.

See **Section 5.4.4 "General call Read Address Bits"** for the details of reading the address bits, and **Section 5.6.8 "Write Command: Write I2C Address bits (C2=0, C1=1, C0=1)"** for writing the address bits.

5.4 I²C General Call Commands

The device acknowledges the general call address command (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. The I²C specification does not allow to use "00000000" (00h) in the second byte. Please refer to the Philips I²C document for more details of the General Call specifications.

The MCP4728 device supports the following I²C General Calls:

- General Call Reset
- General Call Wake-Up
- General Call Software Update
- General Call Read Address Bits

5.4.1 GENERAL CALL RESET

The **General Call Reset** occurs if the second byte is "00000110" (06h). At the acknowledgement of this byte, the device will abort the current conversion and perform the following tasks:

- Internal reset similar to a Power-On-Reset (POR). The contents of the EEPROM are loaded into each DAC input and output registers immediately.
- V_{OUT} will be available immediately regardless of the $\overline{LDAC}$ pin condition.

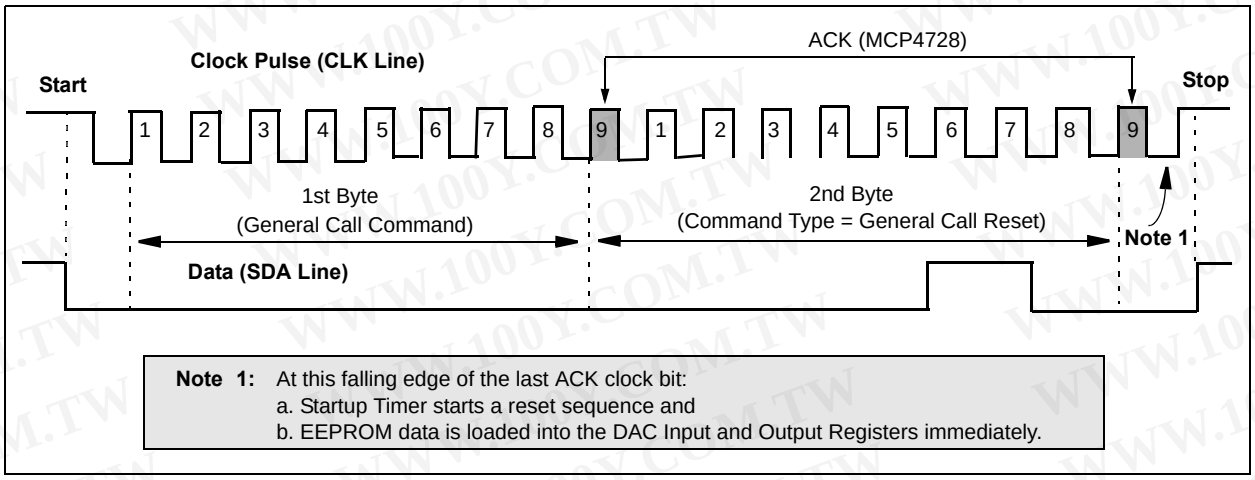


FIGURE 5-3: *General Call Reset.*

5.4.2 GENERAL CALL WAKE-UP

If the second byte is "00001001" (09h), the device will reset the Power-Down bits (PD1,PD0 = 0,0).

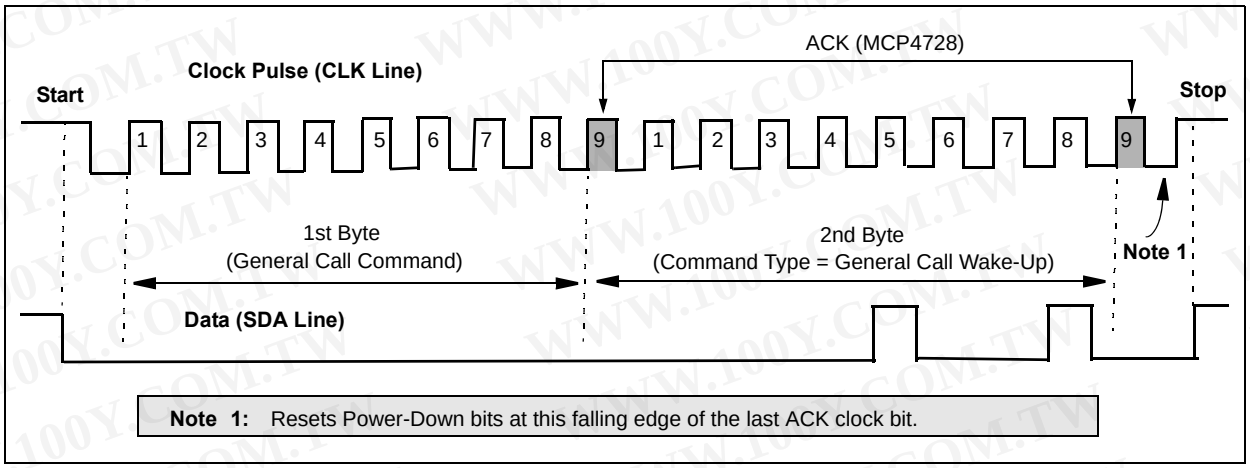


FIGURE 5-4: *General Call Wake-Up.*

5.4.3 GENERAL CALL SOFTWARE UPDATE

If the second byte is “00001000” (08h), the device updates all DAC analog outputs (V_{OUT}) at the same time.

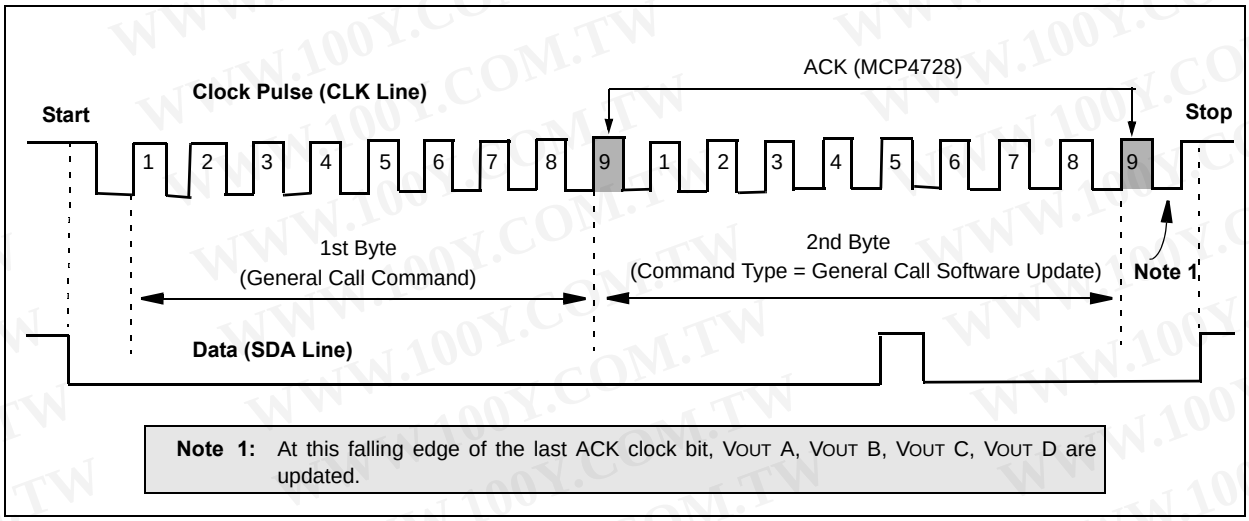
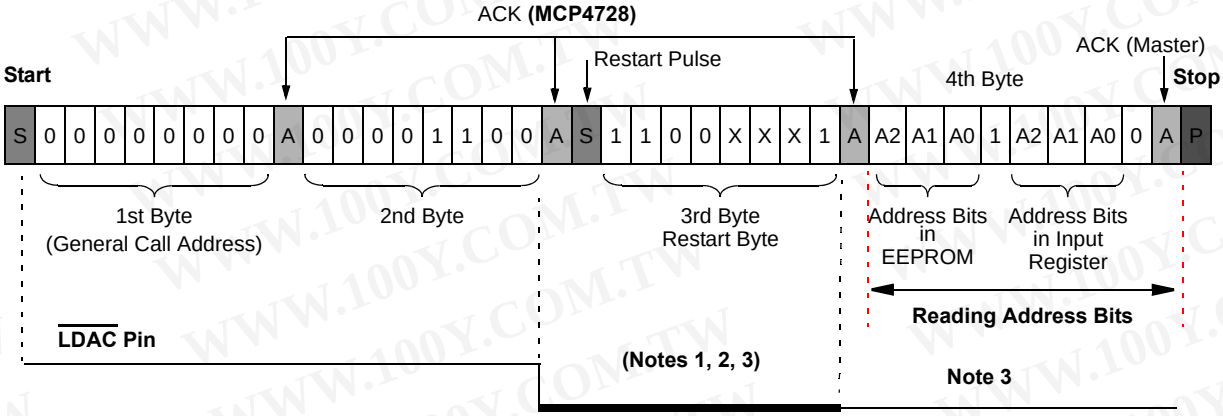
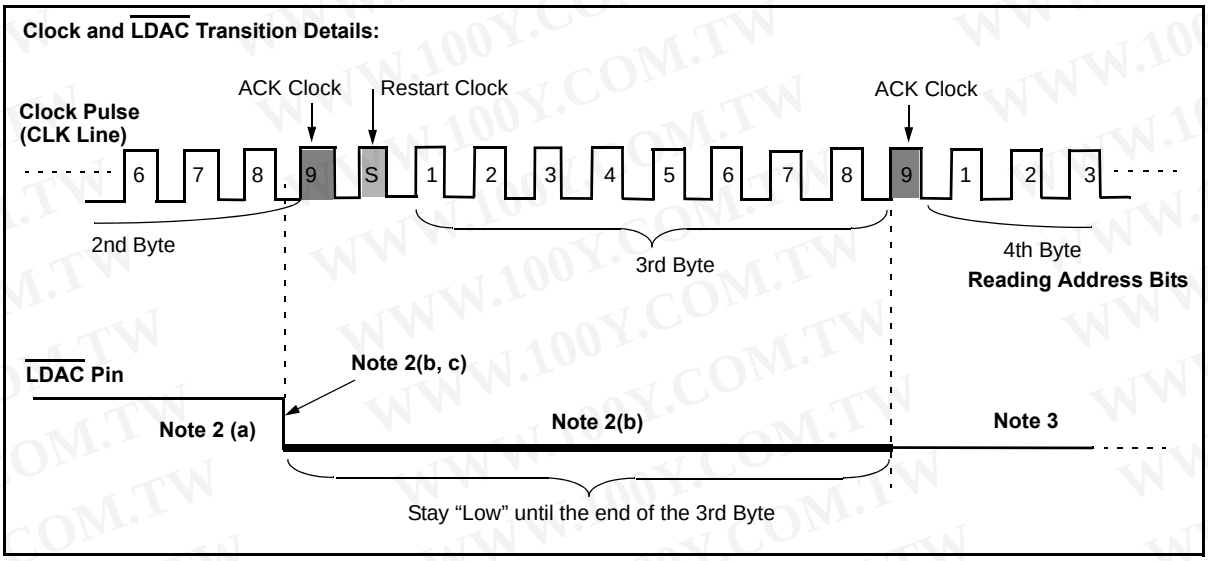


FIGURE 5-5: *General Call Software Update.*

5.4.4 GENERAL CALL READ ADDRESS BITS

This command is used to read the I^2C address bits of the device. If the second byte is "00001100" (0Ch), the device will output its address bits stored in EEPROM and register. This command uses the $\overline{LDAC}$ pin to select the device of interest to read on the I^2C bus. The $\overline{LDAC}$ pin needs a logic transition from "High" to "Low" during the negative pulse of the 8th clock of the second byte, and stays "Low" until the end of the 3rd byte. The maximum clock rate for this command is 400 kHz.





Note 1: Clock Pulse and $\overline{LDAC}$ Transition Details.

2: $\overline{LDAC}$ pin events at the 2nd and 3rd bytes.

a. Keep $\overline{LDAC}$ pin "High" until the end of the positive pulse of the 8th clock of the 2nd byte.

b. $\overline{LDAC}$ pin makes a transition from "High" to "Low" during the negative pulse of the 8th clock of the 2nd byte (just before the rising edge of the 9th clock) and stays "Low" until the rising edge of clock 9 of the 3rd byte.

c. The MCP4728 device does not acknowledge the 3rd byte if the conditions (a) and (b) are not met.

3: $\overline{LDAC}$ pin resumes its normal function after "Stop" bit.

FIGURE 5-6: *General Call Read I^2C Address.*

5.5 Writing and Reading Registers and EEPROM

The Master (MCU) can write or read the DAC input registers or EEPROM using the I^2C interface command.

The following sections describe the communication examples to write and read the DAC registers and EEPROM using the I^2C interface.

5.6 Write Commands for DAC Registers and EEPROM

Table 5-1 summarizes the write command types and their functions.The write command is defined by using three write command type bits (C2, C1, C0) and two write function bits (W1, W0). The register selection bits (DAC1, DAC0) are used to select the DAC channel.

TABLE 5-1: WRITE COMMAND TYPES

Command Field			Write Function		Command Name	Function
C2	C1	C0	W1	W0		
Fast Mode Write						
0	0	X	Not Used		Fast Write for DAC Input Registers	This command writes to the DAC input registers sequentially with limited configuration bits. The data is sent sequentially from channels A to D. The input register is written at the acknowledge clock pulse of the channel's last input data byte. EEPROM is not affected. **(Note 1)**
Write DAC Input Register and EEPROM						
0	1	0	0	0	Multi-Write for DAC Input Registers	This command writes to multiple DAC input registers, one DAC input register at a time. The writing channel register is defined by the DAC selection bits (DAC1, DAC0). EEPROM is not affected. **(Note 2)**
			1	0	Sequential Write for DAC Input Registers and EEPROM	This command writes to both the DAC input registers and EEPROM sequentially. The sequential writing is carried out from a starting channel to channel D. The starting channel is defined by the DAC selection bits (DAC1 and DAC0). The input register is written at the acknowledge clock pulse of the last input data byte of each register. However, the EEPROM data is written altogether at the same time sequentially at the end of the last byte. **(Note 2),(Note 3)**
			1	1	Single Write for DAC Input Register and EEPROM	This command writes to a single selected DAC input register and its EEPROM. Both the input register and EEPROM are written at the acknowledge clock pulse of the last input data byte. The writing channel is defined by the DAC selection bits (DAC1 and DAC0). **(Note 2),(Note 3)**
Write I^2C Address Bits (A2, A1, A0)						
0	1	1	Not Used		Write I^2C Address Bits	This command writes new I^2C address bits (A2, A1, A0) to the DAC input register and EEPROM.
Write V_{REF}, Gain, and Power-Down Select Bits (Note 4)						
1	0	0	Not Used		Write Reference (V_{REF}) selection bits to Input Registers	This command writes Reference (V_{REF}) selection bits of each channel.
1	1	0	Not Used		Write Gain selection bits to Input Registers	This command writes Gain selection bits of each channel.
1	0	1	Not Used		Write Power-Down bits to Input Registers	This command writes Power-Down bits of each channel.

Note 1: The analog output is updated when $\overline{\text{LDAC}}$ pin is (or changes to) "Low". $\overline{\text{UDAC}}$ bit is not used for this command.

2: The DAC output is updated when $\overline{\text{LDAC}}$ pin or $\overline{\text{UDAC}}$ bit is "Low".

3: The device starts writing to the EEPROM on the acknowledge clock pulse of the last channel. The device does not execute any command until RDY/$\overline{\text{BSY}}$ bit comes back to "High".

4: The input and output registers are updated at the acknowledge clock pulse of the last byte. The update does not require $\overline{\text{LDAC}}$ pin or $\overline{\text{UDAC}}$ bit conditions. EEPROM is not affected.

5.6.1 FAST WRITE COMMAND (C2=0, C1=0, C0=X, X = DON'T CARE)

The Fast Write command is used to update the input DAC registers from channels A to D sequentially. The EEPROM data is not affected by this command. This command is called "Fast Write" because it updates the input registers with only limited data bits. Only the Power-Down mode selection bits (PD1 and PD0) and 12 bits of DAC input data are writable.

The input register is updated at the acknowledge pulse of each channel's last data byte. Figure 5-7 shows an example of the Fast Write command.

Updating Analog Outputs:

a. When the $\overline{\text{LDAC}}$ pin is "High" before the last byte of the channel D, all analog outputs are updated simultaneously by bringing down the $\overline{\text{LDAC}}$ pin to "Low" any time.
b. If the command starts with the $\overline{\text{LDAC}}$ pin "Low", the channel's analog output is updated at the falling edge of the acknowledge clock pulse of the channel's last byte.
c. Send the General Call Software Update command: This command updates all channels simultaneously.

Note 1: $\overline{\text{UDAC}}$ bit is not used in this command.

5.6.2 MULTI-WRITE COMMAND: WRITE DAC INPUT REGISTERS (C2=0, C1=1, C0=0; W1=0, W0=0)

This command is used to write DAC input register, one at a time. The EEPROM data is not affected by this command.

The DAC selection bits (DAC1, DAC0) select the DAC channel to write. Only a selected channel is affected. Repeated bytes are used to write more multiple DAC registers.

The D11 - D0 bits in the third and fourth bytes are the DAC input data of the selected DAC channel. Bytes 2 - 4 can be repeated for the other channels. Figure 5-8 shows an example of the Multi-Write command.

Updating Analog Outputs:

The analog outputs can be updated by one of the following events after the falling edge of the acknowledge clock pulse of the 4th byte.

a. When the $\overline{\text{LDAC}}$ pin or $\overline{\text{UDAC}}$ bit is "Low".
b. If $\overline{\text{UDAC}}$ bit is "High", bringing down the $\overline{\text{LDAC}}$ pin to "Low" any time.
c. By sending the General Call Software Update command.

Note 1: The $\overline{\text{UDAC}}$ bit can be used effectively to upload the input register to the output register, but it affects only a selected channel only, while the $\overline{\text{LDAC}}$ pin and General Call Software Update command affect all channels.

5.6.3 SEQUENTIAL WRITE COMMAND: WRITE DAC INPUT REGISTERS AND EEPROM SEQUENTIALLY FROM STARTING CHANNEL TO CHANNEL D (C2=0, C1=1, C0=0; W1=1, W0=0)

When the device receives this command, it writes the input data to the DAC input registers sequentially from the starting channel to channel D, and also writes to EEPROM sequentially. The starting channel is determined by the DAC1 and DAC0 bits. Table 5-2 shows the functions of the channel selection bits for the sequential write command.

When the device is writing EEPROM, the RDY/$\overline{\text{BSY}}$ bit stays “Low” until the EEPROM write operation is completed. The state of the RDY/$\overline{\text{BSY}}$ bit flag can be monitored by a read command or at the RDY/$\overline{\text{BSY}}$ pin. Any new command received during the EEPROM write operation (RDY/$\overline{\text{BSY}}$ bit is “Low”) is ignored. Figure 5-9 shows an example of the sequential write command.

Updating Analog Outputs:

The analog outputs can be updated by one of the following events after the falling edge of the acknowledge clock pulse of the 4th byte.

a. When the $\overline{\text{LDAC}}$ pin or $\overline{\text{UDAC}}$ bit is “Low”.
b. If $\overline{\text{UDAC}}$ bit is “High”, bringing down the $\overline{\text{LDAC}}$ pin to “Low” any time.
c. By sending the General Call Software Update command.

Note 1: The $\overline{\text{UDAC}}$ bit can be used effectively to upload the input register to the output register, but it affects only a selected channel only, while the $\overline{\text{LDAC}}$ pin and General Call Software Update command affect all channels.

TABLE 5-2: DAC CHANNEL SELECTION BITS FOR SEQUENTIAL WRITE COMMAND

DAC1	DAC0	Channels
0	0	Ch. A - Ch. D
0	1	Ch. B - Ch. D
1	0	Ch. C - Ch. D
1	1	Ch. D

5.6.4 SINGLE WRITE COMMAND: WRITE A SINGLE DAC INPUT REGISTER AND EEPROM (C2=0, C1=1, C0=0; W1=1, W0=1)

When the device receives this command, it writes the input data to a selected single DAC input register and also to its EEPROM. The channel is selected by the channel selection bits (DAC1 and DAC0). See Table 4-3 for the channel selection bit function. Figure 5-10 shows an example of the single write command.

Updating Analog Outputs:

The analog outputs can be updated by one of the following events after the falling edge of the acknowledge clock pulse of the 4th byte.

a. When the $\overline{\text{LDAC}}$ pin or $\overline{\text{UDAC}}$ bit is “Low”.
b. If $\overline{\text{UDAC}}$ bit is “High”, bringing down the $\overline{\text{LDAC}}$ pin to “Low” any time.
c. By sending the General Call Software Update command.

Note 1: The $\overline{\text{UDAC}}$ bit can be used effectively to upload the input register to the output register, but it affects only a selected channel only, while the $\overline{\text{LDAC}}$ pin and General Call Software Update command affect all channels.

5.6.5 WRITE COMMAND: SELECT VREF BIT (C2=1, C1=0, C0=0)

When the device receives this command, it updates the DAC voltage reference selection bit (V_{REF}) of each channel. The EEPROM data is not affected by this command. The affected channel's analog output is updated after the acknowledge pulse of the last byte. Figure 5-12 shows an example of the write command for Select V_{REF} bits.

5.6.6 WRITE COMMAND: SELECT POWER-DOWN BITS (C2=1, C1=0, C0=1)

When the device receives this command, it updates the Power-Down selection bits (PD1, PD0) of each channel. The EEPROM data is not affected by this command. The affected channel is updated after the acknowledge pulse of the last byte. Figure 5-13 shows an example of the write command for the Select Power-Down bits.

5.6.7 WRITE COMMAND: SELECT GAIN BIT (C2=1, C1=1, C0=0)

When the device receives this command, it updates the gain selection bits (G_X) of each channel. The EEPROM data is not affected by this command. The analog output is updated after the acknowledge pulse of the last byte. Figure 5-14 shows an example of the write command for select gain bits.

5.6.8 WRITE COMMAND: WRITE I²C ADDRESS BITS (C2=0, C1=1, C0=1)

This command writes new I²C address bits (A2, A1, A0) to the DAC input registers and EEPROM. When the device receives this command, it overwrites the current address bits with the new address bits.

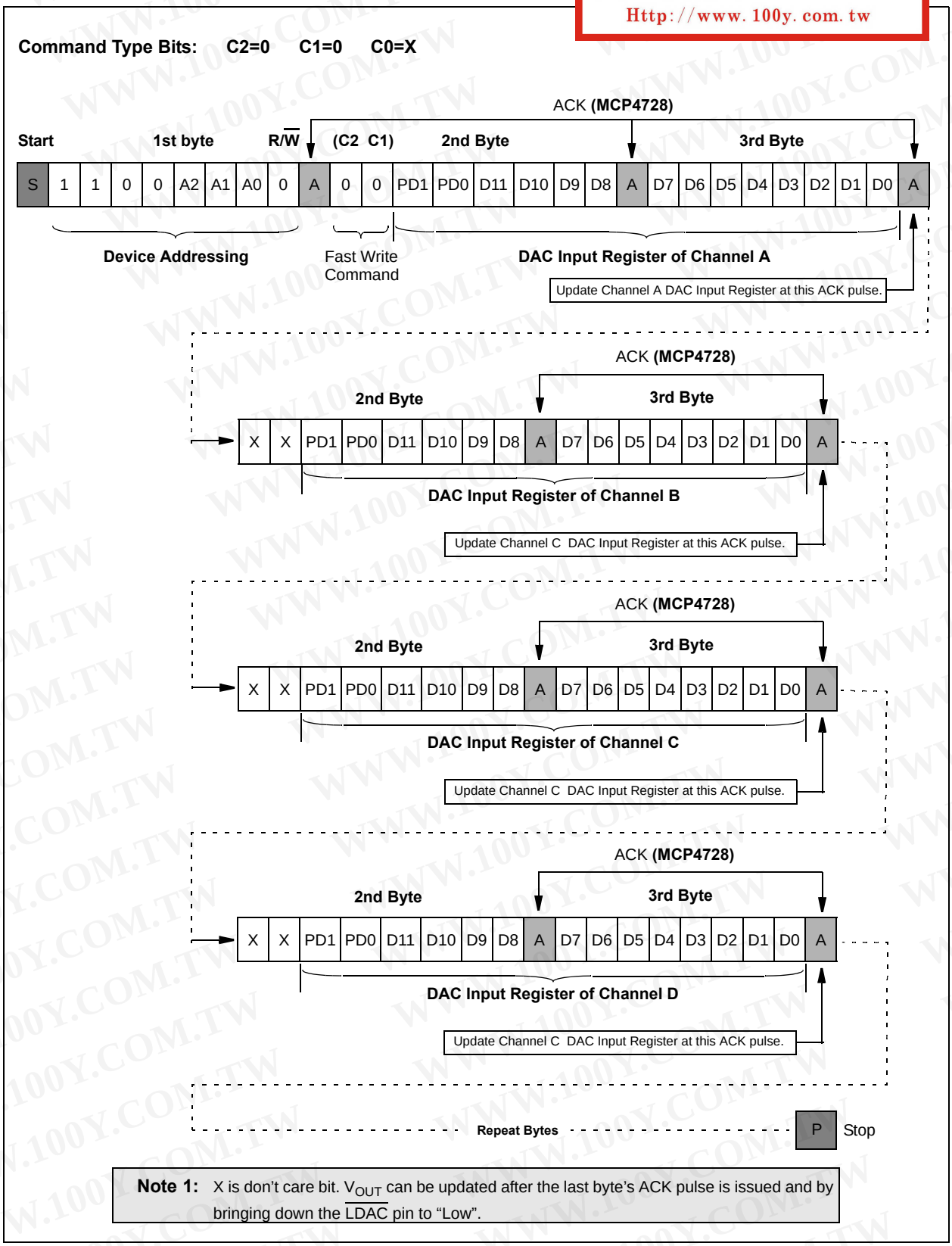
This command is valid only when the $\overline{LDAC}$ pin makes a transition from "High" to "Low" at the low time of the last bit (8th clock) of the second byte, and stays "Low" until the end of the 3rd byte. The update occurs after "Stop" bit if the conditions are met. The $\overline{LDAC}$ pin is used to select a device of interest to write. The highest clock rate of this command is 400 kHz. Figure 5-11 shows the details of the address write command.

Note 1: To write a new device address, it needs the current address of the device. The current address bits can be read out by sending General Call Read Address Bits command. See **5.4.4 "General call Read Address Bits"** for more details of reading the I²C address bits.

5.6.9 READ COMMAND

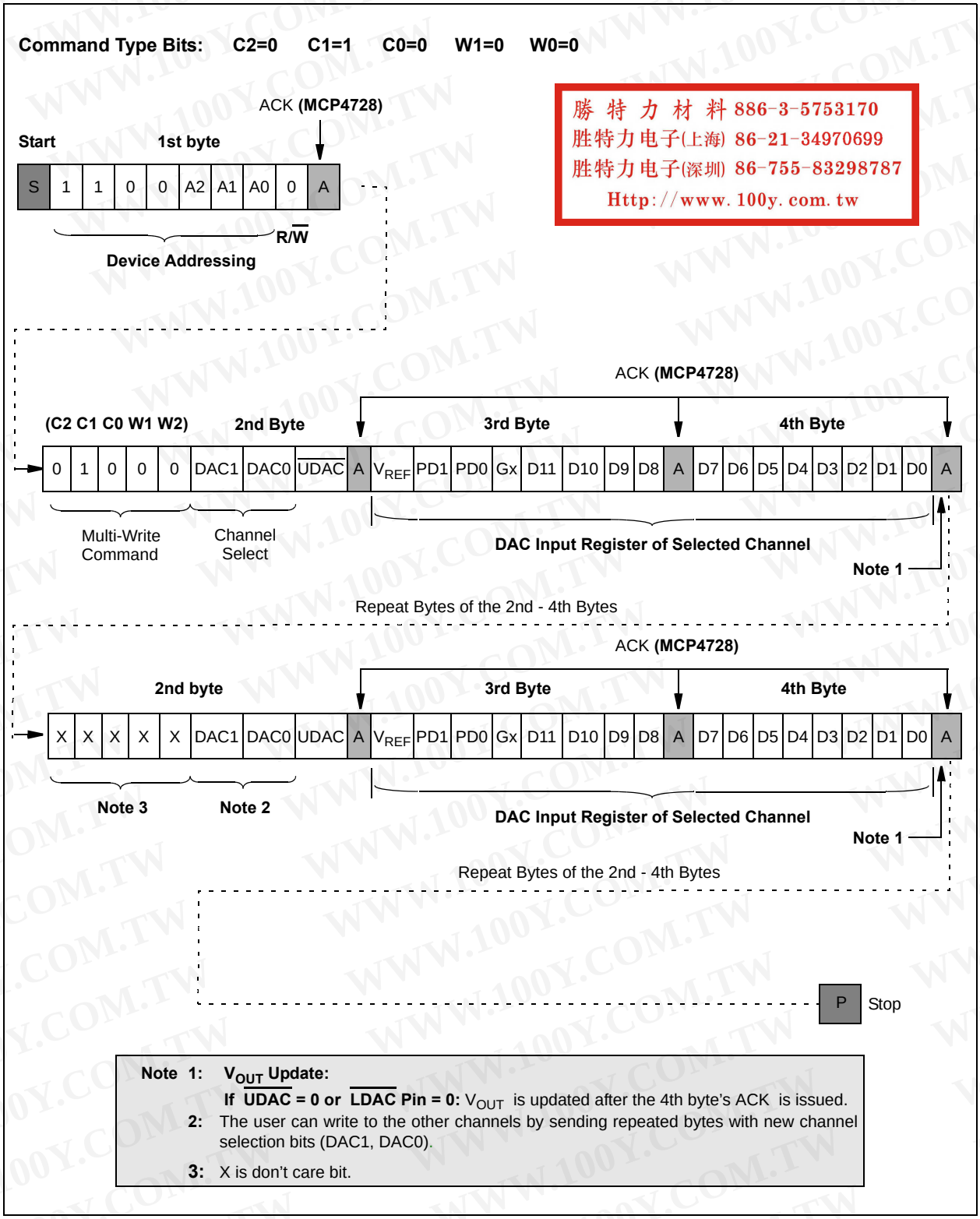
If the R/$\overline{W}$ bit is set to a logic "High" in the I²C serial communications command, the device enters a reading mode and reads out the input registers and EEPROM. Figure 5-15 shows the details of the read command.

Note 1: The device address bits are read by using General Call Read Address Bits command.



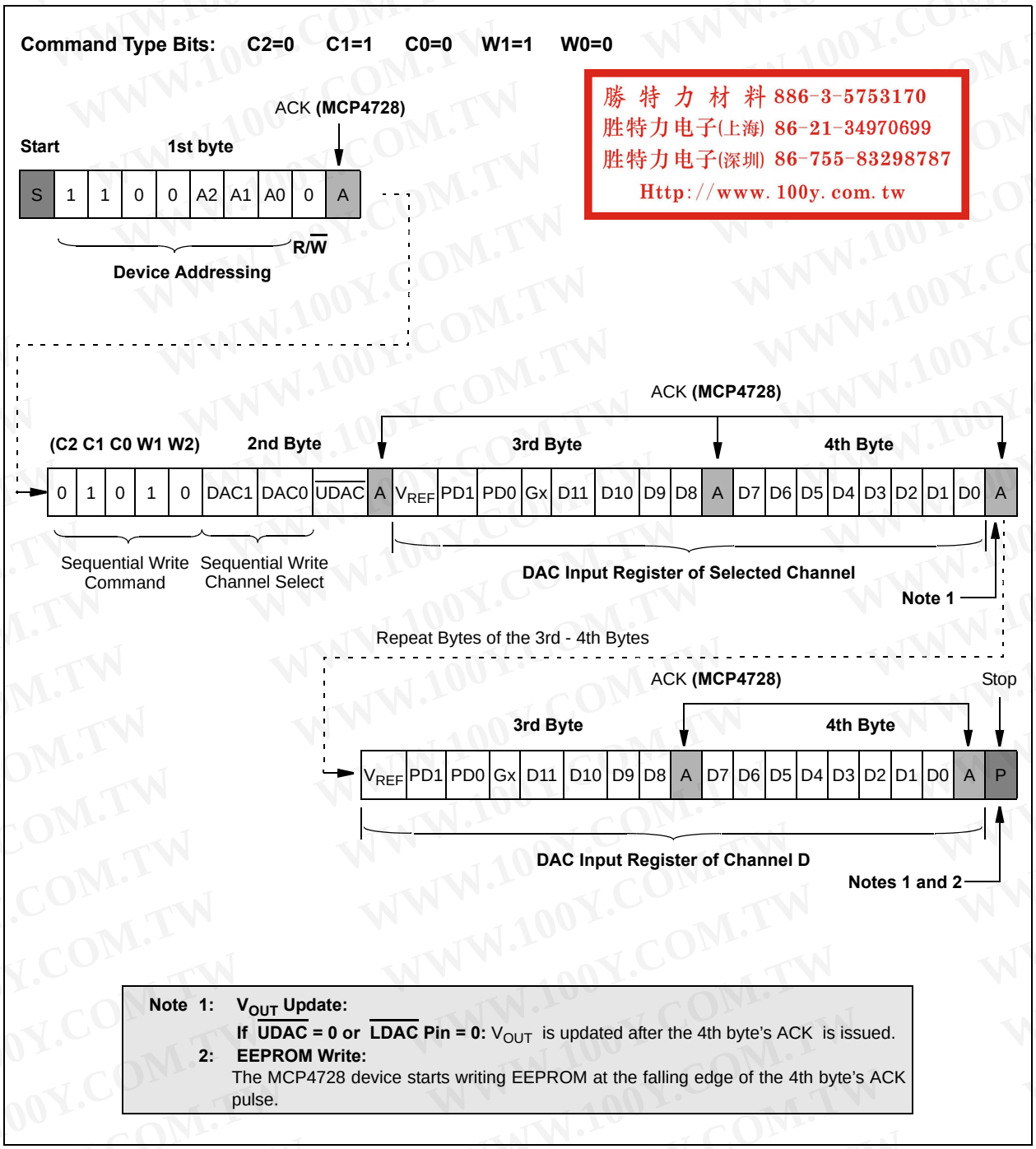
Note 1: X is don't care bit. V_{OUT} can be updated after the last byte's ACK pulse is issued and by bringing down the $\overline{LDAC}$ pin to "Low".

FIGURE 5-7: *Fast Write Command: Write DAC Input Registers Sequentially from Channel A to D.*



Note 1: **V_{OUT} Update:**
If $\overline{UDAC}$ = 0 or $\overline{LDAC}$ Pin = 0: V_{OUT} is updated after the 4th byte's ACK is issued.
2: The user can write to the other channels by sending repeated bytes with new channel selection bits (DAC1, DAC0).
3: X is don't care bit.

FIGURE 5-8: *Multi-Write Command: Write DAC Input Registers.*



Note 1: **V_{OUT} Update:**
If $\overline{\text{UDAC}}$ = 0 or $\overline{\text{LDAC}}$ Pin = 0: V_{OUT} is updated after the 4th byte's ACK is issued.

2: **EEPROM Write:**
The MCP4728 device starts writing EEPROM at the falling edge of the 4th byte's ACK pulse.

FIGURE 5-9: *Sequential Write Command: Write DAC Input Registers and EEPROM Sequentially from Starting Channel to Channel D. Note that this command can send up to 10 bytes including the device addressing and command bytes. Any byte after the 10th byte is ignored.*

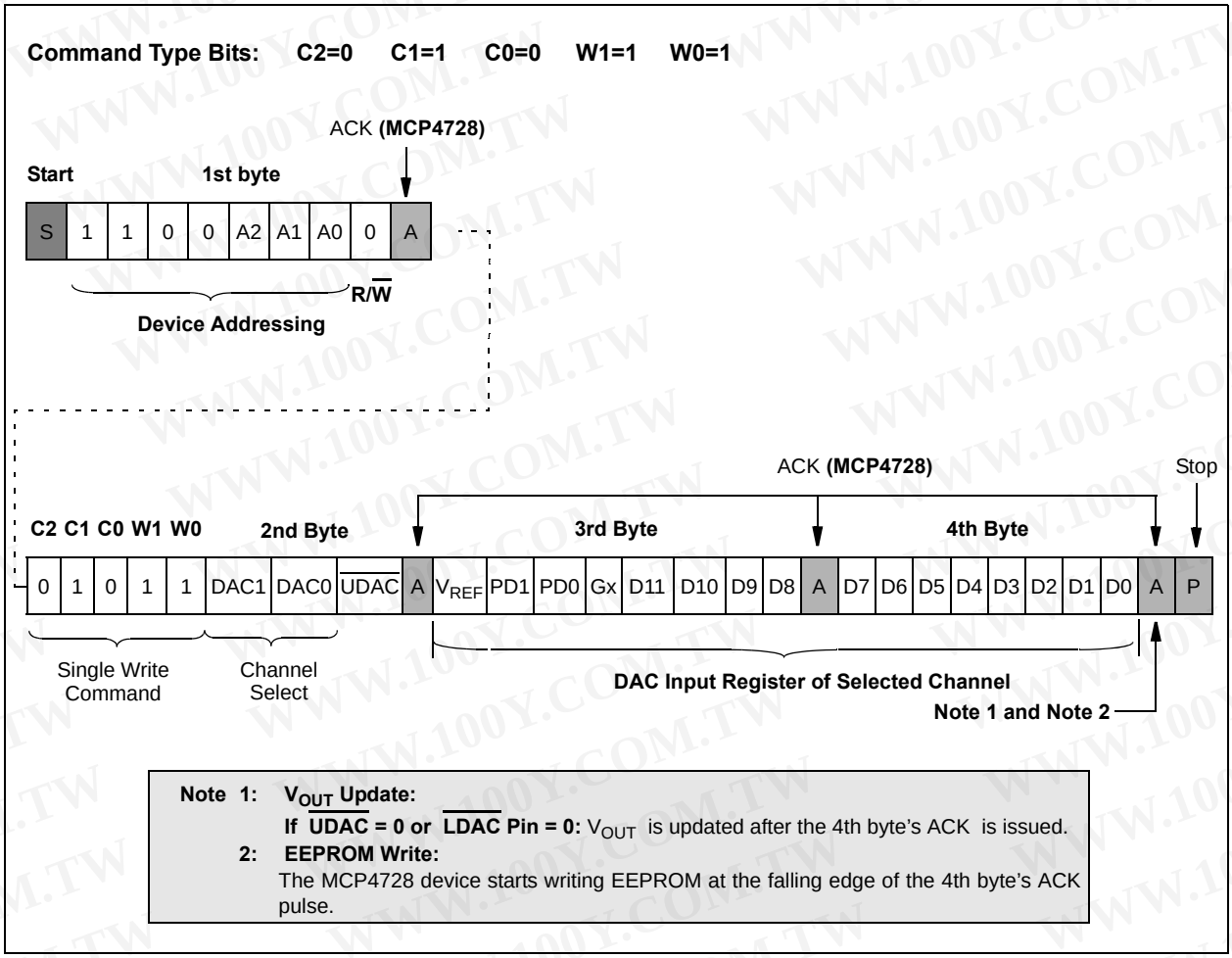
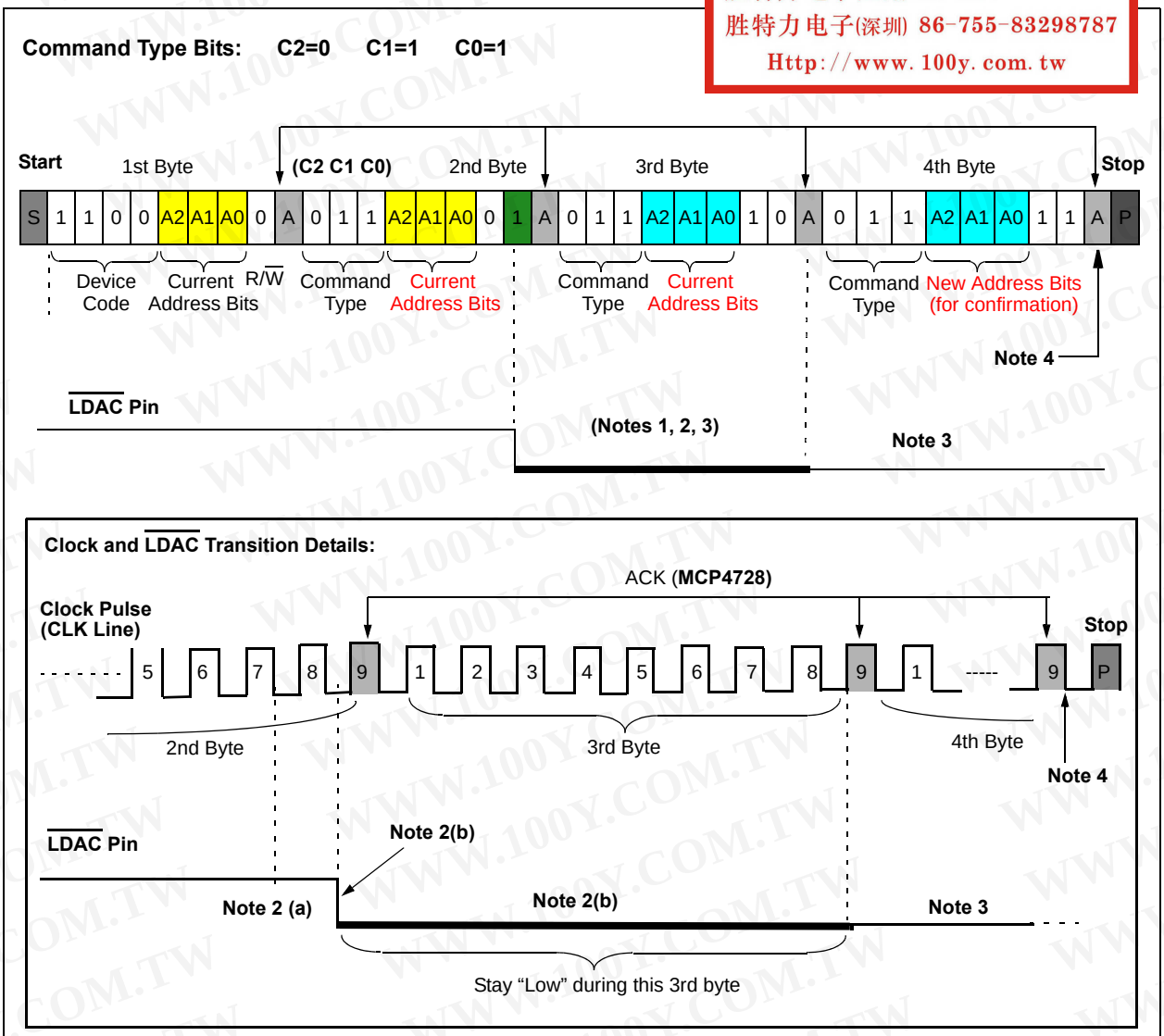


FIGURE 5-10: *Single Write Command: Write to a Single DAC Input Register and EEPROM.*



Note 1: Clock Pulse and LDAC Transition Details.

2: LDAC pin events at the 2nd and 3rd bytes.

a. Keep LDAC pin "High" until the end of the positive pulse of the 8th clock of the 2nd byte.

b. LDAC pin makes a transition from "High" to "Low" during the negative pulse of the 8th clock of the 2nd byte (just before the rising edge of the 9th clock), and stays "Low" until the rising edge of the 9th clock of the 3rd byte.

c. The MCP4728 device does not acknowledge the 3rd byte if the conditions (a) and (b) are not met.

3: LDAC pin resumes its normal function after "Stop" bit.

4: EEPROM Write/

a. Charge Pump initiates the EEPROM write sequence at the falling edge of the 4th byte's ACK pulse.

b. The RDY/BSY bit (pin) goes "Low" at the falling edge of this ACK clock and back to "High" immediately after the EEPROM write is completed.

FIGURE 5-11: *Write Command: Write I^2C Address Bits to the DAC Registers and EEPROM.*

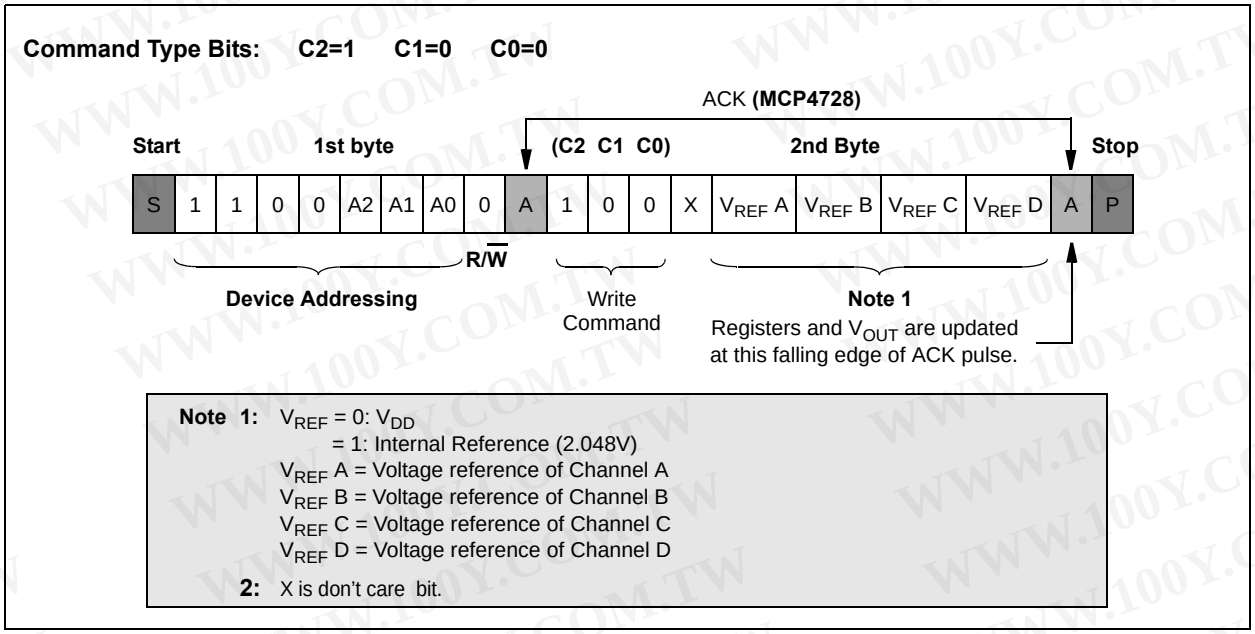


FIGURE 5-12: *Write Command: Write Voltage Reference Selection Bit (V_{REF}) to the DAC Input Registers.*

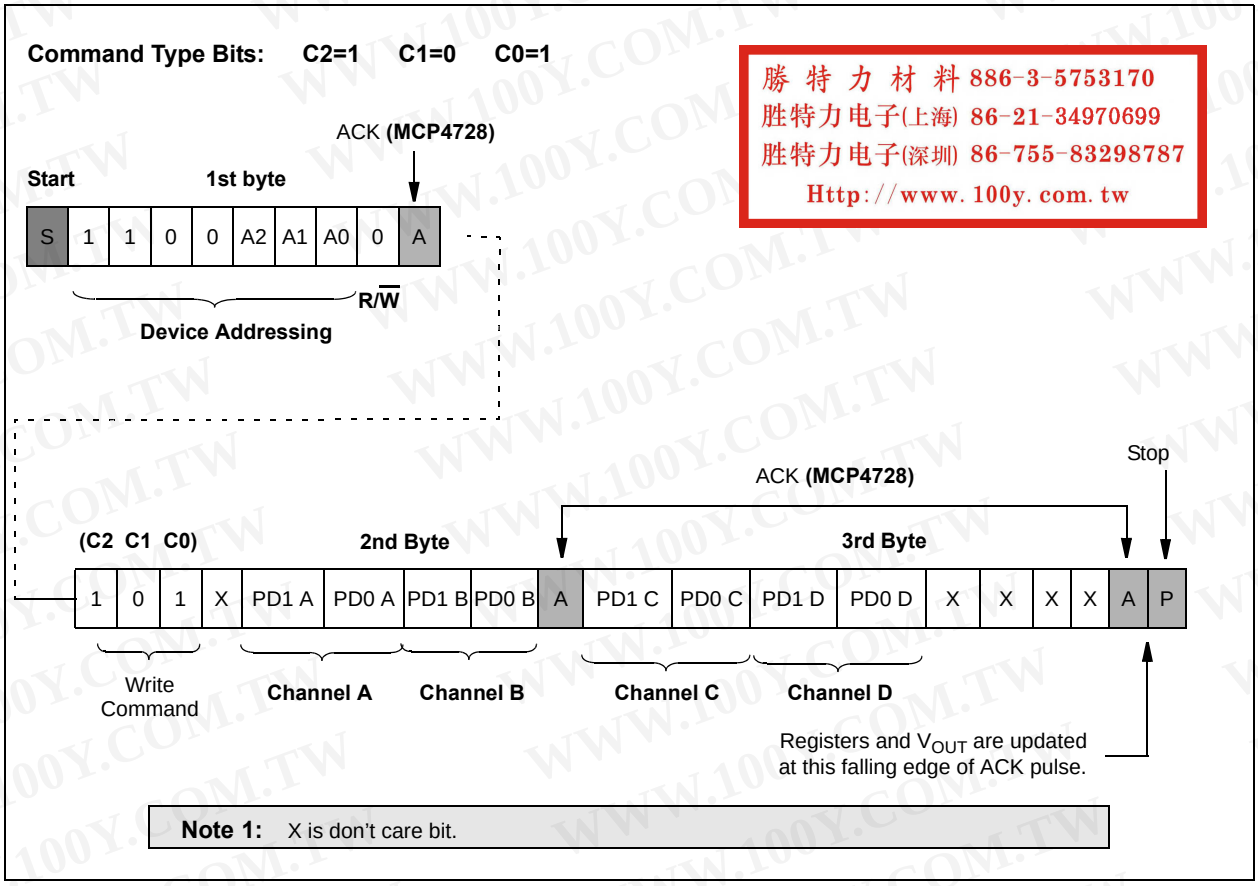


FIGURE 5-13: *Write Command: Write Power-Down Selection Bits (PD1, PD0) to the DAC Input Registers.*

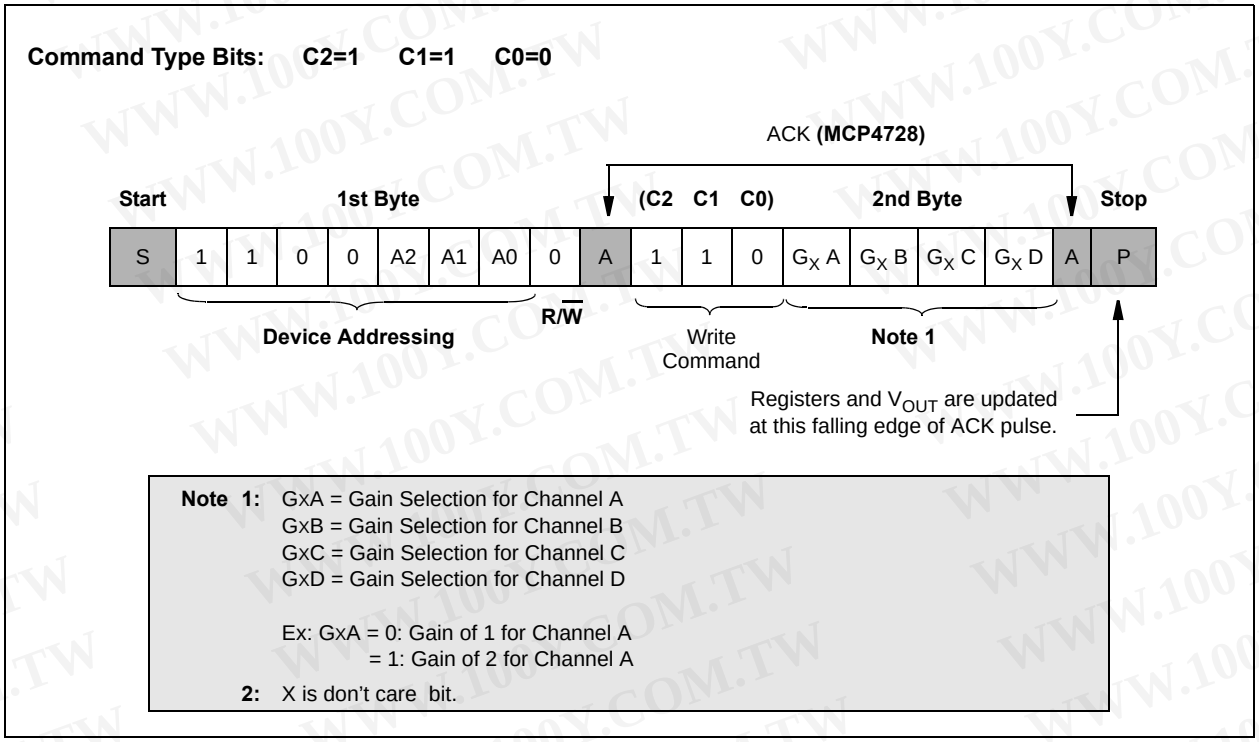
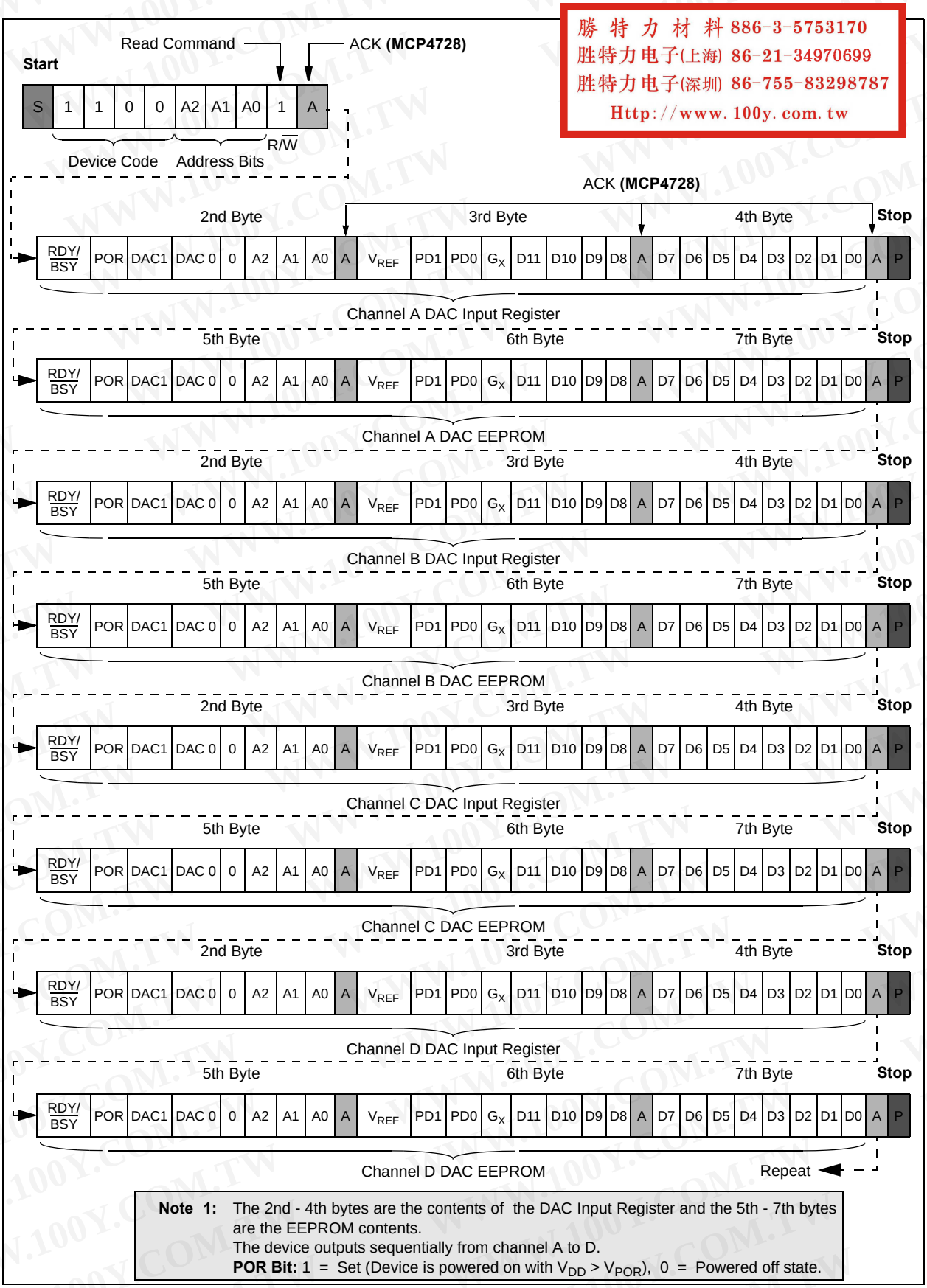


FIGURE 5-14: *Write Command: Write Gain Selection Bit (G_X) to the DAC Input Registers.*



Note 1: The 2nd - 4th bytes are the contents of the DAC Input Register and the 5th - 7th bytes are the EEPROM contents.
The device outputs sequentially from channel A to D.
POR Bit: 1 = Set (Device is powered on with $V_{DD} > V_{POR}$), 0 = Powered off state.

FIGURE 5-15: *Read Command and Device Outputs.*

NOTES:

6.0 TERMINOLOGY

6.1 Resolution

The resolution is the number of DAC output states that divide the full scale range. For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

6.2 LSB

The least significant bit or the ideal voltage difference between two successive codes.

EQUATION 6-1:

$$LSB = \frac{V_{REF}}{2^n}$$

$$= \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{2^{12} - 1}$$

$$= \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{4095}$$

Where

V_{REF} = V_{DD} If external reference is selected

= 2.048V If internal reference is selected

n = The number of digital input bits, n = 12 for MCP4728.

6.3 Integral Nonlinearity (INL)

Integral nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line). In the MCP4728, INL is calculated using two end-points (zero and full scale). INL can be expressed as a percentage of full scale range (FSR) or in fraction of an LSB. INL is also called relative accuracy. Equation 6-2 shows how to calculate the INL error in LSB and Figure 6-1 shows an example of INL accuracy.

EQUATION 6-2: INL ERROR

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

INL is expressed in LSB

V_{Ideal} = Code*LSB

V_{OUT} = The output voltage measured at the given input code

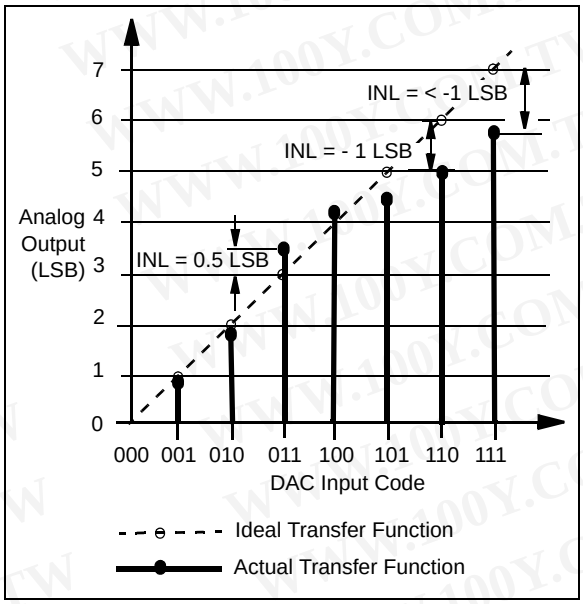


FIGURE 6-1: *INL Accuracy.*

6.4 Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) error (see Figure 6-2) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSB. A DNL error of zero would imply that every code is exactly 1 LSB wide. If the DNL error is less than 1 LSB, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

EQUATION 6-3: DNL ERROR

$$DNL = \frac{\Delta V_{OUT} - LSB}{LSB}$$

Where:

DNL is expressed in LSB.

ΔV_{OUT} = The measured DAC output voltage difference between two adjacent input codes.

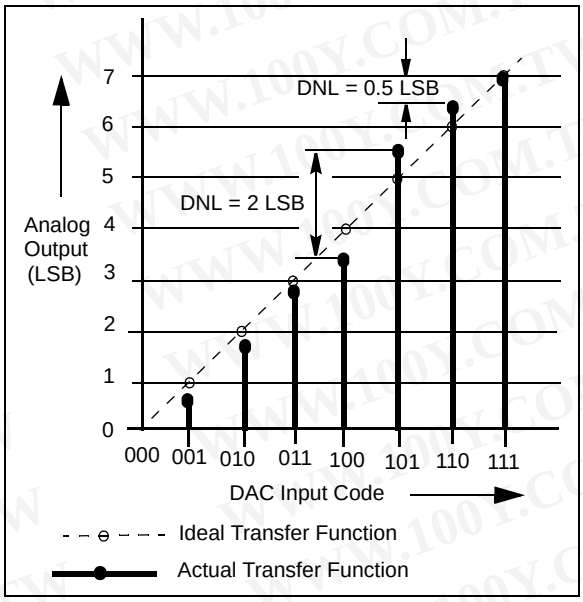


FIGURE 6-2: *DNL Accuracy.*

6.5 Offset Error

Offset error (see Figure 6-3) is the deviation from zero voltage output when the digital input code is zero (zero scale voltage). This error affects all codes by the same amount. For the MCP4728 device, the offset error is not trimmed at the factory. However, it can be calibrated by software in application circuits.

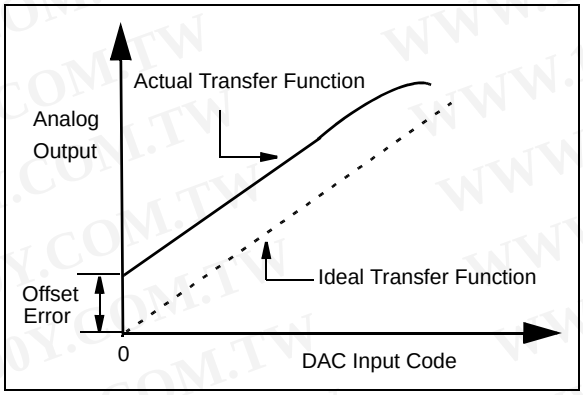


FIGURE 6-3: *Offset Error.*

6.6 Gain Error

Gain error (see Figure 6-4) is the difference between the actual full scale output voltage from the ideal output voltage of the DAC transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full scale range (% of FSR) or in LSB.

For the MCP4728 device, the gain error is not calibrated at the factory and most of the gain error is contributed by the output buffer (op amp) saturation near the code range beyond 4000. For applications that need the gain error specification less than 1% maximum, a user may consider using the DAC code range between 100 and 4000 instead of using full code range (code 0 to 4095). The DAC output of the code range between 100 and 4000 is much more linear than full scale range (0 to 4095). The gain error can be calibrated out by software in applications.

6.7 Full Scale Error (FSE)

Full scale error (see Figure 6-4) is the sum of offset error plus gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh).

EQUATION 6-4:

$$FSE = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

FSE is expressed in LSB.

V_{Ideal} = (V_{REF}) (1 - 2^{-n}) - Offset Voltage (V_{OS})

V_{REF} = Voltage Reference

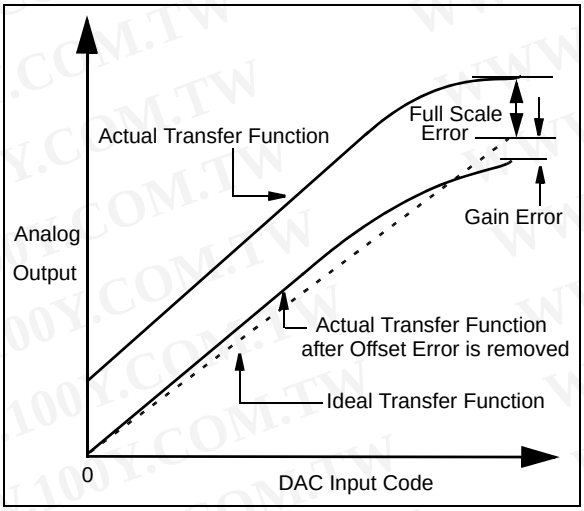


FIGURE 6-4: *Gain Error and Full Scale Error.*

6.8 Gain Error Drift

Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C.

6.9 Offset Error Drift

Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/^{o}C.

6.10 Settling Time

The Settling time is the time delay required for the DAC output to settle to its new output value from the start of code transition, within specified accuracy. In the MCP4728 device, the settling time is a measure of the time delay until the DAC output reaches its final value within 0.5 LSB when the DAC code changes from 400h to C00h.

6.11 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec. and is measured when the digital code is changed by 1 LSB at the major carry transition (Example: 011...111 to 100... 000, or 100... 000 to 011... 111).

6.12 Digital Feedthrough

Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec, and is measured with a full scale change (Example: all 0s to all 1s and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register. This condition can be created by writing input register with both $\overline{\text{UDAC}}$ bit and $\overline{\text{LDAC}}$ pin high.

6.13 Analog Crosstalk

Analog crosstalk is the glitch that appears at the output of one DAC due to a change in the output of the other DAC. The area of the glitch is expressed in nV-Sec, and measured by loading one of the input registers with a full scale code change (all 0s to all 1s and vice versa) while keeping both $\overline{\text{UDAC}}$ bit and $\overline{\text{LDAC}}$ pin high. Then bring down the $\overline{\text{LDAC}}$ pin to low and measure the output of the DAC whose digital code was not changed.

6.14 DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch that appears at the output of one DAC due to an input code change and subsequent output change of the other DAC. This includes both digital and analog crosstalks. The area of the glitch is expressed in nV-Sec, and measured by loading one of the input registers with a full scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{UDAC}}$ bit or $\overline{\text{LDAC}}$ pin low.

6.15 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full scale output of the DAC. It is measured on one DAC that is using an internal V_{REF} while the V_{DD} is varied +/- 10%, and expressed in dB or µV/V.

NOTES:

7.0 TYPICAL APPLICATIONS

The MCP4728 device is a part of Microchip's latest DAC family with non-volatile EEPROM memory. The device is a general purpose resistor string DAC intended to be used in applications where a precision, and low power DAC with moderate bandwidth is required.

Since the device includes non-volatile EEPROM memory, the user can use this device for applications that require the output to return to the previous set-up value on subsequent power-ups.

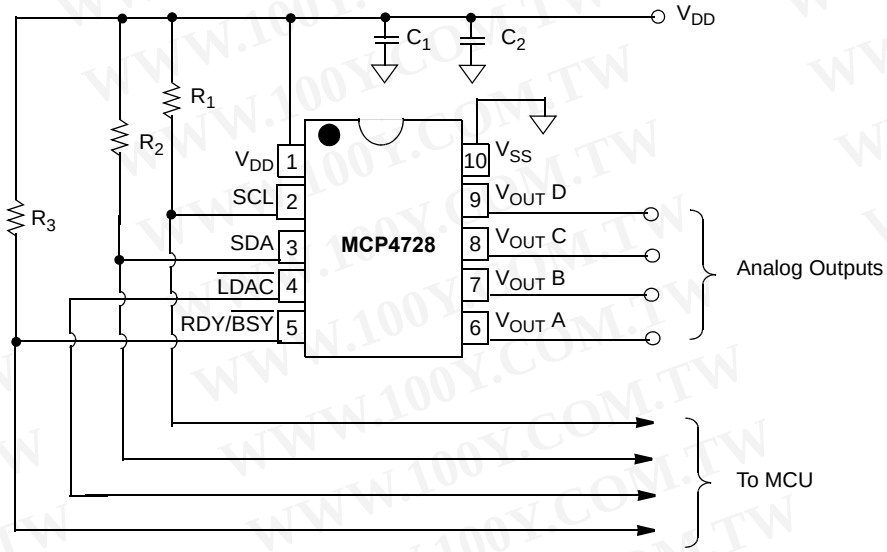
Applications generally suited for the MCP4728 device family include:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery Powered)
- Motor Speed Control

7.1 Connecting to I²C BUS using Pull-Up Resistors

The SCL, SDA, and RDY/$\overline{BSY}$ pins of the MCP4728 device are open-drain configurations. These pins require a pull-up resistor as shown in Figure 7-1. The $\overline{LDAC}$ pin has a schmitt trigger input configuration and it can be driven by an external MCU I/O pin.

The pull-up resistor values (R1 and R2) for SCL and SDA pins depend on the operating speed (standard, fast, and high speed) and loading capacitance of the I²C bus line. Higher value of pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. A lower resistor value, on the other hand, consumes higher power, but allows for higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for standard and fast modes, and less than 1 kΩ for high speed mode.



R_1 - R_3 are the pull-up resistors:

R_1 and R_2:

5 kΩ - 10 kΩ for f_{SCL} = 100 kHz to 400 kHz

~700Ω for f_{SCL} = 3.4 MHz

R_3: ~ 100 kΩ

C_1: 0.1 µF, Ceramic capacitor

C_2: 10 µF, Tantalum capacitor

FIGURE 7-1: *Example of the MCP4728 Device Connection.*

7.1.1 DEVICE CONNECTION TEST

The user can test the presence of the MCP4728 device on the I^2C bus line without performing a data conversion. This test can be achieved by checking an acknowledge response from the MCP4728 device after sending a read or write command. Figure 7-2 shows an example with a read command:

a. Set the R/$\overline{W}$ bit “High” or “Low” in the address byte.
b. Check the ACK pulse after sending the address byte.
   If the device acknowledges (ACK = 0) the command, then the device is connected, otherwise it is not connected.
c. Send Stop bit.

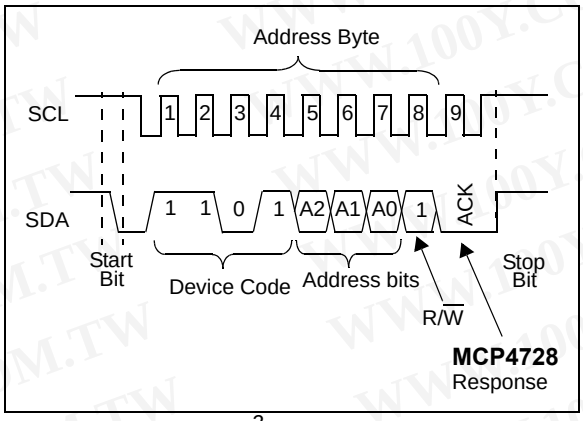


FIGURE 7-2: *I^2C Bus Connection Test.*

7.2 Layout Considerations

Inductively-coupled AC transients and digital switching noise from other devices can affect DAC performance and DAC output signal integrity. Careful board layout will minimize these effects. Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving good DAC performance.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors of the MCP4728 should be terminated to the analog ground plane.

7.3 Power Supply Considerations

The power source should be as clean as possible. The power supply to the device is used for both V_{DD} and DAC voltage reference by selecting $V_{REF} = V_{DD}$. Any noise induced on the V_{DD} line can affect DAC performance. A typical application will require a bypass capacitor in order to filter out high frequency noise on the V_{DD} line. The noise can be induced onto the power supply’s traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 7-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the MCP4728 device should reside on the analog plane.

7.4 Using Power Saving Feature

The device consumes very little power when it is in Power-Down (shut-down) mode. During the Power-Down mode, most circuits in the selected channel are turned off. It is recommended to power down any unused channel.

The device consumes the least amount of power if it enters the Power-Down mode after the internal voltage reference is disabled. This can be achieved by selecting V_{DD} as the voltage reference for all 4 channels and then issuing the Power-Down mode for all channels.

7.5 Using Non-Volatile EEPROM Memory

The user can store the I^2C device address bits, configuration bits and DAC input code of each channel in the on-board non-volatile EEPROM memory using the I^2C write command. The contents of EEPROM are readable and writable using the I^2C command.

When the MCP4728 device is first powered-up or receives General Call Reset Command, it uploads the EEPROM contents to the DAC output registers automatically and provides analog outputs immediately with the saved settings in EEPROM. This feature is very useful in applications where the MCP4728 device is used to provide set points or calibration data for other devices in the application systems. The MCP4728 device can save important system parameters when the application system experiences power failure. See **Section 5.5 “Writing and Reading Registers and EEPROM”** for more details of using the non-volatile EEPROM memory.

7.6 Application Examples

The MCP4728 device is a rail-to-rail output DAC designed to operate with a V_{DD} range of 2.7V to 5.5V. Its output amplifier of each channel is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of external buffers for most applications. Since each channel has its own configuration bits for selecting the voltage reference, gain, power-down, etc., the MCP4728 device offers great simplicity and flexibility to use for various DAC applications.

7.6.1 DC SET POINT OR CALIBRATION VOLTAGE SETTINGS

A common application for the MCP4728 device is a digitally-controlled set point or a calibration of variable parameters such as sensor offset or bias point. Figure 7-3 shows an example of the set point settings.

Let us consider that the application requires different trip voltages (Trip 1 - Trip 4). Assuming the DAC output voltage requirements are given as shown in Table 7-1, examples of sending the Sequential Write and Fast Write commands are shown in Figure 7-4 and Figure 7-5.

TABLE 7-1: EXAMPLE: SETTING V_{OUT} OF EACH CHANNEL

DAC Channel	Voltage Reference	DAC Output (V_{OUT})
V_{OUT} A	V_{DD}	$V_{DD}/2$
V_{OUT} B	V_{DD}	V_{DD} - 1 LSB
V_{OUT} C	Internal	2.048V
V_{OUT} D	Internal	4.096V

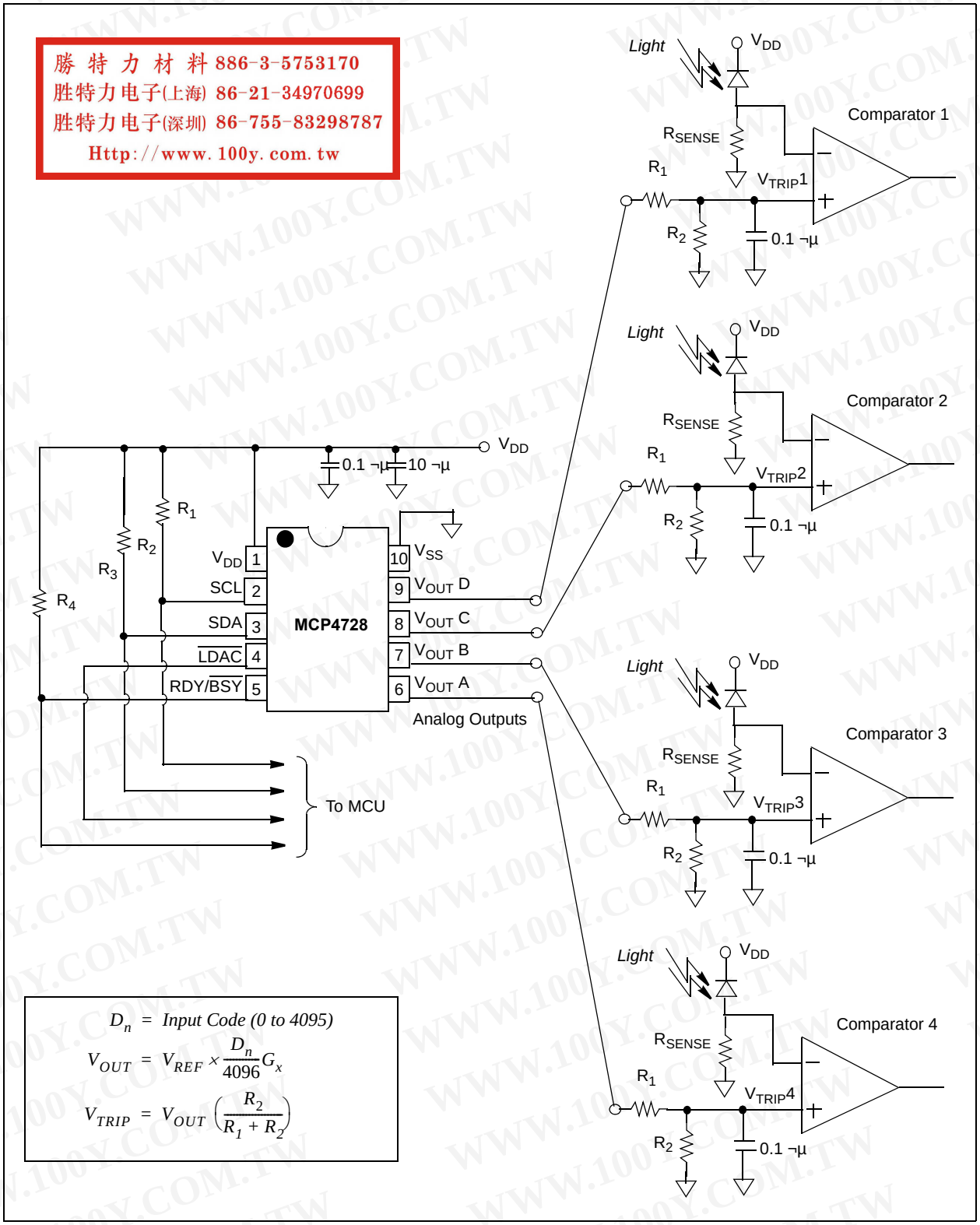
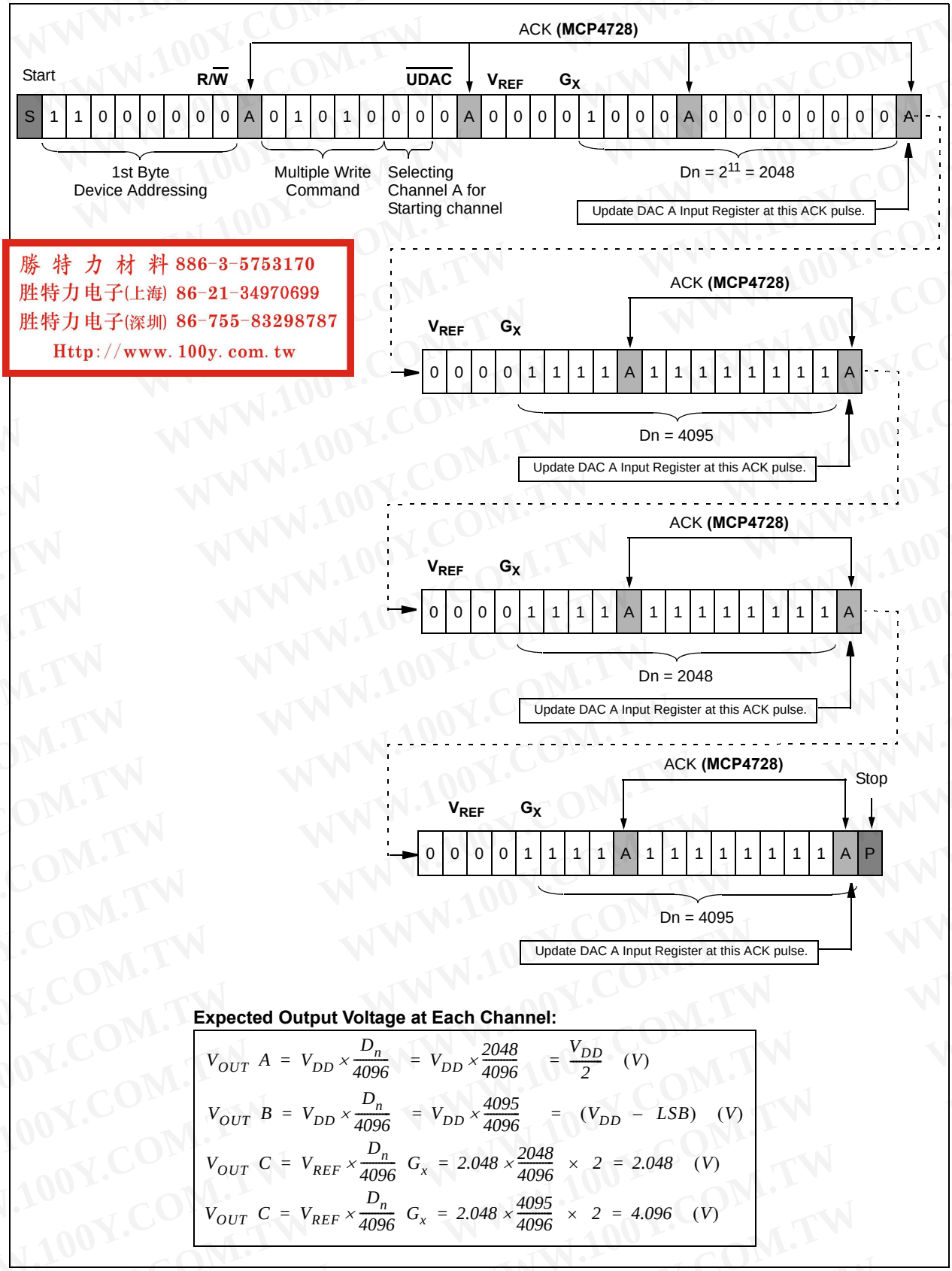


FIGURE 7-3: *Using the MCP4728 for Set Point or Threshold Calibration.*



Expected Output Voltage at Each Channel:

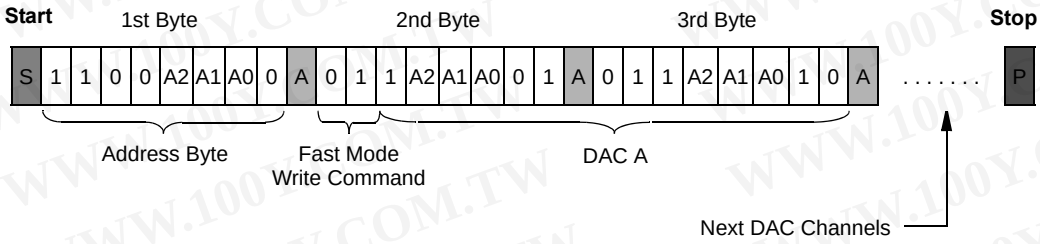
$$V_{OUT}\ A = V_{DD} \times \frac{D_n}{4096} = V_{DD} \times \frac{2048}{4096} = \frac{V_{DD}}{2} \quad (V)$$

$$V_{OUT}\ B = V_{DD} \times \frac{D_n}{4096} = V_{DD} \times \frac{4095}{4096} = (V_{DD} - LSB) \quad (V)$$

$$V_{OUT}\ C = V_{REF} \times \frac{D_n}{4096}\ G_x = 2.048 \times \frac{2048}{4096} \times 2 = 2.048 \quad (V)$$

$$V_{OUT}\ C = V_{REF} \times \frac{D_n}{4096}\ G_x = 2.048 \times \frac{4095}{4096} \times 2 = 4.096 \quad (V)$$

FIGURE 7-4: *Sequential Write Command for Setting Test Points in Figure 7-3.*



The following example shows the expected analog outputs with the corresponding DAC input codes:

DAC A Input Code = 001111-11111111
DAC B Input Code = 000111-11111111
DAC C Input Code = 000011-11111111
DAC D Input Code = 000001-11111111

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{4096} G_x$$

(A) Channel A Output:

Dn for Channel A = 0FFF (hex) = 4095 (decimal)

$$V_{OUT\ A} = \frac{(V_{DD} \times 4095)}{4096} = V_{DD}\left(\frac{4096-1}{4096}\right) = V_{DD}\left(1-\frac{1}{4096}\right) = V_{DD} - LSB$$

(B) Channel B Output:

Dn for Channel B = 07FF (hex) = 2047 (decimal)

$$V_{OUT\ B} = \frac{(V_{DD} \times 2047)}{4096} = V_{DD}\left(\frac{2048-1}{4096}\right) = \frac{V_{DD}}{2}\left(1-\frac{2}{4096}\right) = \frac{V_{DD}}{2} - LSB$$

(C) Channel C Output:

Dn for Channel C = 03FF (hex) = 1023 (decimal)

$$V_{OUT\ C} = \frac{V_{DD} \times 1023}{4096} = V_{DD}\left(\frac{1024-1}{4096}\right) = \frac{V_{DD}}{4}\left(1-\frac{4}{4096}\right) = \frac{V_{DD}}{4} - LSB$$

(D) Channel D Output:

Dn for Channel D = 01FF (hex) = 511 (decimal)

$$V_{OUT\ D} = \frac{V_{DD} \times 511}{4096} = V_{DD}\left(\frac{512-1}{4096}\right) = \frac{V_{DD}}{8}\left(1-\frac{8}{4096}\right) = \frac{V_{DD}}{8} - LSB$$

FIGURE 7-5: *Example of Writing Fast Write Command for Various V_{OUT}. $V_{REF} = V_{DD}$ for all Channels.*

8.0 DEVELOPMENT SUPPORT

8.1 Evaluation & Demonstration Boards

The MCP4728 Evaluation Board is available from Microchip Technology Inc. This board works with Microchip's PICkit™ Serial Analyzer. The user can easily program the DAC input registers and EEPROM using the PICkit Serial Analyzer, and test out the DAC analog output voltages.The PICkit Serial Analyzer uses the PC Graphic User Interface software. Refer to www.microchip.com for further information on this product's capabilities and availability.

FIGURE 8-1: *MCP4728 Evaluation Board.*

FIGURE 8-2: *Setup for the MCP4728 Evaluation Board with PICkit™ Serial Analyzer.*

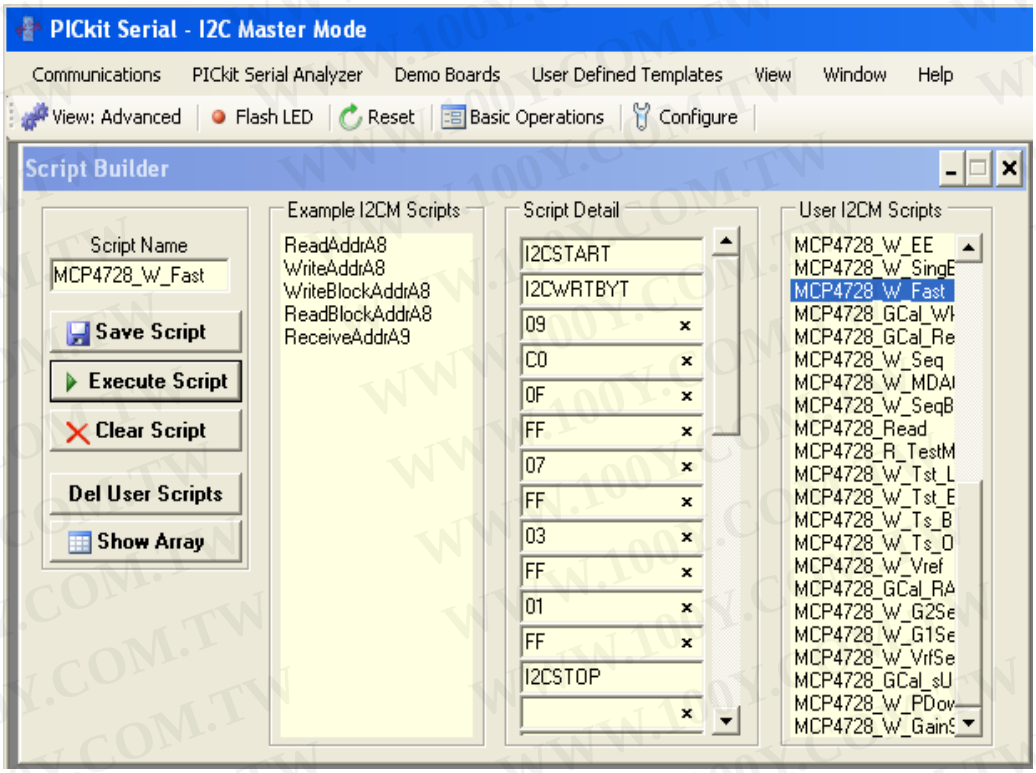


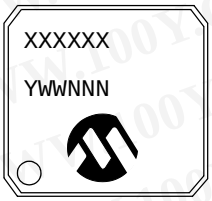
FIGURE 8-3: *Example of PICkit™ Serial User Interface.*

NOTES:

9.0 PACKAGING INFORMATION

9.1 Package Marking Information

10-Lead MSOP



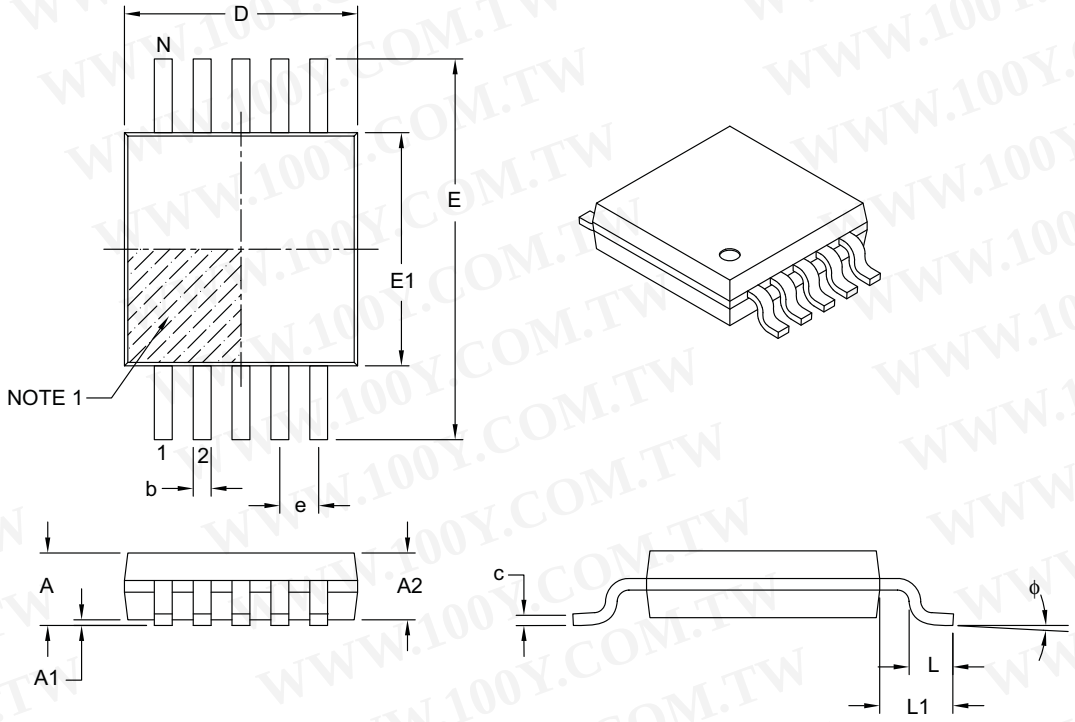
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.15	–	0.33

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

APPENDIX A: REVISION HISTORY

Revision A (June 2009)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	,	X	/XX
Device		Temperature Range	Package

Device:	MCP4728:	Single Comparator
Temperature Range:	E =	-40°C to +125°C
Package:	UN =	Plastic Micro Small Outline Transistor, 10-lead

Examples:

a) MCP4728: Tape and Reel, Extended Temperature, 10LD MSOP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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