#### TLV1572 2.7 V TO 5.5 V, 10-BIT, 1.25 MSPS SERIAL ANALOG-TO-DIGITAL CONVERTER WITH AUTO-POWERDOWN SLAS171A – DECEMBER 1997 – REVISED SEPTEMBER 1998

- Fast Throughput Rate: 1.25 MSPS
- 8-Pin SOIC Package
- Differential Nonlinearity Error: < ±1 LSB
- Integral Nonlinearity Error: < ±1 LSB
- Signal-to-Noise and Distortion Ratio: 59 dB, f<sub>(input)</sub> = 500 kHz
- Single 3-V to 5-V Supply Operation
- Very Low Power: 8 mW at 3V; 25mW at 5 V
- Auto-Powerdown: 10 μA Maximum
- Glueless Serial Interface to TMS320 DSPs and (Q)SPI Compatible Micro-Controllers
- Inherent Internal Sample and Hold Operation

#### Applications

- Mass Storage and HDD
- Automotive
- Digital Servos
- Process Control
- General Purpose DSP
- Contact Image Sensor Processing

#### description

The TLV1572 is a high-speed 10-bit successive-approximation analog-to-digital converter (ADC) that operates from a single 2.7-V to 5.5-V power supply and is housed in a small 8-pin SOIC package.

The TLV1572 accepts an analog input range from 0 to V<sub>CC</sub> and digitizes the input at a maximum 1.25 MSPS throughput rate. The power dissipation is only 8 mW with a 3-V supply or 25 mW with a 5-V supply. The device features an auto-powerdown mode that automatically powers down to 10  $\mu$ A whenever a conversion is not performed.

The TLV1572 communicates with digital microprocessors via a simple 3- or 4-wire serial port that interfaces directly to the Texas Instruments TMS320 DSPs and (Q)SPI compatible microcontrollers without using additional glue logic.

Very high throughput rate, simple serial interface, SO-8 package, 3-V operation, and low power consumption make the TLV1572 an ideal choice for compact or remote high-speed systems.

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	PACKAGE
TA	SMALL OUTLINE (D)
0°C to 70°C	TLV1572CD
-40°C to 85°C	TLV1572ID

AVAILABLE OPTIONS



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



D PACKAGE (TOP VIEW) CS 1 8 DO VREF 2 7 FS GND 3 6 V<sub>CC</sub> AIN 4 5 SCLK

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#### functional block diagram



#### **Terminal Functions**

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TERMINAI NAME	NO.	1/0	DESCRIPTION
AIN	4	0	Analog input
CS/Powerdown	104	c <sub>07</sub>	Chip Select. A low on this input enables the TLV1572. A high disables the device and disconnects the power to the TLV1572.
DO	8	0	Serial data output. A/D conversion results are provided at this output pin.
FS	N.70 N.10	O.Y.C	Frame sync input in DSP mode. The falling edge of the frame sync pulse from DSP indicates the start of a serial data frame shifted out of the TLV1572. The FS input is tied to V <sub>CC</sub> when interfacing to a micro-controller.
GND	3	10 -	Ground
SCLK	5	1007	Serial clock input. This clock synchronizes the serial data transfer and is also used for internal data conversion.
V <sub>CC</sub>	6	1.700	Power supply, recommend connection to analog supply
VREF	2	A. 1.	Reference voltage input. The voltage applied to this pin defines the input span of the TLV1572.

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#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage, GND to V <sub>CC</sub>	0.3 V to 6.5 V
Analog input voltage range	-0.3 V to V <sub>CC</sub> + 0.3 V
Reference input voltage	V <sub>CC</sub> + 0.3 V
Digital input voltage range	-0.3 V to V <sub>CC</sub> + 0.3 V
Operating virtual junction temperature range, T <sub>J</sub>	40°C to 150°C
Operating free-air temperature range, T <sub>A</sub>	0°C to 70°C
Storage temperature range, T <sub>stg</sub>	$\dots -65^{\circ}C$ to $150^{\circ}C$
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

NWW.100Y.CO † Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# recommended operating conditions 1007.0

power supply	
100x. CC MITH MARILOUX.L	MIN NOM M
V <sub>CC</sub> Supply voltage	2.7

### analog inputs

10	OX.CO. ITW	WW JIOOX. COM.TW	W	MIN	MAX	UNIT
VAIN	Analog input voltage	WWWWWWWWWWWWWW	WWW TOOY.C	GND	VREF	V
VREF	Reference input voltage	WWW.LU NY CONT	WWW.	2.7	Vcc	V

# digital inputs

TWW.10 N COM	WWW. OV.COM WWW	MIN	NOM	MAX	UNIT
High-level input voltage, VIH	$V_{CC} = 3 V \text{ to } 5.5 V$	2.1	2.4	$D_{M^{-1}}$	V
Low-level input voltage, VIL	V <sub>CC</sub> = 3 V to 5.5 V	W.1	<b>U Y</b> .	0.8	V
Input SCLK frequency	$V_{CC} = 4.5 V \text{ to } 5.5 V$		001.0	20	MHZ
SCLK pulse duration, clock high, tw(SCLKH)	$V_{CC} = 4.5 V \text{ to } 5.5 V$	23	Yoo.	COr	ns
SCLK pulse duration, clock low, tw(SCLKL)	$V_{CC} = 4.5 V \text{ to } 5.5 V$	23	.10-		ns
Input SCLK frequency	V <sub>CC</sub> = 3 V		N.100	10	MHZ
SCLK pulse duration, clock high, tw(SCLKH)	V <sub>CC</sub> = 3 V	45	100	Y.0	ns
SCLK pulse duration, clock low, tw(SCLKL)	$V_{CC} = 3 V$	45		N.C	ns

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### electrical characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V, WWW.100Y.C V<sub>REF</sub> = 5 V, f<sub>SCLK</sub> = 20 MHz (unless otherwise noted) T100X.COM.T

# digital specifications

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
Logic i	nputs	WWW.L	ON.		
III.	High-level input current	V <sub>CC</sub> = 5 V	-50	50	μA
ĺΓ	Low-level input current	V <sub>CC</sub> = 5 V	-50	50	μA
C <sub>i</sub>	input capacitance	YOOL WWW	5		pF
Logic o	outputs	NV. WWW.	V.COm		
Vон	High-level output voltage	$I_{OH} = 50 \ \mu A - 0.5 \ m A$	Vcc-0	.4	V
VOL	Low-level output voltage	$I_{OL} = 50 \ \mu A - 0.5 \ m A$	0.4		V
loz	High-impedance-state output current	AM WWW	-50	50	μΑ
CO	Output capacitance	COM. MAN.	5	W	pF

# dc specifications

W.Ive	PARAMETER	TEST CONDITIONS	MIN	ГҮР М.	AX	UNIT
-W.100	Resolution	COM.		10	<b>N</b>	Bits
Accuracy	OX.CONTRACTION NOTIO	NT. WI.INC.	100	.Mo		
INL	Integral nonlinearity	Best fit	1100X.+	0.5	±1	LSB
DNL	Differential nonlinearity	WW WITHOUND	<u>t</u>	0.3	±1	LSB
NT.	Offset error	The CONT of the State	4.10°_±	:0.1 ±0.	.15	%FSR
MW.	Gain error	1003. ONLT	W.100±	:0.1 ±	0.2	%FSR
Analog inpu	ut 00. COM WW	W WILLOUIS	100	N.0-	M	IN
W	Input full scale range	W. COM	GND	< V	CC	V
	Input capacitance	NW.ICOM.	NWW.L	15	<b>O</b>	pF
N.	input leakage current	$V_{AIN} = 0$ to $V_{CC}$	WIT	Ino -	50	μA
Voltage refe	erence input	WT. 100Y. CONTRA	W.	100%		M
VREF+	Positive reference voltage	NWW ONLOUM TW	3	V	CC	V
Vref-	Negative reference voltage	Internally connects to GND	G	GND	1	V
	Input resistance	W.100 COM. 1	2	W.IO		KΩ
	Input capacitance	WIT. 100X. COM.TW		300	<u>103</u>	pF
Power supp	bly with the second second	WWWWWWWWWWWWWWWWWWWWWWWWW	W		00	1.00
	Operating supply current	$V_{CC} = 5.5 V$ , $f_{SCLK} = 20 MHz$	5	5.5	8.5	mA
ICC + IREF	Operating supply current	$V_{CC} = 3 V$ , $f_{SCLK} = 10 MHz$		2.7	74	IIIA
IPD	Supply current in powerdown mode	Vcc		N T	10	μA
	Power dissipation	$V_{CC} = 5 V$		25		mW
	Power dissipation	$V_{CC} = 3 V$	×N.	8	111.	mW

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#### electrical characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V, V<sub>REF</sub> = 5 V, f<sub>SCLK</sub> = 20 MHz (unless otherwise noted) (continued)

#### ac specifications

1.1	PARAMETER	TEST CONDITIONS	MIN	TYP	Μ
	Signal-to-noise ratio + distortion	f(input) = 200 kHz	54	58	
THD	Total harmonic distortion	f <sub>(input)</sub> = 200 kHz	56	60	
·OV·	Effective number of bits	f(input) = 200 kHz	8.7	9.35	
-N	Spurious-free dynamic range	f <sub>(input)</sub> = 200 kHz	57	62	
Analog	J Input	IN N. MILLON.	V.L.A.		
BW	Full-power bandwidth	Source impedance = $1 \text{ k}\Omega$	VT N.	12	
BW	Small-signal bandwidth	Source impedance = 1 k $\Omega$	144	20	

# .\_\_\_\_ timing specifications

07.	PARAMETER	TEST CONDITIONS	MIN	ΤΥΡ ΜΑΧ	UN
t <sub>c</sub>	SCLK period	$V_{CC} = 4.5 V - 5.5 V$	50	NT.N	ns
t <sub>C</sub>	SCLK period	$V_{CC} = 2.7 V - 3.3 V$	100	WT	ns
t <sub>rs</sub>	Reset and sampling period	TW WWW.D	ov.co	6	SLC cycle
t <sub>c</sub>	Conversion period	N.W. WWW.	1001.0	10	SLC cycle
t <sub>su1</sub>	FS setup time to SCLK falling edge in DSP mode	M.T.W.	10	COMIT	ns
<sup>t</sup> h1	FS hold time to SCLK falling edge in DSP mode	MA WILL	4	TV	ns
t <sub>su2</sub>	FS setup time to CS falling edge in DSP mode	WW Wn	6	V.CO.	ns ns
<sup>t</sup> h2	FS hold time to CS falling edge in DSP mode	CCM-1	9	CONT.	ns
<sup>t</sup> d1	Output delay after SCLK rising edge in DSP mode	M.I.	W.10	15 25	ns
<sup>t</sup> d(L)1	FS falling edge to next SCLK falling edge in DSP mode	NTW W	6	00Y.	ns
<sup>t</sup> d(L)2	SCLK rising edge after $\overline{CS}$ falling edge in $\mu C$ mode	V WT TO	4	INY.COM	ns
t <sub>d2</sub>	Output delay after SCLK rising edge in $\mu$ C mode	CONT	WW.	15 25	ns

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#### definitions of specifications and terminology

#### integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

#### differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than  $\pm$ 1 LSB ensures no missing codes.

#### zero offset

The first code transition ideally occurs at an analog value 1/2 LSB above V<sub>REF</sub>-. The zero offset error is defined as the error between the ideal first transition point and the actual first transition. This error effectively shifts left or right an ADC transfer function

#### gain error

The first code transition occurs at an analog value 1/2 LSB above negative full scale. The last transition occurs at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

#### signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

#### effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

N = (SINAD - 1.76)/6.02

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

#### total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

#### spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the largest peak spurious signal.



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### APPLICATION INFORMATION

The TLV1572 is a 600-ns, 10-bit analog-to-digital converter with the throughput up to 1.25 MSPS at 5 V and up to 625 KSPS at 3 V respectively. To run at its fastest conversion rate, it must be clocked at 20 MHz at 5 V or 10 MHz at 3 V. The TLV1572 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. Its serial interface is designed to be fully compatible with Serial Peripheral Interface (SPI) and TMS320 DSP serial ports. It requires no hardware to interface between the TLV1572 and the microcontrollers (uCs) with the SPI serial port or the TMS320 DSPs. However, speed is limited by the SCLK rate of the  $\mu$ C or the DSP.

The TLV1572 interfaces to the DSPs over four lines:  $\overline{CS}$ , SCLK, DO, and FS, and interfaces to  $\mu Cs$  over three lines:  $\overline{CS}$ , SCLK, and DO. The FS input must be pulled high in  $\mu C$  mode. The chip is in 3-state and powerdown mode when CS is high. After CS falls, the TLV1572 checks the FS input at the CS falling edge to determine the operation mode. If FS is low, DSP mode is set, else µC mode is set.

#### interfacing TLV1572 to TMS320 DSPs

The TLV1572 is compatible with Texas Instruments TMS320 DSP serial ports. Figures 3(a) and 3(b) show the pin connections to interface the TLV1572 to the TMS320 DSPs.



a) DSP Serial Port Operating in Burst Mode

b) FS Externally Generated



Figure 4. Typical Timing Diagram for DSP Application

In the DSP mode, the FS input must be low when the  $\overline{CS}$  goes low. There is a hold time before the FS input can ao high after the CS falling edge to ensure proper mode latching. With CS going low, DO comes out of 3-state but the device is still in powerdown until FS (frame sync signal from DSP) goes high.

The TLV1572 checks FS at the falling edges of SCLK. Once FS is detected high, the sampling of input is started. As soon as FS goes low, the device starts shifting the data out on the DO line. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by DSP on the falling edges. Figure 4 shows the DSP mode timing diagram.



#### **APPLICATION INFORMATION**

#### interfacing TLV1572 to TMS320 DSPs (continued)

The TLV1572 goes into auto-powerdown after the LSB is shifted out. The next FS pulls it out of auto-powerdown as shown in Figure 5. If FS comes on the 16th bit, the next conversion cycle starts from the next rising edge of SCLK allowing back to back conversions as shown in Figure 6. An FS high in the middle of a conversion cycle resets the device and starts a new conversion cycle. Therefore variable-bit transfer is supported if FS appears earlier.

CS can be pulled high asynchronously to put the device into 3-state and powerdown. CS can also be pulled low asynchronously to start checking for FS on the falling edges of the clock.





#### key points

- When CS goes low, if FS is low, it is in DSP mode. FS is sampled twice by a CS falling edge and again by an internally delayed CS falling edge. Even if a glitch appears and one latch latches 1 and another latches 0, the device goes into DSP mode (μC mode requires both latches to latch 1). There is a hold time before FS can go high again after the CS falling edge to ensure proper mode latching as detailed above. With CS going low, DO is in 3-state and the device is in powerdown until a FS rising edge.
- 2. The TLV1572 checks for FS at every falling edge of SCLK. If FS is detected high, the device goes into reset. When FS goes low, the TLV1572 waits for the DSP to latch the first 0 bit.
- Sampling occurs from first falling edge of SCLK after FS going low until the rising edge when the 6th 0 bit is sent out. Thereafter decisions are taken on the rising edges and data is sent out on the rising edges (1 bit delayed). The DSP samples on the falling edge of SCLK. Data is padded with 6 leading zeros.



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### **APPLICATION INFORMATION**

#### key points (continued)

- 4. Note that the device goes into autopower down on the 17th falling edge of SCLK (just after the LSB). The FS rising edge pulls it out of autopower down. If FS comes on the 16th bit, the next conversion cycle starts from the next rising edge allowing back to back conversions. An FS in the middle of a conversion cycle starts a new conversion cycle. Thus variable-bit transfer is supported if FS appears earlier.
- 5. DO goes into 3-state on the 17th rising edge and comes out on a FS rising edge.
- 6. CS can be pulled high asynchronously to put the device into 3-state and powerdown. CS may also be pulled low asynchronously to start checking for FS on the falling edges of the clock.

For applications where the analog input must be sampled at a precise instant in time, data conversion can be initiated by an external conversion start pulse which is completely asynchronous to the SCLK as shown in Figure 4. When a conversion start pulse is received, the pulse is used as a frame sync (FS) signal to initiate the data conversion and transfer. The corresponding timing diagram is shown in Figure 6.

#### interfacing TLV1572 to SPI/QSPI compatible microcontrollers (µCs)

The TLV1572 is compatible with SPI and QSPI serial interface standards (Note: the TLV1572 supports the following SPI clock options: clock\_polarity= 0, i.e. SCLK idles low, and clock\_phase = 1). Figure 7 shows the pin connections to interface the TLV1572 to SPI/QSPI compatible microcontrollers.



Figure 8. Typical Timing Diagram for  $\mu$ C Application

To use the TLV1572 in a non-DSP application, the FS input must be pulled high as shown in Figure 8.

A total of 16 clocks are normally supplied for each conversion. If the  $\mu$ C cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and next 8 bits with another 8 clocks.  $\overline{CS}$  must be kept low throughout the conversion. The delay between these two 8-clock periods must not be longer than 100  $\mu$ s.



### **APPLICATION INFORMATION**

#### interfacing TLV1572 to SPI/QSPI compatible microcontrollers(µCs) (continued)

Unlike the DSP mode in which the conversion is initiated by the FS input signal from the DSP, the conversion is initiated by the incoming SCLK after  $\overline{CS}$  falls. Sampling of the input is started on the first rising edge of SCLK after  $\overline{CS}$  goes low. After six null bits, the A/D conversion data becomes available on SCLK rising edges and is latched by the  $\mu$ C on the falling edges.  $\overline{CS}$  can be pulled high during the conversion before the LSB is shifted out to use the device as a lower resolution ADC. Figure 9 shows the  $\mu$ C mode timing diagram.

The device goes into autopower down after the LSB is shifted out and is brought out of powerdown by the next clock rising edge as shown in Figure 9.





#### key points

- 1. When  $\overline{CS}$  goes low, if FS is high, it is in  $\mu C$  ({Q}SPI) mode. Thus, FS is tied to V<sub>DD</sub>. FS is latched twice, on the falling edge of  $\overline{CS}$  and again on an internally delayed falling edge of  $\overline{CS}$ . Only if both latches latch 1, then  $\mu C$  mode is set else DSP mode is set. Only polarity = 0 is supported, i.e. SCLK idles low. Only clock\_phase = 1 is supported as shown in the timing diagrams.
- 2. For each conversion 16 clocks have to be supplied. If the  $\mu$ C cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and the next 8 bits with another 8 clocks keeping  $\overline{CS}$  low throughout the conversion. The delay between these two 8-clock periods must not be longer than 100  $\mu$ s.
- 3. Sampling starts on the first rising edge of SCLK and ends on the edge when the 6th 0 bit is sent out. Decisions are made on the rising edge and data is output on the same edge but a bit delayed to avoid noise.
- 4. The device goes into autopower down on the falling edge of the 16th clock and is brought out of powerdown by next first (17th) clock rising edge.
- If the (Q)SPI wants less than a 16-bit transfer, CS must go high after each transfer. The falling edge of CS resets the TLV1572 for the next conversion. Thus a 14-bit transfer is possible when using the device as an 8-bit A/D.
- 6. CS going high puts the device in 3-state and complete powerdown. CS going low sets the mode and pulls DO out of 3-state.



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#### **MECHANICAL INFORMATION**

#### D (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **14 PIN SHOWN**



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012



TEXAS

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLV1572CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572CDG4	ACTIVE	SOIC	TVD	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572ID	ACTIVE	SOIC	O D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572IDG4	ACTIVE	SOIC	CO D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1572IDRG4	ACTIVE	SOIC	Boy	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### TAPE AND REEL INFORMATION

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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1572CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1572IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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TEXAS INSTRUMENTS

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LV1572CDR	SOIC	D 10	8	2500	346.0	346.0	29.0
TLV1572IDR	SOIC	D	8	2500	346.0	346.0	29.0

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