

March 1997

CMOS Octal Inverting Bus Transceiver

Features

- Full Eight Bit Bi-Directional Bus Interface
- Industry Standard 8287 Compatible Pinout
- High Drive Capability
 - B Side I_{OL} 20mA
 - A Side I_{OL} 12mA
- Three-State Inverting Outputs
- Propagation Delay 35ns Max.
- Gated Inputs
 - Reduce Operating Power
 - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation ICCSB = 10μA
- Operating Temperature Range
 - C82C87H 0°C to +70°C
 - I82C87H -40°C to +85°C
 - M82C87H -55°C to +125°C

Description

The Intersil 82C87H is a high performance CMOS Octal Transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C87H provides a full eight-bit bi-directional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable (\overline{OE}) permits simple interface to the 80C86, 80C88 and other microprocessors. The 82C87H has gated inputs, eliminating the need for pull-up/pull-down resistors and reducing overall system operating power dissipation. The 82C87H provides inverted data at the outputs.

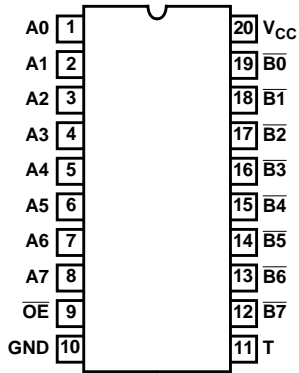
Ordering Information

| PART NUMBERS | | PACK-AGE | TEMP. RANGE | PKG. NO. |
|----------------|----------|--------------|-----------------|----------|
| 5MHz | 8MHz | | | |
| CP82C87H-5 | CP82C87H | 20 Ld PDIP | 0°C to +70°C | E20.3 |
| IP82C87H-5 | IP82C87H | | -40°C to +85°C | E20.3 |
| CS82C87H-5 | CS82C87H | 20 Ld PLCC | 0°C to +70°C | N20.35 |
| IS82C87H-5 | IS82C87H | | -40°C to +85°C | N20.35 |
| CD82C87H-5 | CD82C87H | 20 Ld CERDIP | 0°C to +70°C | F20.3 |
| ID82C87H-5 | ID82C87H | | -40°C to +85°C | F20.3 |
| MD82C87H-5/B | - | | -55°C to +125°C | F20.3 |
| 5962-8757702RA | - | SMD # | | F20.3 |
| MR82C87H-5/B | - | 20 Pad CLCC | -55°C to +125°C | J20.A |
| 5962-87577022A | - | SMD # | | J20.A |

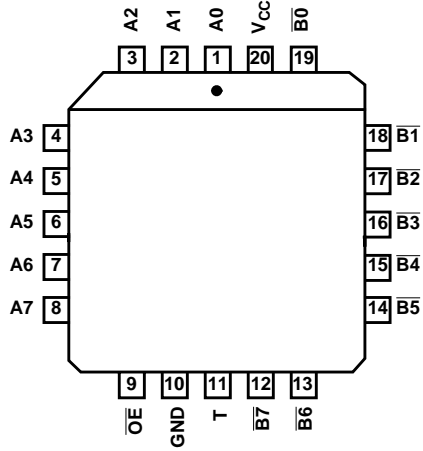
82C87H

Pinouts

82C87H (PDIP, CERDIP)
TOP VIEW



82C87H (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

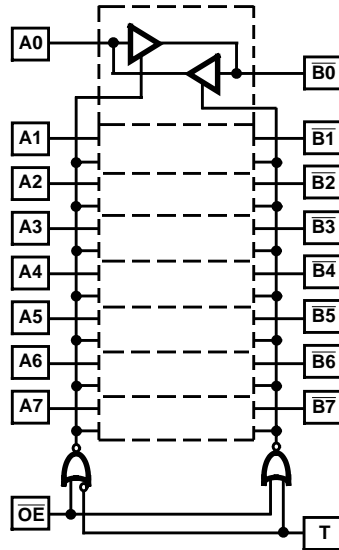
| T | OE | A | B |
|---|----|------|------|
| X | H | Hi-Z | Hi-Z |
| H | L | I | O |
| L | L | O | I |

H = Logic One
 L = Logic Zero
 I = Input Mode
 O = Output Mode
 X = Don't Care
 Hi-Z = High Impedance

PIN NAMES

| PIN | DESCRIPTION |
|--------------------------------|--------------------------|
| A ₀ -A ₇ | Local Bus Data I/O Pins |
| B ₀ -B ₇ | System Bus Data I/O Pins |
| T | Transmit Control Input |
| OE | Active Low Output Enable |

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Intersil 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled (\overline{OE} = logic one for the 82C87H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-Channel and lower N-Channel (See Figures 1 and 2). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of $10\mu A$ during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C86H/87H data sheet is determined by:

$$I = C_L (dv/dt) \quad (\text{EQ. 4})$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(V_{CC} \times 80\%)}{tR/tF} \quad (\text{EQ. 5})$$

where $tR = 20\text{ns}$, $V_{CC} = 5.0\text{V}$, $C_L = 300\text{pF}$ on each eight outputs.

$$I = (80 \times 300 \times 10^{-12}) \times (5.0\text{V} \times 0.8) / (20 \times 10^{-9}) \quad (\text{EQ. 6}) \\ = 480\text{mA}$$

This current spike may cause a large negative voltage spike on V_{CC} which could cause improper operation of the device. To filter out this noise, it is recommended that a $0.1\mu\text{F}$ ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

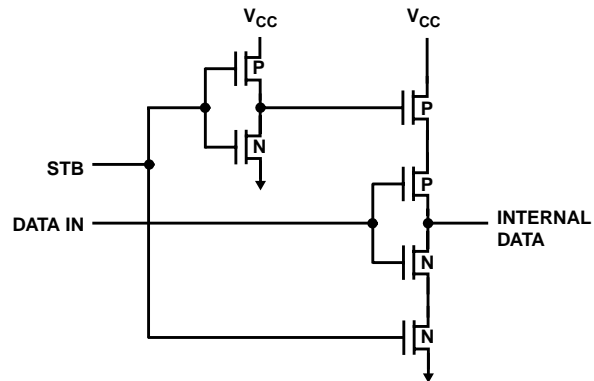


FIGURE 3. 82C82/83H

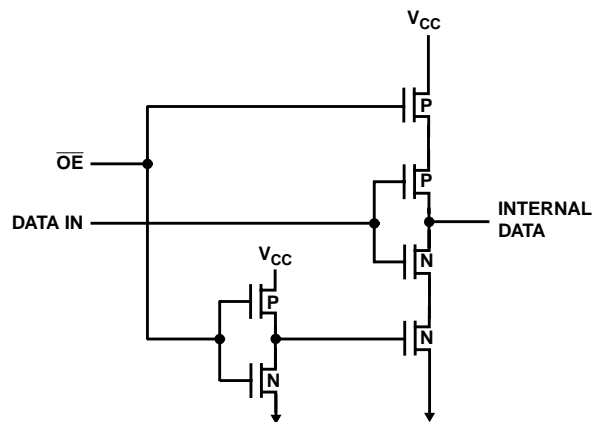


FIGURE 4. 82C86H/87H GATED INPUTS

82C87H

Absolute Maximum Ratings

Supply Voltage +8.0V
 Input, Output or I/O Voltage GND -0.5V to $V_{CC} + 0.5V$
 ESD Classification Class 1

Operating Conditions

Operating Voltage Range +4.5V to +5.5V
 Operating Temperature Range
 C82C87H 0°C to +70°C
 I82C87H -40°C to +85°C
 M82C87H -55°C to +125°C

Thermal Information

| | | |
|---|-----------------------------------|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| CERDIP Package | 70 | 16 |
| CLCC Package | 80 | 20 |
| PDIP Package | 75 | N/A |
| PLCC Package | 75 | N/A |
| Storage Temperature Range | -65°C to +150°C | |
| Maximum Junction Temperature Hermetic Package | +175°C | |
| Maximum Junction Temperature Plastic Package | +150°C | |
| Maximum Lead Temperature (Soldering 10s) | +300°C (PLCC - Lead Tips Only) | |

Die Characteristics

Gate Count 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications $V_{CC} = 5.0V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$ (C82C87H);
 $T_A = -40^\circ C$ to $+85^\circ C$ (I82C87H);
 $T_A = -55^\circ C$ to $+125^\circ C$ (M82C87H)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|----------|--------------------------------|----------------|------|---------|---|
| V_{IH} | Logical One | 2.0 | - | V | C82C87H, I82C87H |
| | Input Voltage | 2.2 | - | V | M82C87H (Note 1) |
| V_{IL} | Logical Zero Input Voltage | - | 0.8 | V | |
| V_{OH} | Logical One Output Voltage | | | | |
| | B Outputs | 3.0 | - | V | $I_{OH} = -8mA$ |
| | A Outputs | 3.0 | - | V | $I_{OH} = -4mA$ |
| | A or B Outputs | $V_{CC} - 0.4$ | - | V | $I_{OH} = -100\mu A$ |
| V_{OL} | Logical Zero Output Voltage | | | | |
| | B Outputs | - | 0.45 | V | $I_{OL} = 20mA$ |
| | A Outputs | - | 0.45 | V | $I_{OL} = 12mA$ |
| I_I | Input Leakage Current | -10.0 | 10.0 | μA | $V_{IN} = GND$ or V_{CC} DIP Pins 9, 11 |
| I_O | Output Leakage Current | -10.0 | 10.0 | μA | $V_O = GND$ or V_{CC} , $\overline{OE} \geq V_{CC} - 0.5V$ DIP Pins 1 - 8, 12 - 19 |
| ICCSB | Standby Power Supply Current | - | 10 | μA | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$, Outputs Open |
| ICCOP | Operating Power Supply Current | - | 1 | mA/MHz | $T_A = +25^\circ C$, Typical (See Note 2) |

NOTES:

- V_{IH} is measured by applying a pulse of magnitude = $V_{IH(MIN)}$ to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (T , \overline{OE}) are tested separately with all device data input pins at $V_{CC} - 0.4$.
- Typical ICCOP = 1mA/MHz of read/ cycle time. (Example: 1.0 μs read/write cycle time = 1mA).

Capacitance $T_A = +25^\circ C$

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|--------|-------------------|---------|-------|--|
| CIN | Input Capacitance | | | |
| | B Inputs | 18 | pF | Freq = 1MHz, all measurements are referenced to device GND |
| | A Inputs | 14 | pF | |

82C87H

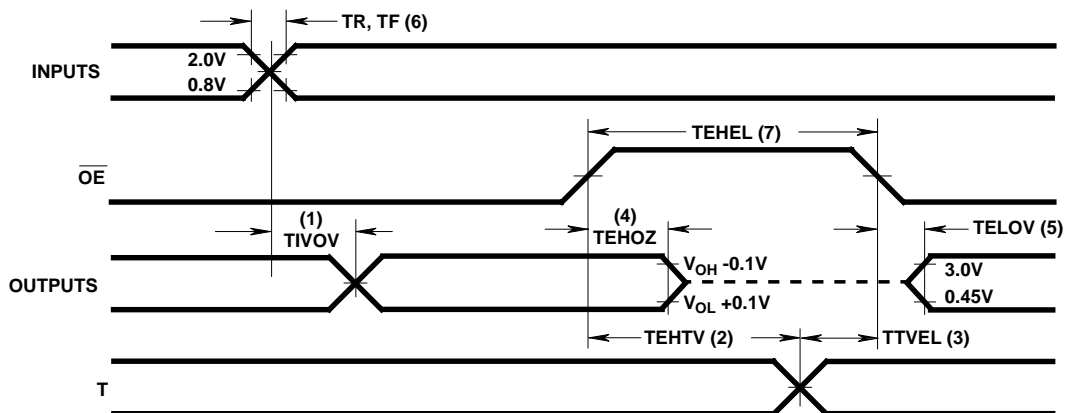
AC Electrical Specifications $V_{CC} = 5.0V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$ (C82C87H);
 Freq = 1MHz $T_A = -40^\circ C$ to $+85^\circ C$ (I82C87H);
 $T_A = -55^\circ C$ to $+125^\circ C$ (M82C87H)

| SYMBOL | PARAMETER | MIN | NOTE 4 | | UNITS | TEST CONDITIONS |
|------------|---------------------------------|-----|---------------|-----------------|-------|-----------------|
| | | | 82C87H MAX | 82C87H-5 MAX | | |
| (1) TIVOV | Input to Output Delay | | | | | Notes 1, 2 |
| | Inverting | 5 | 30 | 35 | ns | |
| | Non-Inverting | 5 | 32 | 35 | ns | |
| (2) TEHTV | Transmit/Receive Hold Time | 5 | - | - | ns | Notes 1, 2 |
| (3) TTVEL | Transmit/Receive Setup Time | 10 | - | - | ns | Notes 1, 2 |
| (4) TEHOZ | Output Disable Time | 5 | 30 | 35 | ns | Notes 1, 2 |
| (5) TELOV | Output Enable Time | 10 | 50 | 65 | ns | Notes 1, 2 |
| (6) TR, TF | Input Rise/Fall Times | - | 20 | 20 | ns | Notes 1, 2 |
| (7) TEHEL | Minimum Output Enable High Time | | | | | Note 3 |
| | 82C87H | 30 | - | - | ns | |
| | 82C87H-5 | 35 | - | - | ns | |

NOTES:

- All AC parameters tested as per test circuits and definitions in timing waveforms and test load circuits. Input rise and fall times are driven at 1ns/V.
- Input test signals must switch between $V_{IL} - 0.4V$ and $V_{IH} + 0.4V$.
- A system limitation only when changing direction. Not a measured parameter.
- 82C87H is available in commercial and industrial temperature ranges only. 82C87H-5 is available in commercial, industrial and military temperature ranges.

Timing Waveform

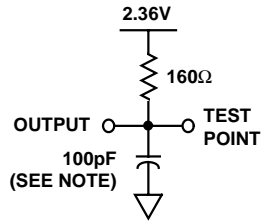


82C87H

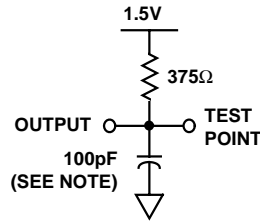
Test Load Circuits

A SIDE OUTPUTS

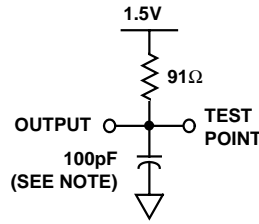
TIVOV LOAD CIRCUIT



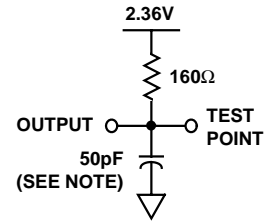
TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT



TELOV OUTPUT LOW ENABLE LOAD CIRCUIT

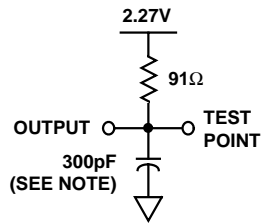


TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT

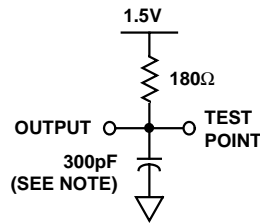


B SIDE OUTPUTS

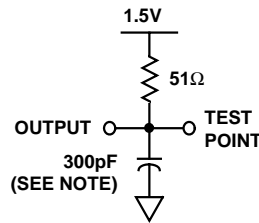
TIVOV LOAD CIRCUIT



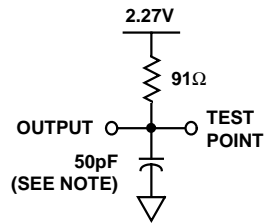
TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT



TELOV OUTPUT LOW ENABLE LOAD CIRCUIT



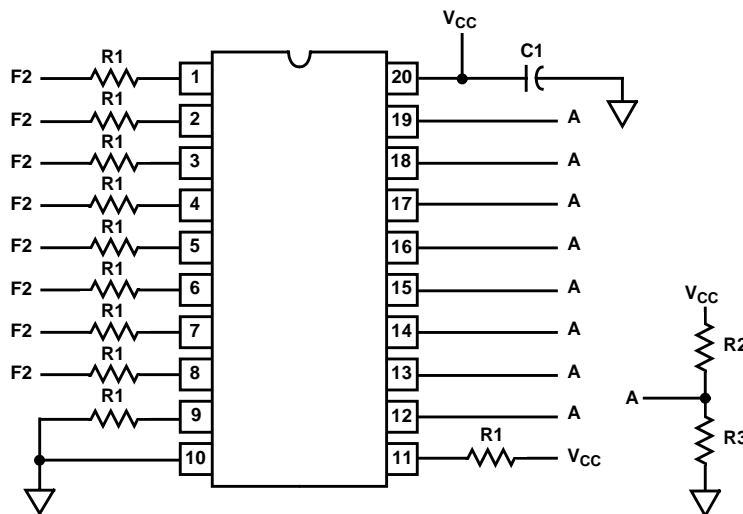
TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT



NOTE: Includes jig and stray capacitance.

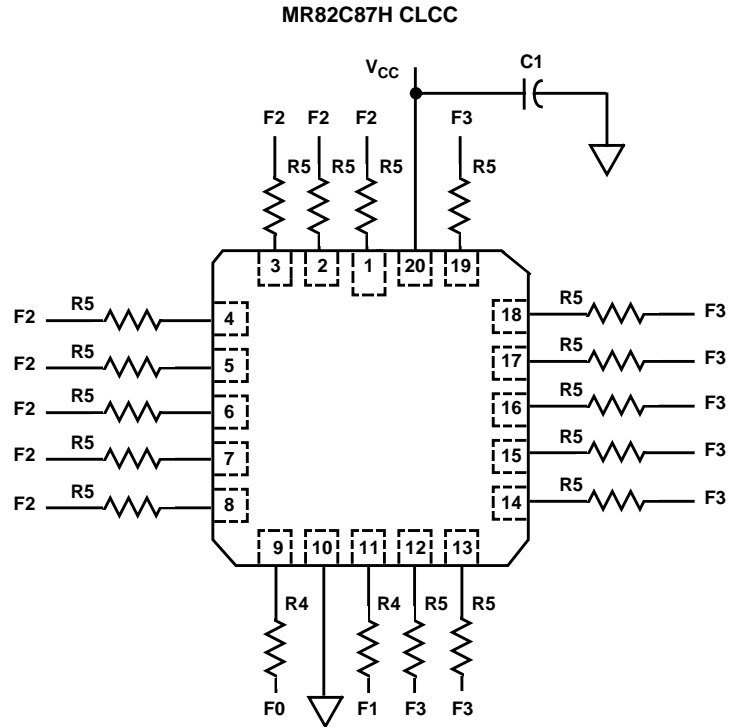
Burn-In Circuits

MD82C87H CERDIP



82C87H

Burn-In Circuits (Continued)



NOTES:

1. $V_{CC} = 5.5V \pm 0.5V$, GND = 0V
2. $V_{IH} = 4.5V \pm 10\%$
3. $V_{IL} = -0.2V$ to 0.4V
4. $R1 = 47k\Omega \pm 5\%$
5. $R2 = 2.4k\Omega \pm 5\%$
6. $R3 = 1.5k\Omega \pm 5\%$
7. $R4 = 1k\Omega \pm 5\%$
8. $R5 = 5k\Omega \pm 5\%$
9. $C1 = 0.01\mu F$ minimum
10. $F0 = 100kHz \pm 10\%$
11. $F1 = F0/2$, $F2 = F1/2$, $F3 = F2/2$

82C87H

Die Characteristics

DIE DIMENSIONS:

138.6 x 155.5 x 19 ± 1mils

METALLIZATION:

Type: Si - Al

Thickness: 11kÅ ± 1kÅ

GLASSIVATION:

Type: SiO₂

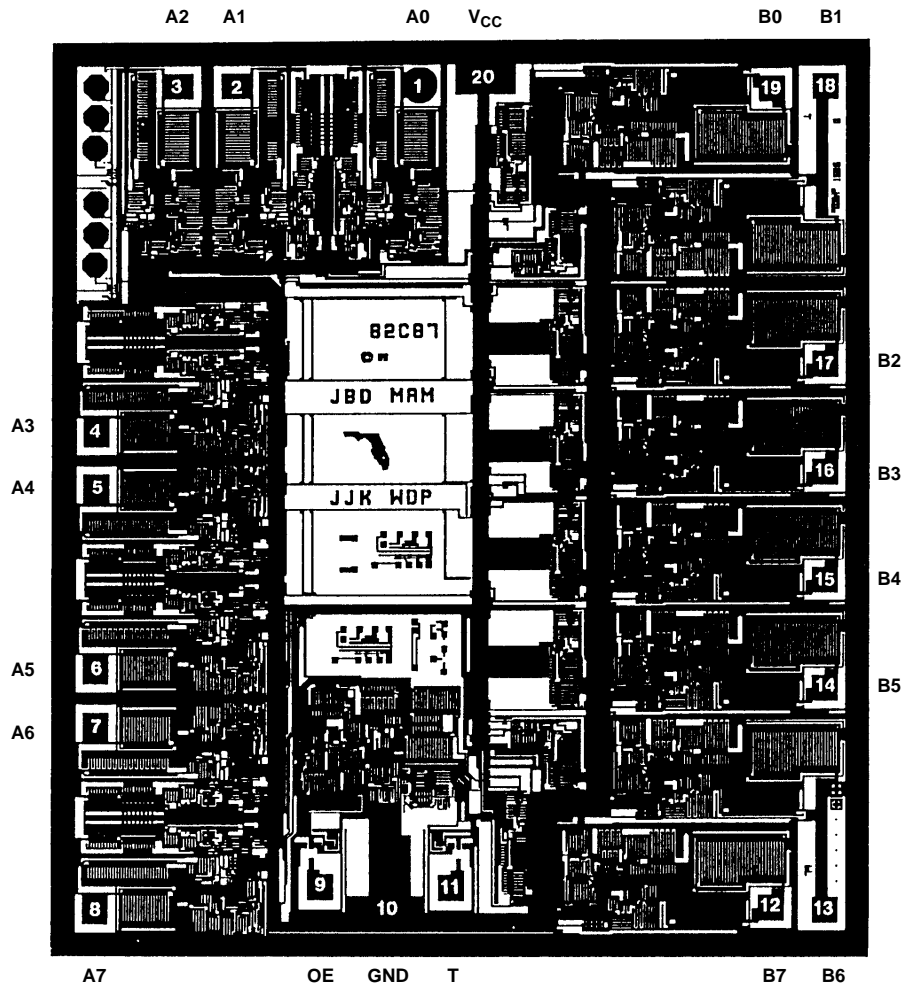
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:

1.47 x 10⁵ A/cm²

Metallization Mask Layout

82C87H



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>