iC-LF 1401

128x1 LINEAR IMAGE SENSOR

FEATURES

- 128 active pixels with 56µm x 200µm photodiodes in a 63.5µm pitch (400DPI)
- Integrating L-V conversion followed by a sample-and-hold circuit
- High sensitivity and uniformity over wavelength
- High clock rates of up to 5MHz
- Shutter function enables flexible integration times
- Push-Pull output amplifier
- 5V single supply operation
- Can run off external bias to reduce power consumption
- Functions equivalent to and pin-to-pin compatible with TSL1401 (in an 8-pin oLGA LF2C package)

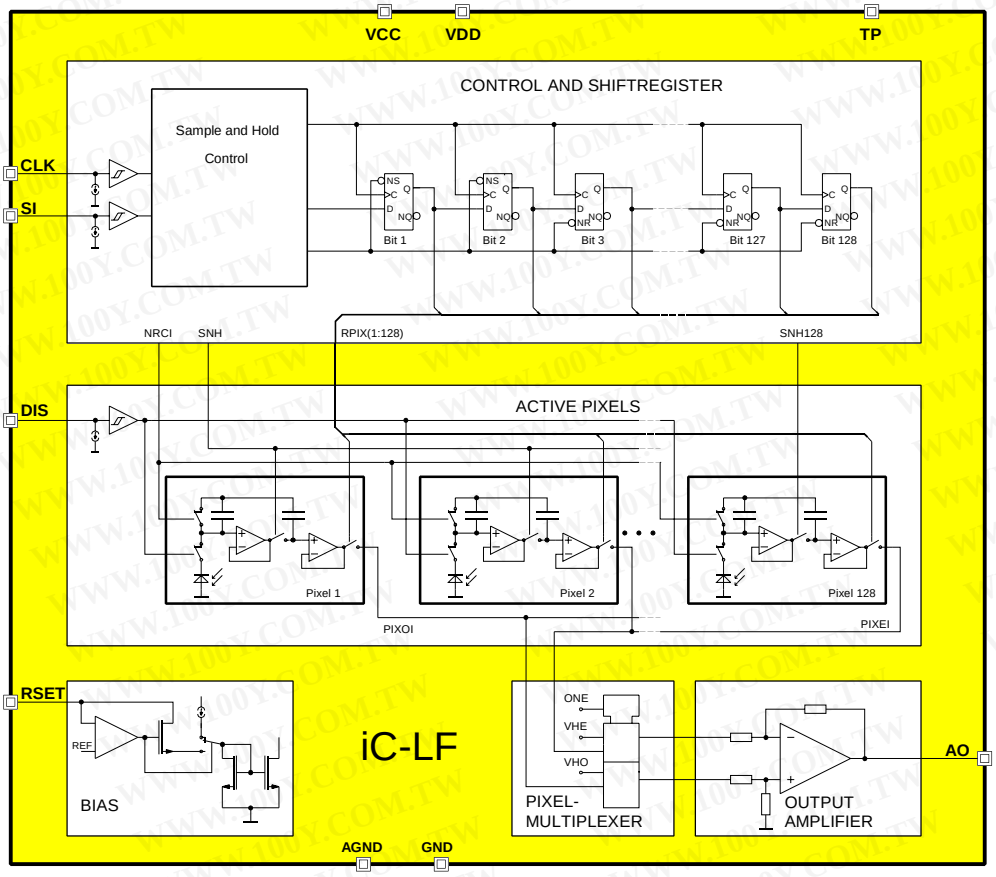
APPLICATIONS

- Optical row sensors
- CCD substitute

PACKAGES

chip size 8.5mm x 1.6mm

BLOCK DIAGRAM



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DESCRIPTION

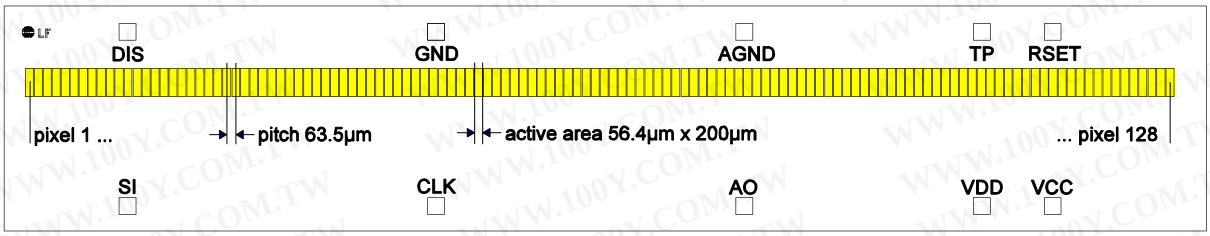
iC-LF is an integrating light-to-voltage converter with a row of 128 pixels pitched at 63.5µm (center-to-center distance). Each pixel consists of a 56.4µm x 200µm photodiode, an integration capacitor and a sample-and-hold circuit.

The integrated control logic makes operation very simple, with only a start and clock signal necessary. A third control input enables the integration period to be prematurely terminated at any time.

When the start signal is given hold mode is activated for all pixels simultaneously with the next rising clock edge; starting with pixel 1 the hold voltages are switched in sequence to the push-pull output amplifier. The second clock pulse deletes all integration capacitors and the integration period starts again in the background during the output phase. A run is complete after 128 clock pulses.

iC-LF is suitable for high clock rates of up to 5MHz. If this is not required the supply current can be reduced via the external bias setting.

CHIP LAYOUT



PAD DESCRIPTION

Name	Function
SI	Start Integration Input
CLK	Clock Input
AO	Analog Output (1mA push-pull)
VDD	+5V Supply Voltage (digital)
VCC	+5V Supply Voltage (analog)
RSET	Bias Current Adjust (by resistor from VCC; when linked to GND the internal bias setting is activated)
TP	Test Output
AGND	Analog Ground
GND	Digital Ground
DIS	Disable Integration Input (use is optional; input can be switched to GND or left open for compatibility with TSL1401)

External connections linking GND to AGND and VDD to VCC are required.

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDD	Digital Supply Voltage			-0.3	6	V
G002	VCC	Analog Supply Voltage			-0.3	6	V
G003	V()	Voltage at SI, CLK, DIS, RSET, TP, AO			-0.3	VCC+0.3	V
G004	I()	Current in RSET, TP, AO			-10	10	mA
E001	Vd()	ESD Susceptibility at all pins	MIL-STD-883, Method 3015, HBM 100pF/ 1.5kΩ			2	kV
TG1	Tj	Operating Junction Temperature			-40	125	°C
TG2	Tj	Storage Temperature Range	see package specification				

THERMAL DATA

Operating Conditions: VCC= VDD= 5V ±10%

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range (extended range on request)	see package specification					

OPTICAL CHARACTERISTICS: Diagrams

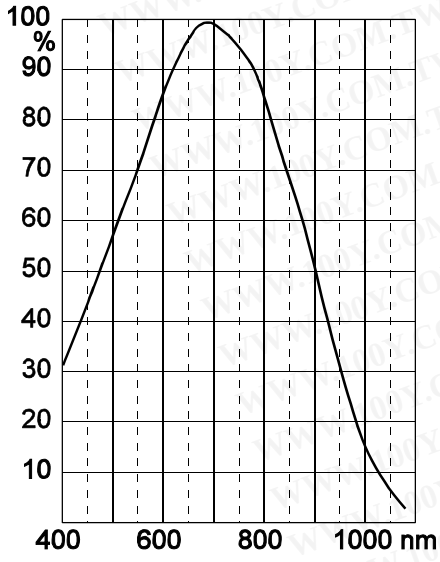


Fig. 1: relative spectral sensitivity

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VDD= 5V ±10%, RSET= GND, Tj= -25..85°C unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VDD	Digital Supply Voltage Range				4.5		5.5	V
002	VCC	Analog Supply Voltage Range				4.5		5.5	V
003	I(VDD)	Supply Current in VDD	f(CLK)= 1MHz				200	300	µA
004	I(VCC)	Supply Current in VCC					8	13	mA
005	Vc()hi	Clamp Voltage hi at SI, CLK, DIS, TP, RSET	Vc()hi= V() - V(VCC); I()= 1mA			0.3		1.8	V
006	Vc()lo	Clamp Voltage lo at SI, CLK, DIS, TP, RSET	Vc()hi= V() - V(AGND); I()= -1mA			-1.5		-0.3	V
007	Vc()hi	Clamp Voltage hi at AO	Vc()hi= V(AO) - V(VCC); I(AO)= 1mA			0.3		1.5	V
008	Vc()lo	Clamp Voltage lo at AO, VCC, VDD, GND	Vc()lo= V() - V(AGND); I()= -1mA			-1.5		-0.3	V
Photodiode Array									
201	A()	Radiant Sensitive Area	200µm x 56.40µm per Pixel				0.01128		mm^2
202	S(λ)max	Spectral Sensitivity	λ= 680nm				0.5		A/W
203	λar	Spectral Application Range	S(λar)= 0.25xS(λ)max			400		1000	nm
Analog Output AO									
301	Vs()lo	Saturation Voltage lo	I()= 1mA					0.5	V
302	Vs()hi	Saturation Voltage hi	Vs()hi= VCC - V(), I()= -1mA					1	V
303	K	Sensitivity	λ= 680nm, package OLGA LF2C				2.88		V/pWs
304	V0()	Offset Voltage	integration time 1ms, no illumination				400	800	mV
305	ΔV0()	Offset Voltage Deviation during integration mode	ΔV0()= V(AO)t1-V(AO)t2, Δt= t2 -t1= 1ms			-250		50	mV
306	ΔV()	Signal Deviation during hold mode	ΔV0()=V(AO)t1-V(AO)t2, Δt= t2 -t1= 1ms			-150		150	mV
307	tp(CLK-AO)	Settle Time	Cl(AO)= 10pF, CLK lo-> hi until V(AO)= 0.98xV(VCC)					200	ns
Power-On-Reset									
801	VCCon	Power-On Release by VCC						4.4	V
802	VCCoff	Power-Down Reset by VCC				1			V
803	VCChys	Hysteresis	VCChys= VCCon - VCCoff			0.4	1	2	V
Bias Current Adjust RSET									
901	Ibias()	Permissible External Bias Current				20		100	µA
902	Vref	Reference Voltage	I(RSET)= Ibias			2.5	3	3.5	V
Input Interface SI, CLK, DIS									
B01	Vt()hi	Threshold Voltage hi				1.4		1.8	V
B02	Vt()lo	Threshold Voltage lo				0.9		1.2	V
B03	Vt()hys	Hysteresis	Vt()hys= Vt()hi - Vt()lo			300		800	mV
B04	I()	Pull-Down Current				10	30	50	µA
B05	fclk	Permissible Clock Frequency						5	MHz

OPERATING REQUIREMENTS: Logic

Operating Conditions: VCC= VDD= 5V ±10%, Tj= -25..85°C
input levels lo= 0..0.45V, hi= 2.4V..VCC, see Fig. 2 for reference levels

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I1	tset	Setup Time: SI stable before CLK lo→hi		2	50		ns
I2	thold	Hold Time: SI stable after CLK lo→hi		2	50		ns

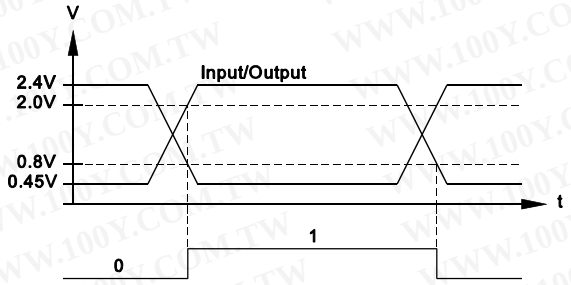


Fig. 2: reference levels

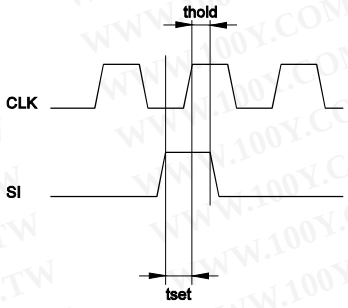


Fig. 3: timing diagram

DESCRIPTION OF FUNCTIONS

Normal operation

Following an internal power-on reset the integration and hold capacitances are deleted and the sample-and-hold circuit is set to sample mode. A high at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle.

In this process the hold capacitances of pixels 1 to 127 are switched to hold mode immediately (SNH= 1), with pixel 128 (SNH128= 1) following suit one clock pulse later. This special procedure allows all pixels to be read out with just 128 clock pulses. The integration capacitances are deleted by a pulse-long reset signal (NRCI= 0) which occurs between the 2nd and 3rd falling edge of the readout clock pulse (see Figure 4). After the 127 pixels have been read out these are again set to sample mode (SNH= 0), likewise for pixel 128 one clock pulse later (SNH128= 0).

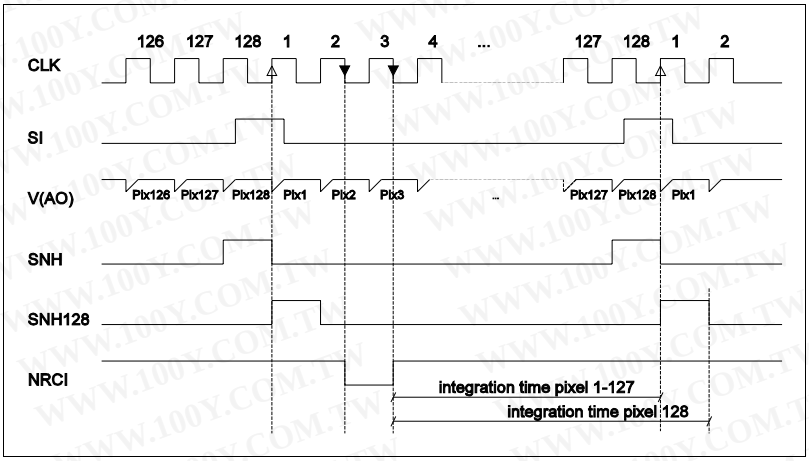


Fig. 4: readout cycle and integration sequence

If prior to the 128th clock pulse a high occurs at SI the present readout is halted and immediately reinitiated with pixel 1. In this instance the hold capacitances retain their old value i.e. hold mode prevails (SNH/SNH128= 0).

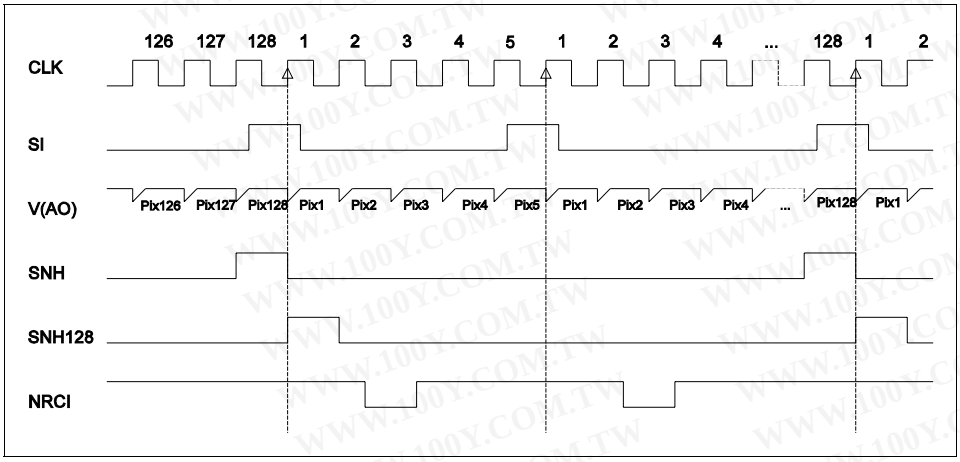


Fig. 5: restarting a readout cycle

If there are over 128 clock pulses until the next SI signal pixel 1 is output without entering hold mode; the output voltage tracks the voltage of the pixel 1 integration capacitance.

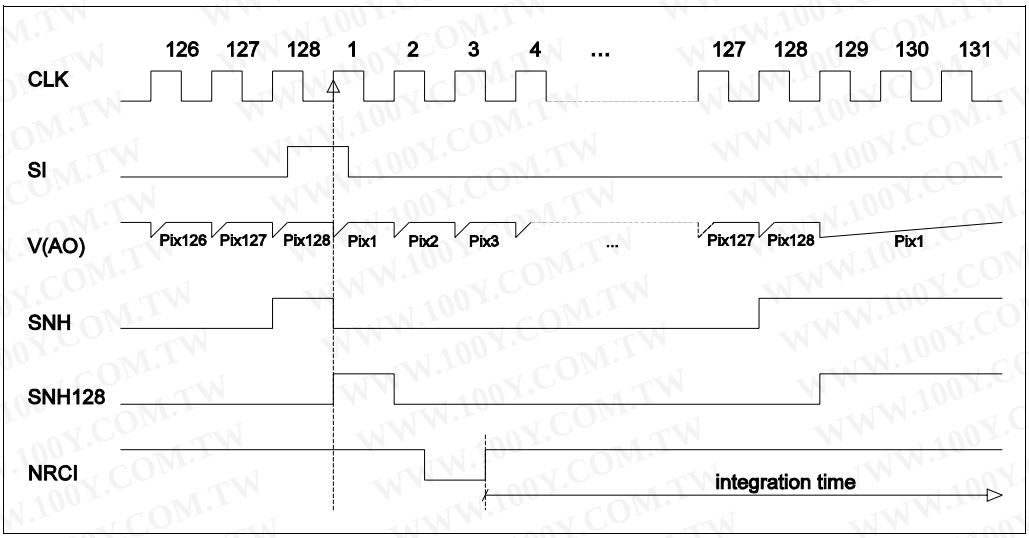


Fig. 6: clock pulse continued without giving a new integration start signal

Operation with the shutter function

Integration can be disabled at any time via pin DIS, i.e. the photodiodes are switched away from their corresponding integration capacitance when DIS is high and the current integration capacitance voltages are maintained. If this pin is open or switched to GND the pixel photocurrents are summed up by the integration capacitances until the next successive SI signal follows.

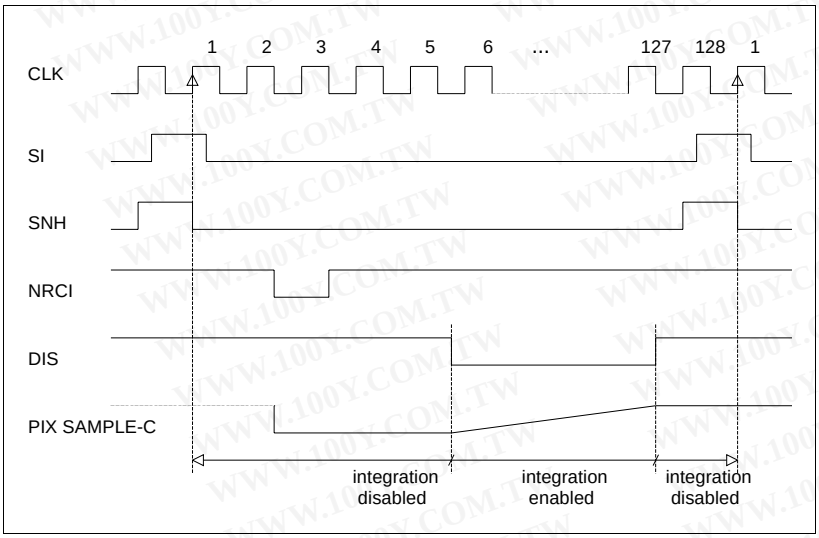


Fig. 7: defining the integration time via shutter input DIS

External bias current setting

In order to reduce the power consumption of the device an external reference current can be supplied to pin RSET what reduces the maximum readout frequency, however. To this end a resistor must be wired from VCC to RSET. If this pin is not used it should be linked to GND.

ORDERING INFORMATION

Type	Package	Order designation
iC-LF	-	iC-LF chip
	OLGA	iC-LF OLGA LF2C

For information about prices, terms of delivery, options for other case types, etc., please contact:

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