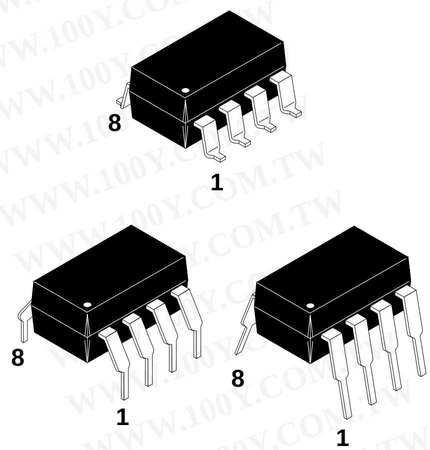
QT OPTOELECTRONICS

LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON OPTOCOUPLERS

SINGLE-CHANNEL	DUAL-CHANNEL
6N138	HCPL-2730
6N139	HCPL-2731



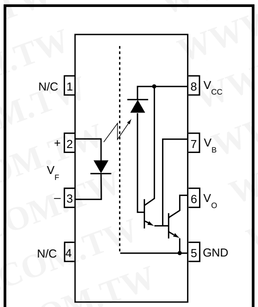
DESCRIPTION

The 6N138/9 and HCPL-2730/HCPL-2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

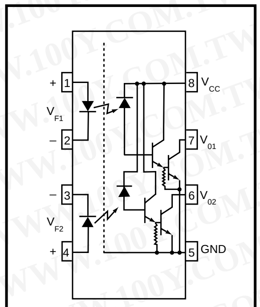
The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL-2730/HCPL2731, an integrated emitter - base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

An internal noise shield provides exceptional common mode rejection of 10 kV/µs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard 220 V.



6N138 / 6N139



HCPL-2730 / HCPL-2731

FEATURES

- Low current - 0.5 mA
- Superior CTR-2000%
- Superior CMR-10 kV/µs
- Double working voltage-480V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)
- Dual Channel - HCPL-2730 HCPL-2731

APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- µP bus isolation
- Current loop receiver

ABSOLUTE MAXIMUM RATINGS (No derating required up to 85°C)

Parameter		Symbol	Value	Units
Storage Temperature		T_{STG}	-55 to +125	°C
Operating Temperature		T_{OPR}	-40 to +85	°C
Lead Solder Temperature		T_{SOL}	260 for 10 sec	°C
EMITTER				
DC/Average Forward Input Current	Each Channel	I_F (avg)	20	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	Each Channel	I_F (pk)	40	mA
Peak Transient Input Current - (≤ 1 µs P.W., 300 pps)		I_F (trans)	1.0	A
Reverse Input Voltage	Each Channel	V_R	5	V
Input Power Dissipation	Each Channel	P_D	35	mW
DETECTOR				
Average Output Current	Each Channel	I_O (avg)	60	mA
Emitter-Base Reverse Voltage	(6N138 and 6N139)	V_{EB}	0.5	V
Supply Voltage, Output Voltage	(6N138, HCPL-2730)	V_{CC}, V_O	-0.5 to 7	V
	(6N139, HCPL-2731)		-0.5 to 18	
Output power dissipation	Each Channel	P_D	100	mW

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ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER							
Input Forward Voltage	(T_A =25°C)	V_F	All		1.30	1.7	V
	Each Channel (I_F = 1.6 mA)					1.75	
Input Reverse Breakdown Voltage	(T_A = 25°C, I_R = 10 µA) Each Channel	BV_R	All	5.0	20		V
Temperature coefficient of forward voltage	(I_F = 1.6 mA)	($\Delta V_F/\Delta T_A$)	All		-1.8		mV/°C
DETECTOR							
Logic high output current	(I_F = 0 mA, V_O = V_{CC} = 18 V) Each Channel	I_{OH}	6N139 / HCPL-2731		0.01	100	µA
	(I_F = 0 mA, V_O = V_{CC} = 7 V) Each Channel		6N138 / HCPL-2730		0.01	250	
Logic low supply	(I_F = 1.6 mA, V_O = Open) (V_{CC} = 18 V)	I_{CCL}	6N138 / 6N139		0.4	1.5	mA
	(I_{F1} = I_{F2} = 1.6 mA, V_{CC} = 18 V) (V_{O1} = V_{O2} = Open, V_{CC} = 7 V)		HCPL-2731 / HCPL-2730		1.3	3	
Logic high supply	(I_F = 0 mA, V_O = Open) (V_{CC} = 18 V)	I_{CCH}	6N138 / 6N139		0.05	10	µA
	(I_{F1} = I_{F2} = 0 mA, V_{CC} = 18 V) (V_{O1} = V_{O2} = Open, V_{CC} = 7 V)		HCPL-2731 / HCPL-2730		0.1	20	

** All typicals at T_A = 25°C

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TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
COUPLED	(I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V)	CTR	6N139	400	1100		%
	Each Channel		HCPL-2731		3500		
Current transfer ratio (Notes 1,2)	(I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V)		6N139	500	1300		%
	Each Channel		HCPL-2731		2500		
	(I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V)		6N138	300	1300		%
	Each Channel		HCPL-2730		2500		
Logic low output voltage output voltage (Note 2)	(I_F = 0.5 mA, I_O = 2 mA, V_{CC} = 4.5 V)	V_{OL}	6N139		0.08	0.4	V
	(I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V)		6N139		0.01	0.4	
	Each Channel		HCPL-2731				
	(I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V)		6N139		0.13	0.4	
	Each Channel		HCPL-2731				
	(I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V)		6N139		0.20	0.4	
	Each Channel		HCPL-2731				
	(I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V)		6N138		0.10	0.4	
	Each Channel		HCPL-2730				

** All typicals at T_A = 25°C

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SWITCHING CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified., V_{CC} = 5 V)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low (Note 2) (Fig. 22)	(R_L = 4.7 kΩ, I_F = 0.5 mA)	T_{PHL}	6N139			30	µs
	T_A = 25°C		6N139		4	25	
	(R_L = 4.7 kΩ, I_F = 0.5 mA) Each Channel		HCPL-2731			120	
	Each Channel T_A = 25°C		HCPL-2731		3	100	
	(R_L = 270 Ω, I_F = 12 mA)		6N139			2	
	T_A = 25°C		6N139		0.2	1	
	(R_L = 270 Ω, I_F = 12 mA) Each Channel		HCPL-2730			3	
	Each Channel T_A = 25°C		HCPL-2731		0.3	2	
	(R_L = 2.2 kΩ, I_F = 1.6 mA)		6N138			15	
	T_A = 25°C		6N138		1.5	10	
	(R_L = 2.2 kΩ, I_F = 1.6 mA) Each Channel		HCPL-2731			25	
	Each Channel T_A = 25°C		HCPL-2730		1	20	
Propagation delay time to logic high (Note 2) (Fig. 22)	(R_L = 4.7 kΩ, I_F = 0.5 mA)	T_{PLH}	6N139			90	µs
	Each Channel		HCPL-2731				
	(R_L = 4.7 kΩ, I_F = 0.5 mA) T_A = 25°C		6N139		12	60	
	Each Channel		HCPL-2731		22		
	(R_L = 270 Ω, I_F = 12 mA)		6N139			10	
	T_A = 25°C		6N139		1.3	7	
	(R_L = 270 Ω, I_F = 12 mA) Each Channel		HCPL-2730			15	
	T_A = 25°C		HCPL-2731		5	10	
	(R_L = 2.2 kΩ, I_F = 1.6 mA)		6N138			50	
	Each Channel		HCPL-2730/1				
	(R_L = 2.2 kΩ, I_F = 1.6 mA) T_A = 25°C		6N138		7	35	
	Each Channel		HCPL-2730/1		16		
Common mode transient immunity at logic high	(I_F = 0 mA, $\|V_{CM}\|$ = 10 V_{P-P}) T_A = 25°C, (R_L = 2.2 kΩ) (Note 3) (Fig. 23)	$\|CM_H\|$	6N138, 6N139	1,000	10,000		V/µs
	Each Channel		HCPL-2730, HCPL-2731				
Common mode transient immunity at logic low	(I_F = 1.6 mA, $\|V_{CM}\|$ = 10 $V_{P-P,}$ R_L = 2.2 kΩ) T_A = 25°C (Note 3) (Fig. 23)	$\|CM_L\|$	6N138, 6N139	1,000	10,000		V/µs
	Each Channel		HCPL-2730, HCPL-2731				

** All typicals at T_A = 25°C

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ISOLATION CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) (T_A = 25°C, t = 5 s) (V_{I-O} = 3000 VDC) (Note 8)	I_{I-O}			1.0	µA
Withstand insulation test voltage	(RH ≤ 50%, T_A = 25°C) (Note 4) (t = 1 min.)	V_{ISO}	2500			V_{RMS}
Resistance (input to output)	(Note 4) (V_{I-O} = 500 VDC)	R_{I-O}		10^{12}		Ω
Capacitance (input to output)	(Note 4,5) (f = 1 MHz)	C_{I-O}		0.6		pF
Input-Input Insulation leakage current	(RH ≤ 45%, V_{I-I} = 500 VDC) (Note 6) t = 5 s, (HCPL-2730/2731 only)	I_{I-I}		0.005		µA
Input-Input Resistance	(V_{I-I} = 500 VDC) (Note 6) (HCPL-2730/2731 only)	R_{I-I}		10^{11}		Ω
Input-Input Capacitance	(f = 1 MHz) (Note 6) (HCPL-2730/2731 only)	C_{I-I}		0.03		pF

** All typicals at T_A = 25°C

NOTES

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 open. (6N138 and 6N139 only)
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic high state (i.e., $V_O > 2.0$ V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., $V_O < 0.8$ V).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. For dual channel devices, C_{I-O} is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
6. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Current Limiting Resistor Calculations

$$R_1 \text{ (Non-Invert)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} - = V_{OLX} \text{ (@ } I_L - I_2)}{I_L}$$

Where:

V_{DD1} - Input Supply Voltage
V_{DD2} - Output Supply Voltage
V_{DF} - Diode Forward Voltage
V_{OL1} - Logic “0” Voltage of Driver
V_{OH1} - Logic “1” Voltage of Driver
I_F - Diode Forward Current
V_{OLX} - Saturation Voltage of Output Transistor
I_L - Load Current Through Resistor R2
I_2 - Input Current of Output Gate

INPUT			OUTPUT						
			CMOS @ 5 V	CMOS @ 10 V	74XX	74LXX	74SXX	74LSXX	74HXX
		R1 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10 V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Fig. 1 Resistor Values for Logic Interface

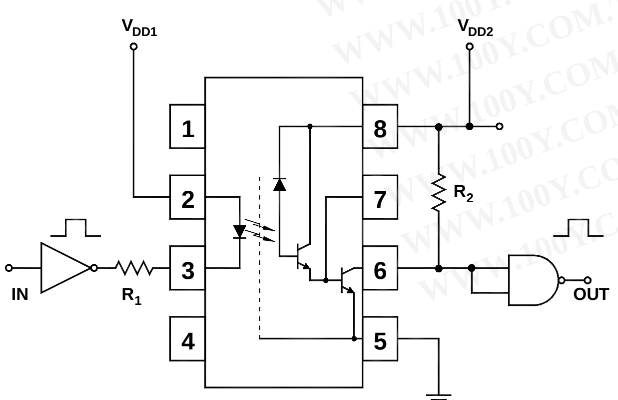

Fig. 2 Non-Inverting Logic Interface

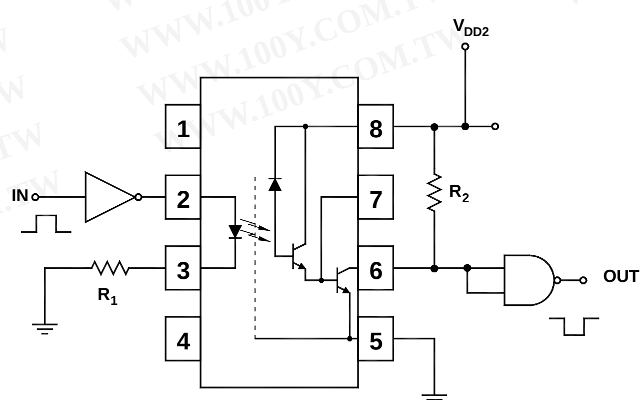

Fig. 3 Inverting Logic Interface

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Fig. 4 LED Forward Current vs. Forward Voltage

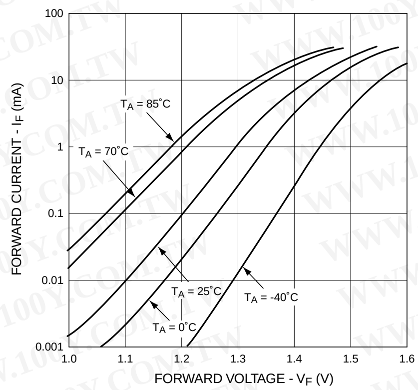


Fig. 5 LED Forward Voltage vs. Temperature

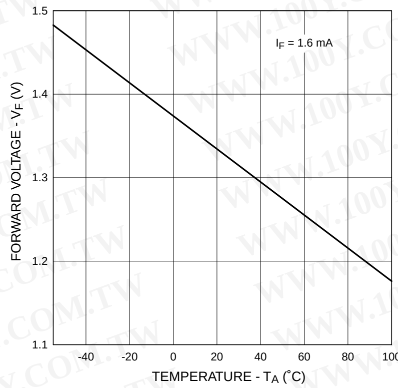


Fig. 6 Non-saturated Rise and Fall Times vs. Load Resistance (6N138 / 6N139 Only)

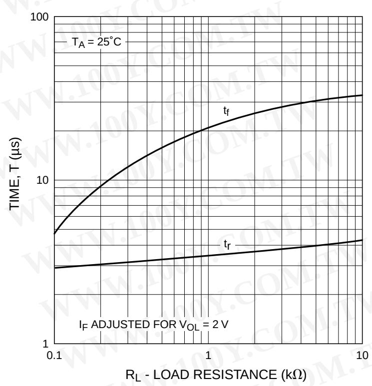


Fig. 7 Non-saturated Rise and Fall Times vs. Load Resistance (HCPL-2730 / HCPL-2731 Only)

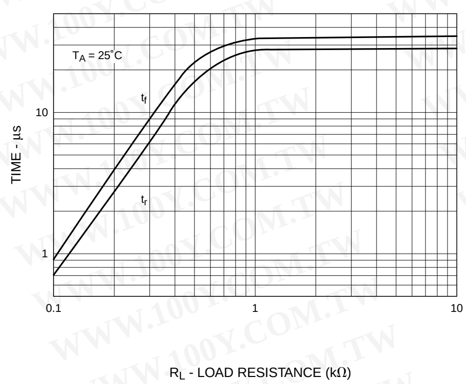


Fig. 8 Current Transfer Ratio vs. Forward Current (6N138 / 6N139 Only)

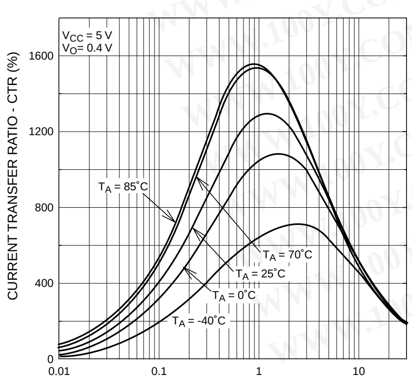
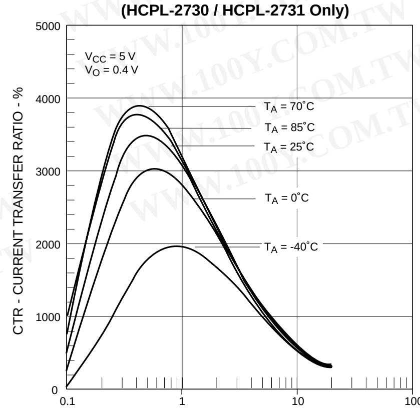


Fig. 9 Current Transfer Ratio vs. Forward Current (HCPL-2730 / HCPL-2731 Only)



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6N139	HCPL-2731

Fig. 10 Output Current vs Output Voltage (6N138 / 6N139 Only)

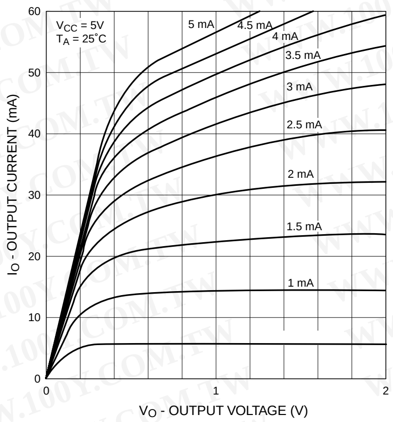


Fig. 11 Output Current vs Output Voltage (HCPL-2730 / HCPL-2731 Only)

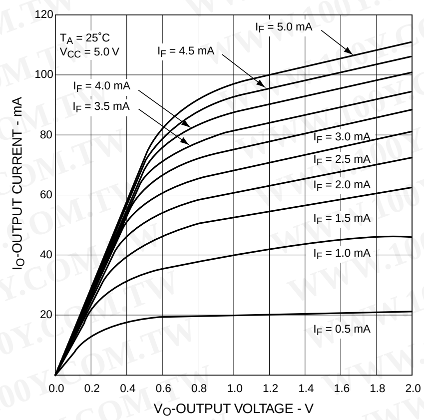


Fig. 12 Output Current vs. Input Diode Forward Current (6N138 / 6N139 Only)

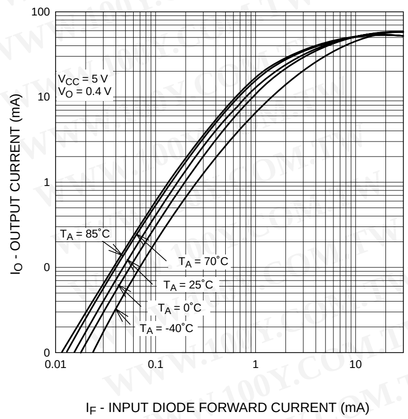


Fig. 13 Output Current vs Input Diode Forward Current (HCPL-2730 / HCPL-2731 Only)

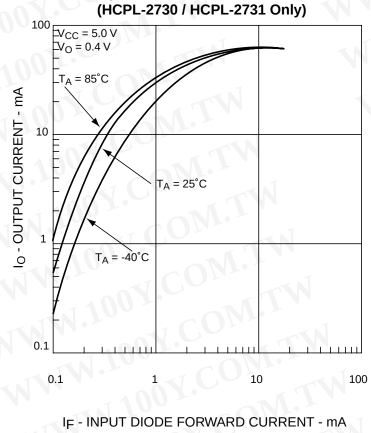


Fig. 14 Logic Low Supply Current vs. Input Diode Forward Current (6N138 / 6N139 Only)

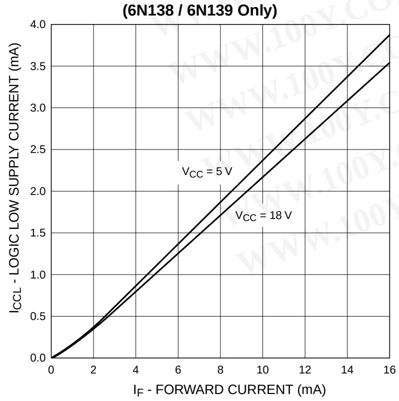


Fig. 15 Logic Low Supply Current vs. Input Diode Forward Current (HCPL-2730 / HCPL-2731 Only)

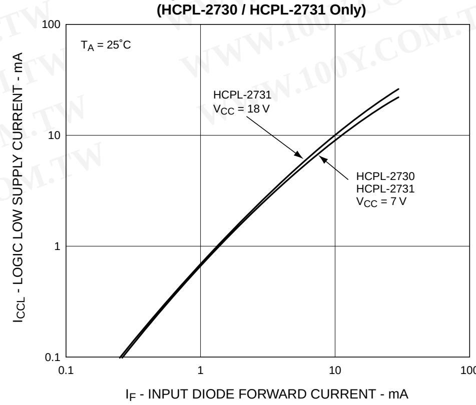


Fig. 16 Propagation Delay vs. Input Diode Forward Current (6N138 / 6N139 Only)

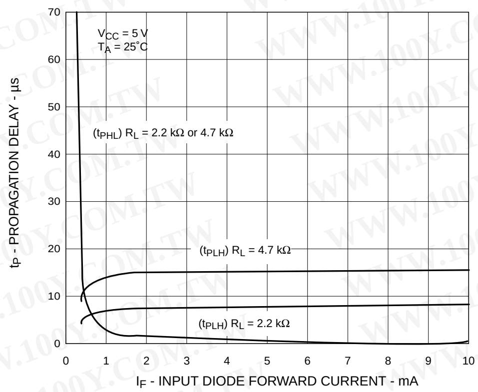


Fig. 17 Propagation Delay vs. Input Diode Forward Current (HCPL-2730 / HCPL-2731 Only)

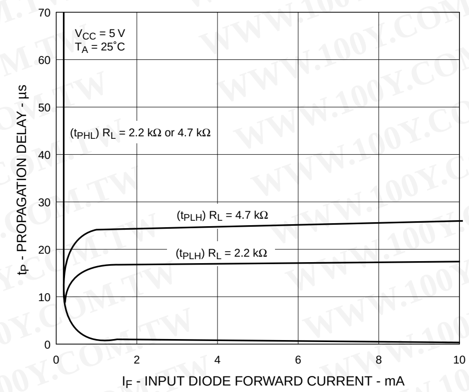


Fig. 18 Propagation Delay to Logic Low vs. Pulse Period (6N138 / 6N139 Only)

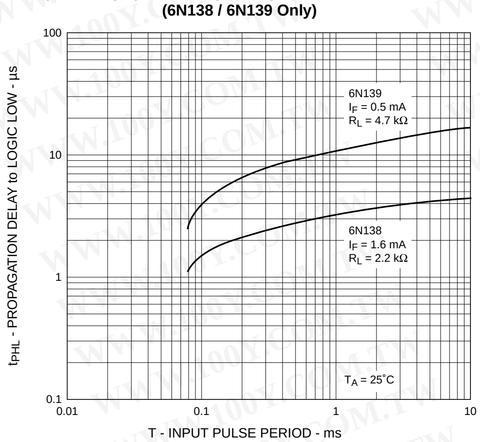


Fig. 19 Propagation Delay to Logic Low vs. Pulse Period (HCPL-2730 / HCPL-2731 Only)

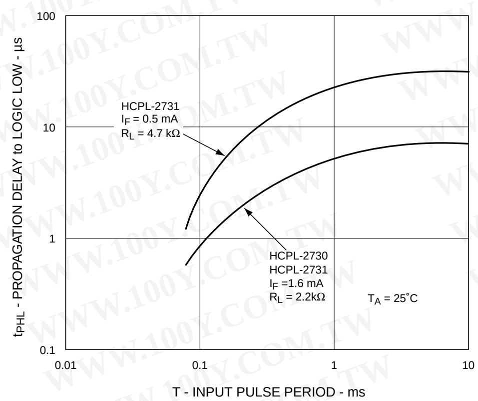


Fig. 20 Propagation Delay vs. Temperature (6N138 / 6N139 Only)

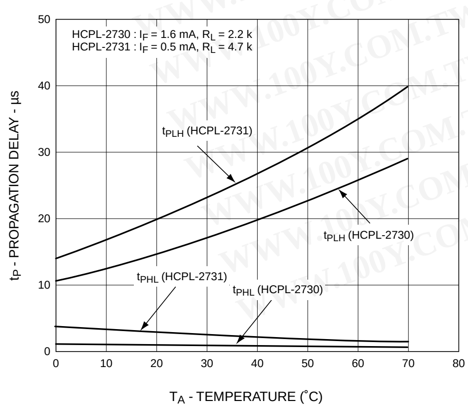
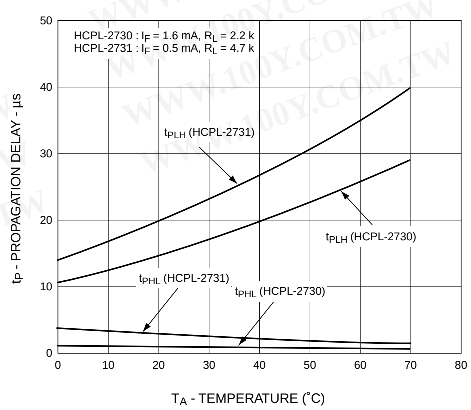


Fig. 21 Propagation Delay vs. Temperature (HCPL-2730 / HCPL-2731 Only)



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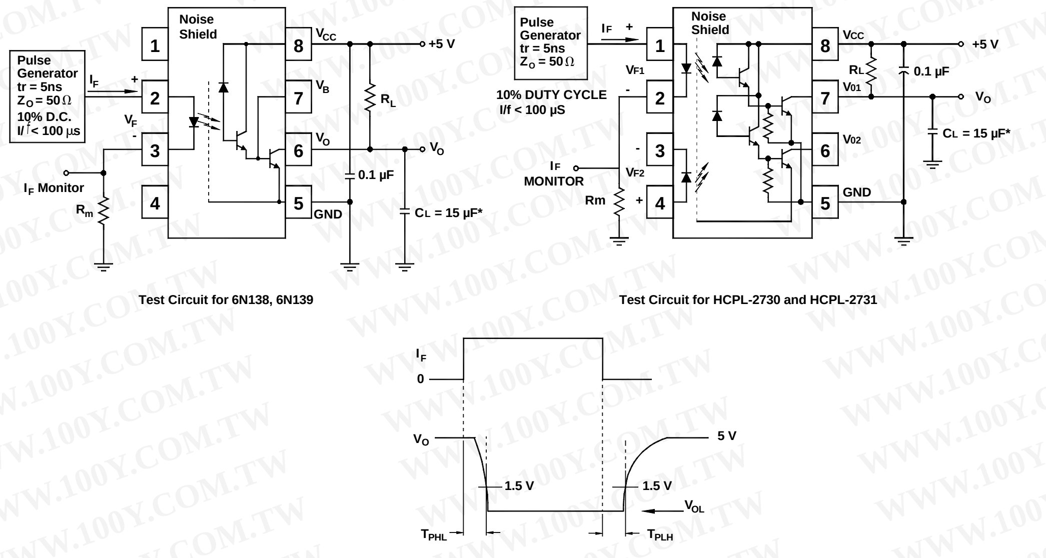
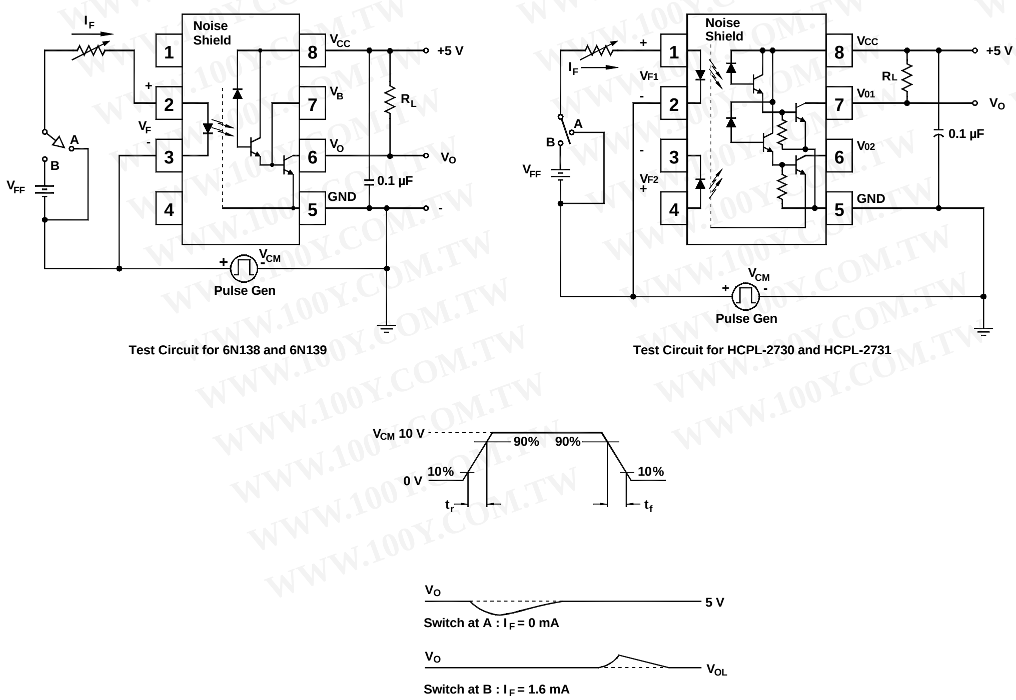


Test Circuit for 6N138, 6N139

Test Circuit for HCPL-2730 and HCPL-2731

Fig. 22 Switching Time Test Circuit

*Includes Probe and Fixture Capacitance



Test Circuit for 6N138 and 6N139

Test Circuit for HCPL-2730 and HCPL-2731

Fig. 23 Common Mode Immunity Test Circuit

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SINGLE-CHANNEL	DUAL-CHANNEL
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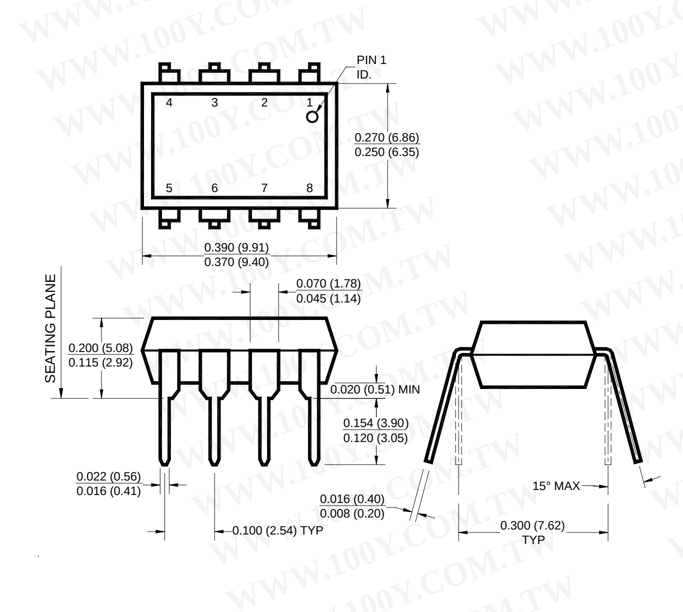
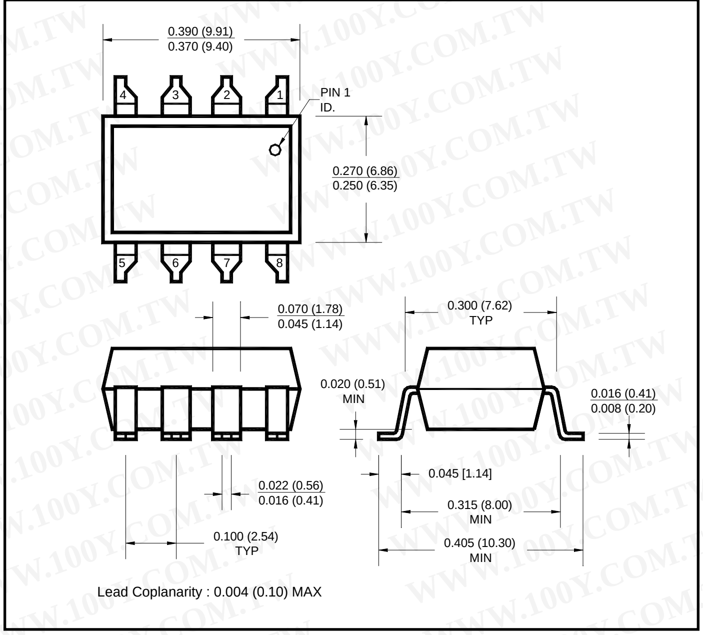
6N139	HCPL-2731

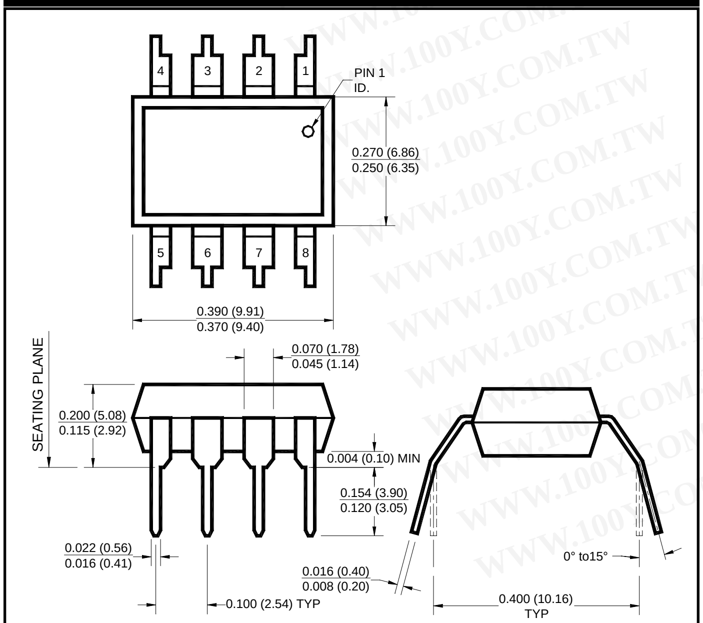
Package Dimensions (Through Hole)



Package Dimensions (Surface Mount)



Package Dimensions (0.4"Lead Spacing)



NOTE

All dimensions are in inches (millimeters)

www.qtopto.com

Call QT Optoelectronics for more information or the phone number of your nearest distributor.

United States 800-533-6786 • France 33 [0] 1.45.18.78.78 • Germany 49 [0] 89/96.30.51 • United Kingdom 44 [0] 1296 394499 • Asia/Pacific 603-7352417

QT OPTOELECTRONICS

LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON OPTOCOUPLERS

SINGLE-CHANNEL	DUAL-CHANNEL
6N138	HCPL-2730
6N139	HCPL-2731

ORDERING INFORMATION

Option	Order Entry Identifier	Description
R2	.R2	Opto Plus Reliability Conditioning
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
W	.W	0.4" Lead Spacing

QT Carrier Tape Specifications ("D" Taping Orientation)