

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
 Http://www.100y.com.tw

FAIRCHILD
 SEMICONDUCTOR™

November 1988
 Revised November 1999

74AC244 • 74ACT244

Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The AC/ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

Features

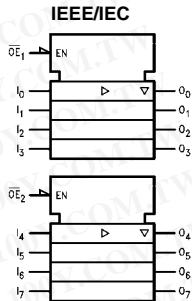
- I_{CC} and I_{OZ} reduced by 50%
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- ACT244 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74AC244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT244MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ACT244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

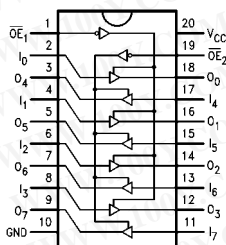
Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I_0-I_7	Inputs
O_0-O_7	Outputs

Connection Diagram



FACT™ is a trademark of Fairchild Semiconductor Corporation.

Truth Tables

Inputs		Outputs
\overline{OE}_1	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

X = Immaterial
 Z = High Impedance

74AC244 • 74ACT244 Octal Buffer/Line Driver with 3-STATE Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-
out exception, to ensure that the system design is reliable over its power
supply, temperature, and output/input loading variables. Fairchild does not
recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -55^\circ C$ to $+125^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Typ	Guaranteed Limits		Guaranteed Limits					
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15	3.15	3.15				
		5.5	2.75	3.85	3.85	3.85	3.85				
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35	1.35	1.35				
		5.5	2.75	1.65	1.65	1.65	1.65				
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4	4.4	4.4				
		5.5	5.49	5.4	5.4	5.4	5.4				
		3.0		2.56	2.4	2.4	2.46	V	$I_{OH} = 12 mA$ $I_{OH} = 24 mA$ $I_{OH} = 24 mA$ (Note 2)		
		4.5		3.86	3.7	3.7	3.76				
		5.5		4.86	4.7	4.7	4.76				
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1	0.1	0.1				
		5.5	0.001	0.1	0.1	0.1	0.1				
		3.0		0.36	0.50	0.50	0.44	V			$I_{OL} = 12 mA$ $I_{OL} = 24 mA$ $I_{OL} = 24 mA$ (Note 2)
4.5		0.36	0.50	0.50	0.44						
5.5		0.36	0.50	0.50	0.44						
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	±1.0	μA	$V_I = V_{CC}, GND$		
I_{OZ}	Maximum 3-STATE Current	5.5		±0.25	±5.0	±2.5	±2.5	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}, V_{GND}$ $V_O = V_{CC}, GND$		
I_{OLD}	Minimum Dynamic	5.5			50	75		mA	$V_{OLD} = 1.65V$ Max		
I_{OHD}	Output Current (Note 3)	5.5			-50	-75		mA	$V_{OHD} = 3.85V$ Min		
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	40.0	μA	$V_{IN} = V_{CC}$ or GND		

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

DC Electrical Characteristics for ACT									
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -55°C to +125°C	T _A = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits					
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4	5.4			
		4.5		3.86	3.70	3.76			V
5.5		4.86	4.70	4.76					
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1	0.1			
		4.5		0.36	0.50	0.44			V
5.5		0.36	0.50	0.44					
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-STATE Current	5.5		±0.25	±5.0	±2.5	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CC}	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	Minimum Dynamic	5.5			50	75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 6)	5.5			-50	-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V _{IN} = V _{CC} or GND	

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0	1.0	12.5	1.5	10.0	ns
		5.0	1.5	5.0	7.0	1.0	9.5	1.0	7.5	
t _{PHL}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0	1.0	12.0	2.0	10.0	ns
		5.0	1.5	5.0	7.0	1.0	9.0	1.0	7.5	
t _{PZH}	Output Enable Time	3.3	2.0	6.0	10.5	1.0	11.5	1.5	11.0	ns
		5.0	1.5	5.0	7.0	1.0	9.0	1.5	8.0	
t _{PZL}	Output Enable Time	3.3	2.5	7.5	10.0	1.0	13.0	2.0	11.0	ns
		5.0	1.5	5.5	8.0	1.0	10.5	1.5	8.5	
t _{PHZ}	Output Disable Time	3.3	3.0	7.0	10.0	1.0	12.5	1.5	10.5	ns
		5.0	2.5	6.5	9.0	1.0	10.5	1.0	9.5	
t _{PLZ}	Output Disable Time	3.3	2.5	7.5	10.5	1.0	13.0	2.5	11.5	ns
		5.0	2.0	6.5	9.0	1.0	11.0	2.0	9.5	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) (Note 8)	T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	5.0	2.0	6.5	9.0	1.0	10.0	1.5	10.0	ns
		5.0	2.0	7.0	9.0	1.0	10.0	1.5	10.0	
t _{PHL}	Propagation Delay Data to Output	5.0	2.0	7.0	9.0	1.0	10.0	1.5	10.0	ns
t _{PZH}	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	1.0	9.5	ns
t _{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns
t _{PHZ}	Output Disable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns
t _{PLZ}	Output Disable Time	5.0	2.5	7.5	10.0	1.0	11.5	2.0	10.5	ns

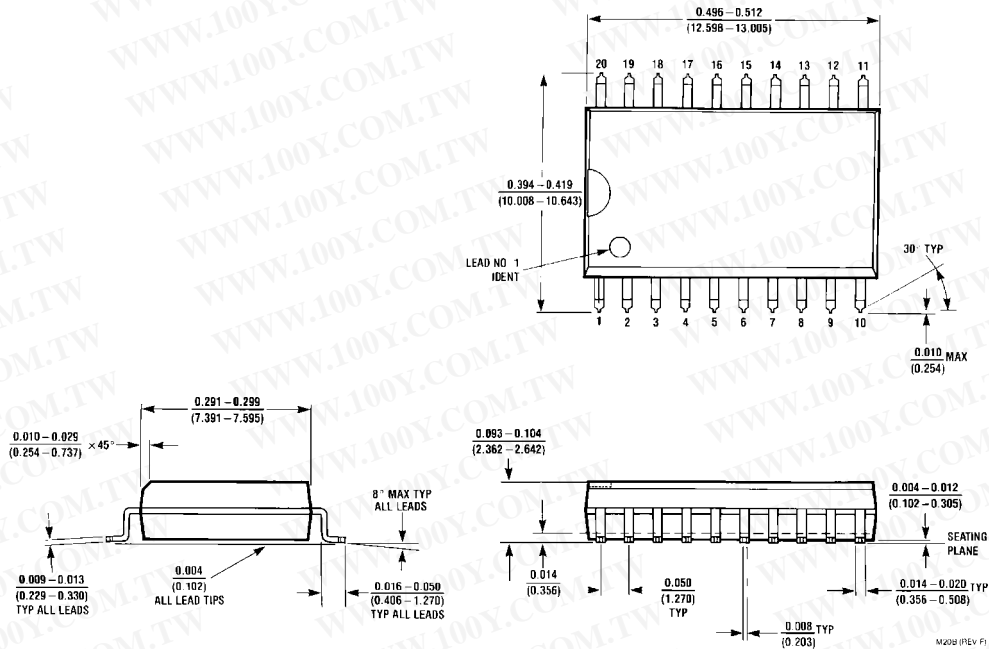
Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	45.0	pF	V _{CC} = 5.0V

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Physical Dimensions inches (millimeters) unless otherwise noted

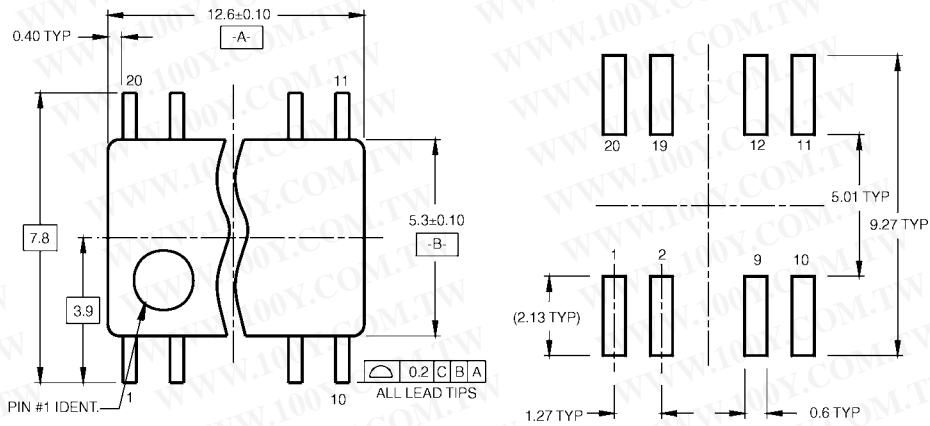


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body Package Number M20B

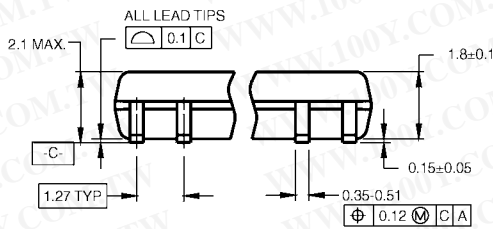
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

74AC244 • 74ACT244

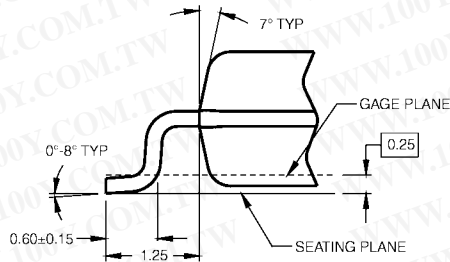
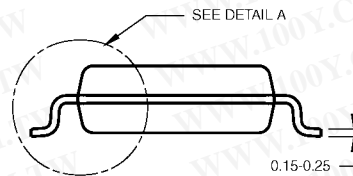
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

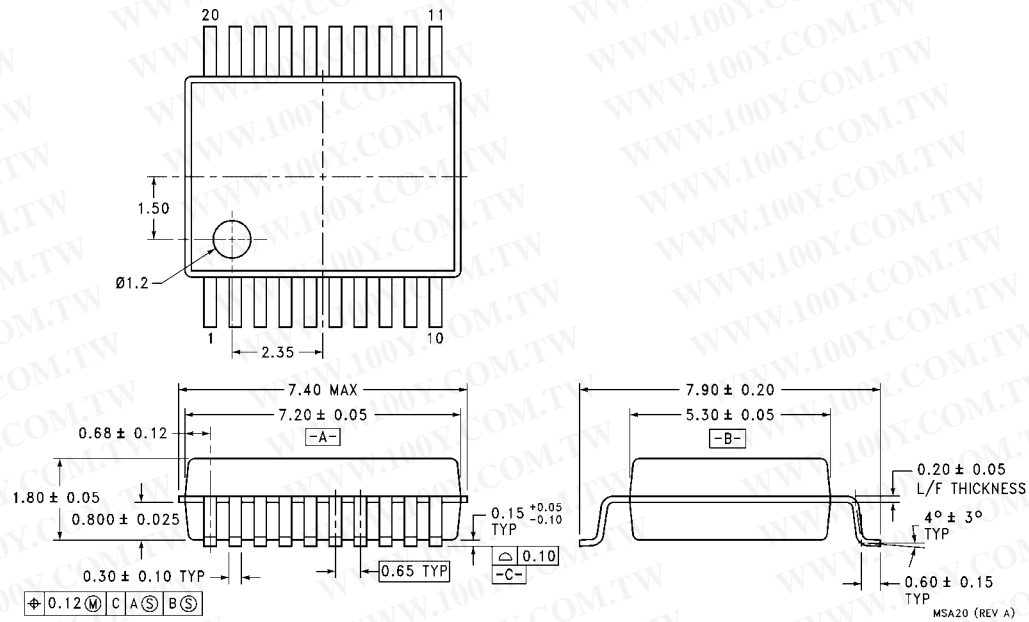
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

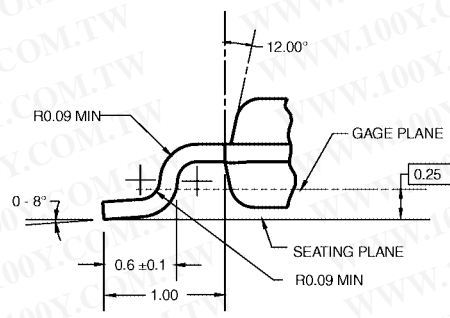
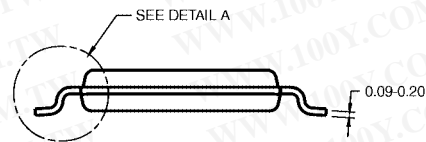
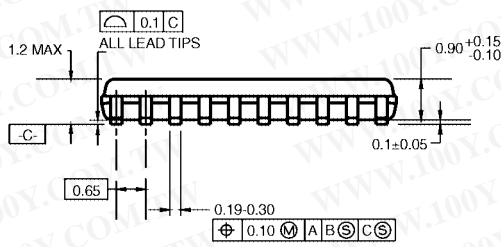
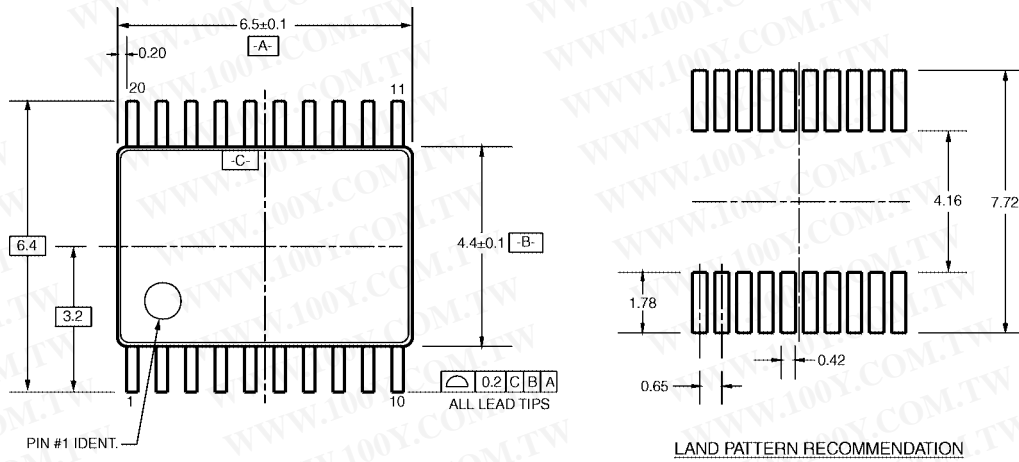
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

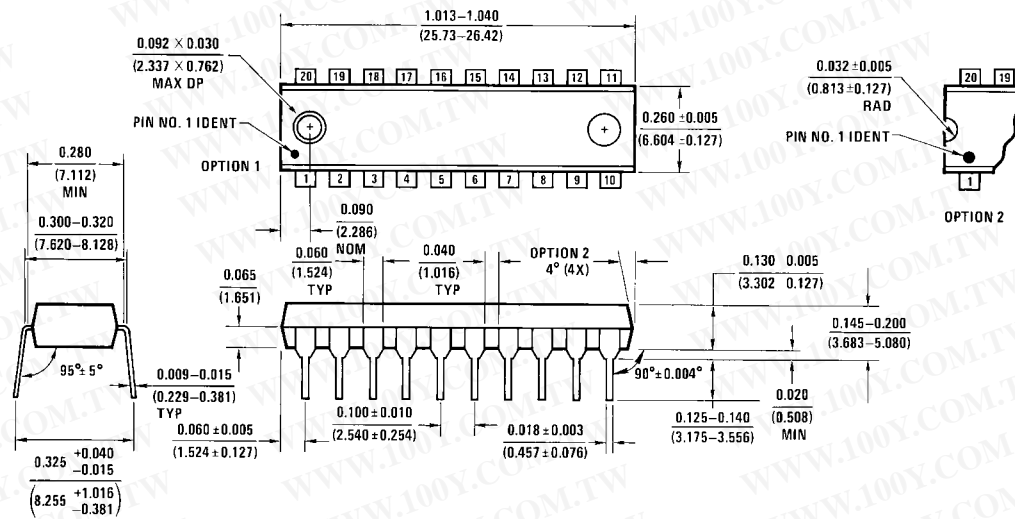
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com