



April 1988
Revised September 2000

74F175 Quad D-Type Flip-Flop

General Description

The 74F175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, LOW.

Features

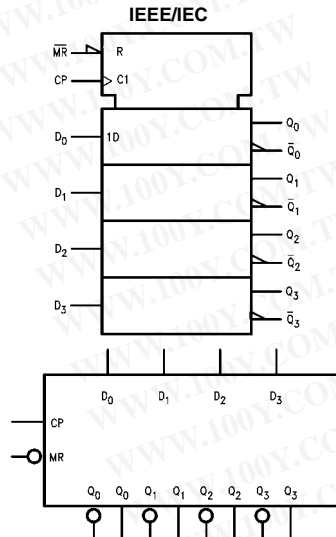
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output

Ordering Code:

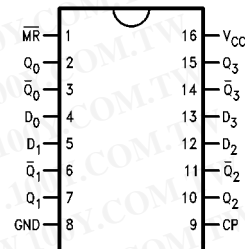
Order Number	Package Number	Package Description
74F175SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F175PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



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Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_3	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/-0.6 mA
\overline{MR}	Master Reset Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
Q_0-Q_3	True Outputs	50/33.3	-1 mA/20 mA
$\overline{Q_0}-\overline{Q_3}$	Complement Outputs	50/33.3	-1 mA/20 mA

Functional Description

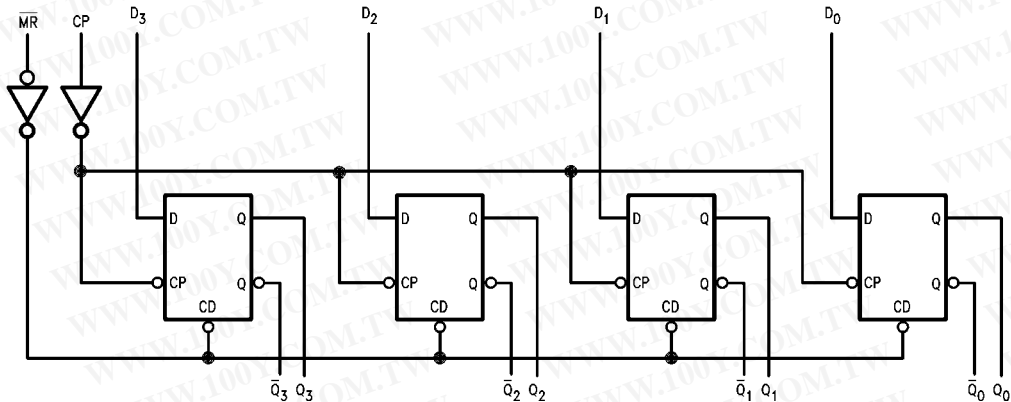
The 74F175 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and \overline{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \overline{Q} outputs to follow. A LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \overline{Q} outputs HIGH independent of Clock or Data inputs. The 74F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs			Outputs	
\overline{MR}	CP	D_n	Q_n	$\overline{Q_n}$
L	X	X	L	H
H	↗	H	H	L
H	↗	L	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)


Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IDP} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		22.5	34.0	mA	Max	CP =  D _n = MR = HIGH

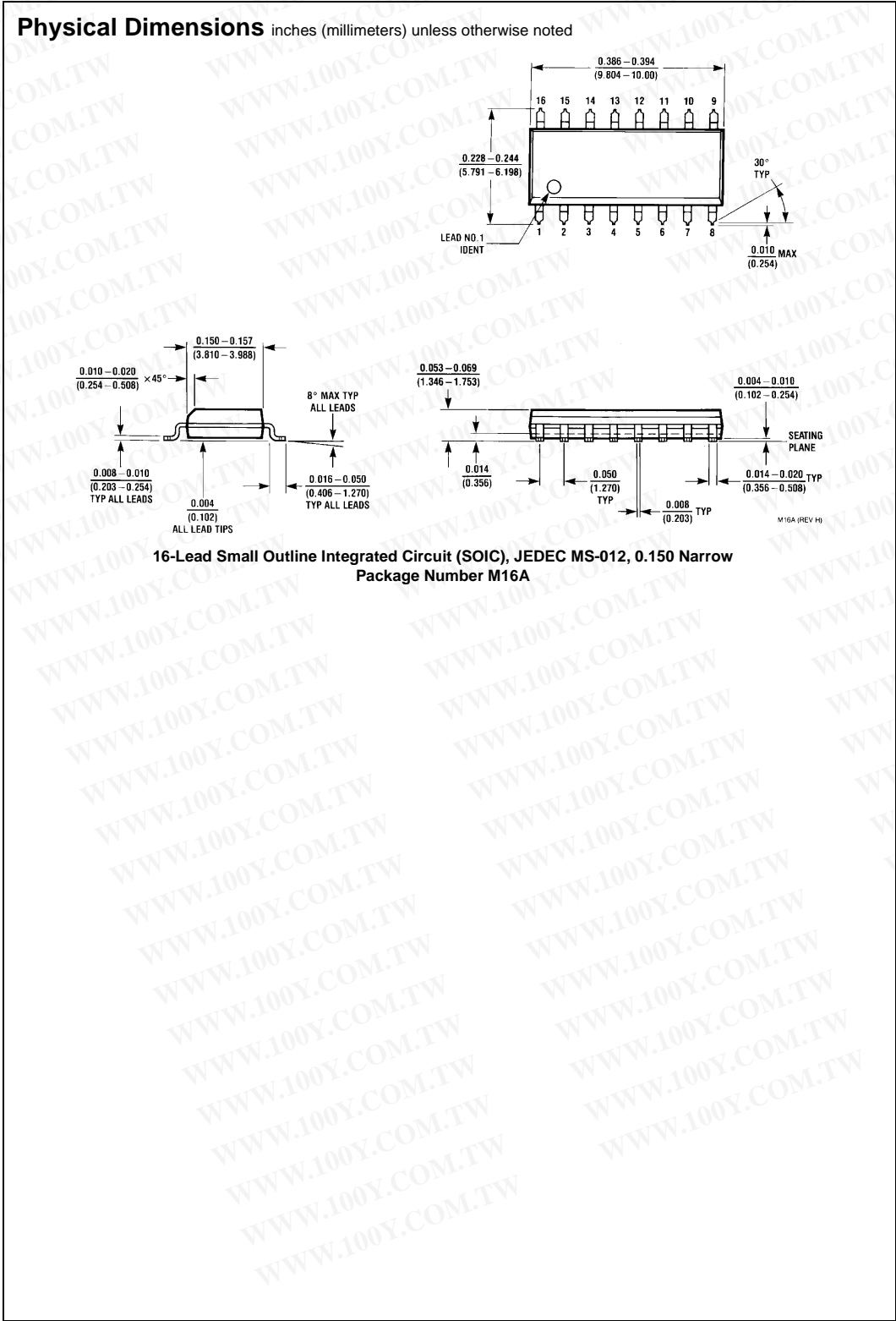
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AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	140		80		100		MHz
t _{PLH}	Propagation Delay CP to Q _n or \overline{Q}_n	4.0	5.0	6.5	3.5	8.5	4.0	7.5	ns
t _{PHL}	Propagation Delay MR to Q _n	4.0	6.5	8.5	4.0	10.5	4.0	9.5	ns
t _{PLH}	Propagation Delay MR to \overline{Q}_n	4.5	9.0	11.5	4.5	15.0	4.5	13.0	ns
t _{PLH}	Propagation Delay MR to \overline{Q}_n	4.0	6.5	8.0	4.0	10.0	4.0	9.0	ns

AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns
t _S (L)	D _n to CP	3.0		3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0		1.0		1.0		
t _H (L)	D _n to CP	1.0		2.0		1.0		ns
t _W (H)	CP Pulse Width	4.0		4.0		4.0		
t _W (L)	HIGH or LOW	5.0		5.0		5.0		
t _W (L)	MR Pulse Width, LOW	5.0		5.0		5.0		ns
t _{REC}	Recovery Time, MR to CP	5.0		5.0		5.0		ns



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0.47 TYP

10.2±0.1

-A-

16

9

7.8

3.9

5.3±0.1

-B-

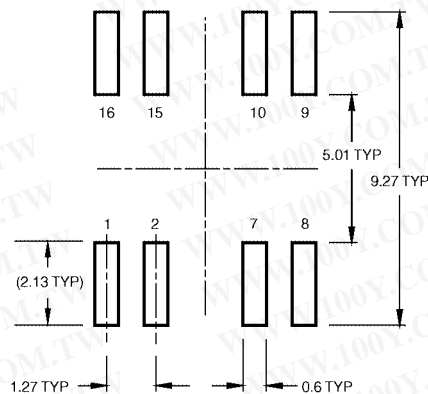
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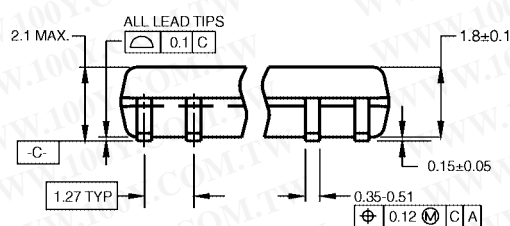
	0.2	C	B	A
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PIN #1 IDENT

ALL LEAD TIPS



LAND PATTERN RECOMMENDATION

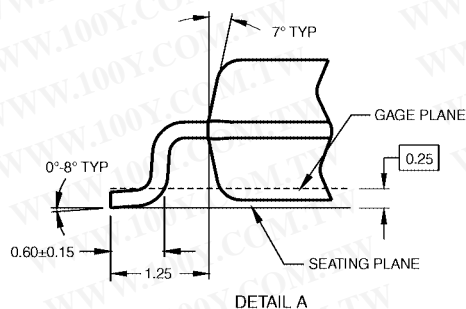
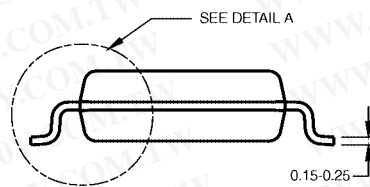


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

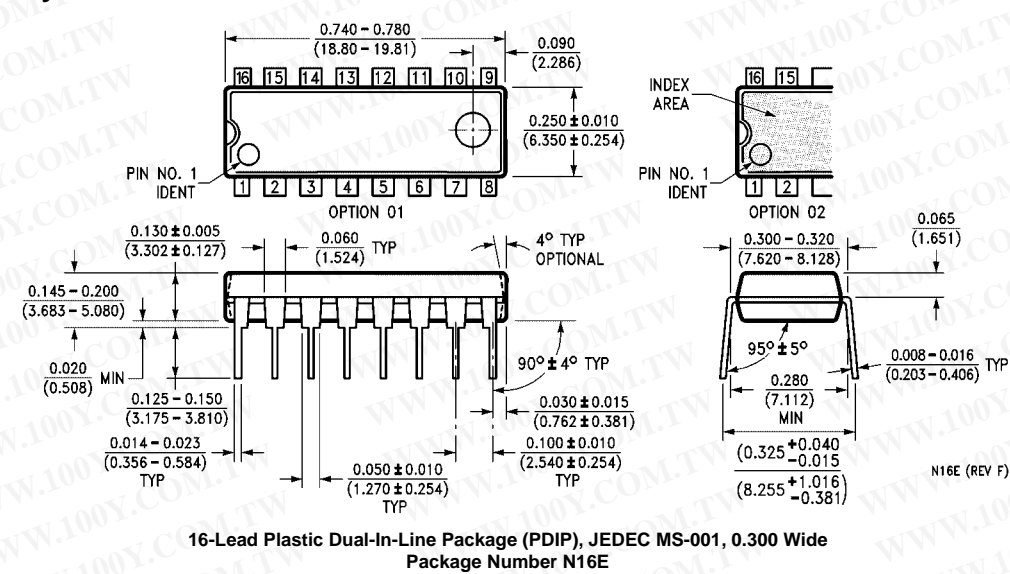


DETAIL A

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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