DATA SHEET

74LVC4245A
Octal dual supply translating transceiver; 3-state

Product specification
Supersedes data of 2004 Feb 11

2004 Mar 30

Philips Semiconductors

PHILIPS

Octal dual supply translating transceiver; 3-state 74LVC4245A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range:
  - 3 V port (V_{CCB}): 1.5 V to 3.6 V
  - 5 V port (V_{CCA}): 1.5 V to 5.5 V.
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when V_{CC} = 0 V
- Complies with JEDEC standard no. JESD8B/JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC4245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

The 74LVC4245A features an output enable input (pin $\overline{OE}$) for easy cascading and a send/receive input (pin DIR) for direction control. Pin $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typical 0.7 V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}	propagation delay An to Bn	C_L = 50 pF; V_{CCA} = 5.0 V; V_{CCB} = 3.3 V	3.3	ns
	propagation delay Bn to An	C_L = 50 pF; V_{CCA} = 5.0 V; V_{CCB} = 3.3 V	3.4	ns
t_{PLH}	propagation delay An to Bn	C_L = 50 pF; V_{CCA} = 5.0 V; V_{CCB} = 3.3 V	2.8	ns
	propagation delay Bn to An	C_L = 50 pF; V_{CCA} = 5.0 V; V_{CCB} = 3.3 V	3.0	ns
C_I	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance An and Bn		5.0	pF
C_{PD}	5 V port: power dissipation capacitance Bn to An	V_{CC} = 5.0 V; notes 1 and 2 outputs enabled outputs disabled	 17 5	 pF pF
	3 V port: power dissipation capacitance An to Bn	V_{CC} = 3.3 V; notes 1 and 2 outputs enabled outputs disabled	 17 5	 pF pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		INPUT/OUTPUT	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC4245AD	–40 °C to +125 °C	24	SO24	plastic	SOT137-1
74LVC4245ADB	–40 °C to +125 °C	24	SSOP24	plastic	SOT340-1
74LVC4245APW	–40 °C to +125 °C	24	TSSOP24	plastic	SOT355-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	V_{CCA}	supply voltage (5 V bus)
2	DIR	direction control
3	A0	data input or output
4	A1	data input or output
5	A2	data input or output
6	A3	data input or output
7	A4	data input or output
8	A5	data input or output
9	A6	data input or output
10	A7	data input or output
11	GND	ground (0 V)
12	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
13	GND	ground (0 V)
14	B7	data output or input
15	B6	data output or input
16	B5	data output or input
17	B4	data output or input
18	B3	data output or input
19	B2	data output or input
20	B1	data output or input
21	B0	data output or input
22	$\overline{OE}$	output enable input (active LOW)
23	V_{CCB}	supply voltage (3 V bus)
24	V_{CCB}	supply voltage (3 V bus)

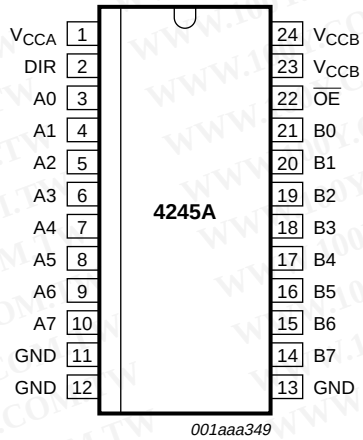


Fig.1 Pin configuration.

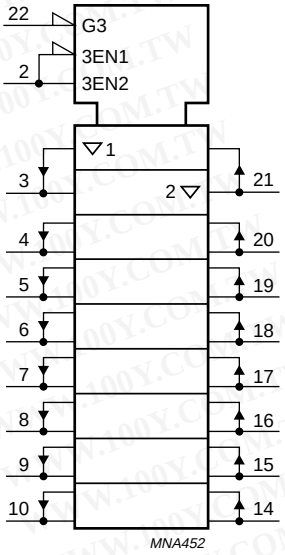


Fig.2 IEC logic symbol.

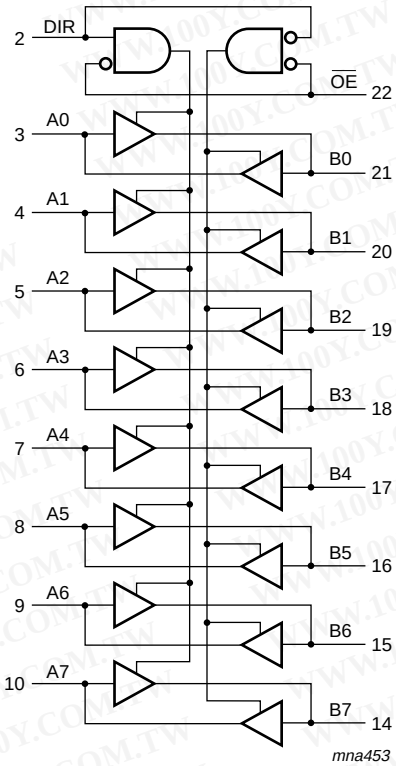


Fig.3 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	supply voltage 5 V port (for maximum speed performance)	$V_{CCA} \geq V_{CCB}$; see Fig.4	1.5	5.5	V
V_{CCB}	supply voltage 3 V port (for low-voltage applications)	$V_{CCA} \geq V_{CCB}$; see Fig.4	1.5	3.6	V
V_I	input voltage (control inputs)		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CCB} = 2.7 V to 3.0 V	0	20	ns/V
		V_{CCB} = 3.0 V to 3.6 V	0	10	ns/V
		V_{CCA} = 3.0 V to 4.5 V	0	20	ns/V
		V_{CCA} = 4.5 V to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	supply voltage 5 V port		–0.5	+6.5	V
V_{CCB}	supply voltage 3 V port		–0.5	+4.6	V
I_{IK}	input diode current	$V_I < 0$ V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		output 3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
   For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CCA} (V)	V_{CCB} (V)				
T_{amb} = –40 °C to +85 °C; note 1								
V_{IH}	HIGH-level input voltage		–	2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	–	2.0	–	–	V
V_{IL}	LOW-level input voltage		–	2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –12 mA	–	2.7	V_{CCB} – 0.5	–	–	V
		I_O = –100 µA	–	2.7 to 3.6	V_{CCB} – 0.2	V_{CCB}	–	V
		I_O = –24 mA	–	3.0	V_{CCB} – 0.8	–	–	V
		V_I = V_{IH} or V_{IL}						
		I_O = –12 mA	4.5	–	V_{CCA} – 0.5	–	–	V
		I_O = –100 µA	4.5 to 5.5	–	V_{CCA} – 0.2	V_{CCA}	–	V
		I_O = –24 mA	4.5	–	V_{CCA} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 12 mA	–	2.7	–	–	0.40	V
		I_O = 100 µA	–	2.7 to 3.6	–	–	0.20	V
		I_O = 24 mA	–	3.0	–	–	0.55	V
		V_I = V_{IH} or V_{IL}						
		I_O = 12 mA	4.5	–	–	–	0.40	V
		I_O = 100 µA	4.5 to 5.5	–	–	–	0.20	V
		I_O = 24 mA	4.5	–	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	–	–	–	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; note 2	–	3.6	–	±0.1	±5	µA
			5.5	–	–	±0.1	±5	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	–	3.6	–	0.1	10	µA
			5.5	–	–	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per control pin	V_I = V_{CC} – 0.6 V; I_O = 0 A; note 3	–	2.7 to 3.6	–	5	500	µA
			4.5 to 5.5	–	–	5	500	µA

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CCA} (V)	V_{CCB} (V)				
T_{amb} = −40 °C to +125 °C								
V_{IH}	HIGH-level input voltage		–	2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	–	2.0	–	–	V
V_{IL}	LOW-level input voltage		–	2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −12 mA	–	2.7	V_{CCB} − 0.65	–	–	V
		I_O = −100 µA	–	2.7 to 3.6	V_{CCB} − 0.3	–	–	V
		I_O = −24 mA	–	3.0	V_{CCB} − 1.0	–	–	V
		V_I = V_{IH} or V_{IL}						
		I_O = −12 mA	4.5	–	V_{CCA} − 0.65	–	–	V
		I_O = −100 µA	4.5 to 5.5	–	V_{CCA} − 0.3	–	–	V
		I_O = −24 mA	4.5	–	V_{CCA} − 1.0	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 12 mA	–	2.7	–	–	0.60	V
		I_O = 100 µA	–	2.7 to 3.6	–	–	0.30	V
		I_O = 24 mA	–	3.0	–	–	0.80	V
		V_I = V_{IH} or V_{IL}						
		I_O = 12 mA	4.5	–	–	–	0.60	V
		I_O = 100 µA	4.5 to 5.5	–	–	–	0.30	V
		I_O = 24 mA	4.5	–	–	–	0.80	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	–	–	–	–	±20	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; note 2	–	3.6	–	–	±20	µA
			5.5	–	–	–	±20	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	–	3.6	–	–	40	µA
			5.5	–	–	–	40	µA
ΔI_{CC}	additional quiescent supply current per control pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; note 3	–	2.7 to 3.6	–	–	5000	µA
			4.5 to 5.5	–	–	–	5000	µA

Notes

1. All typical values are at V_{CCA} = 5.0 V, V_{CCB} = 3.3 V and T_{amb} = 25 °C.
2. For transceivers, the parameter I_{OZ} includes the input leakage current.
3. V_{CCB} = 2.7 V to 3.6 V: other inputs at V_{CCB} or GND.
   V_{CCA} = 4.5 V to 5.5 V: other inputs at V_{CCA} or GND.

AC CHARACTERISTICS

GND = 0 V; V_{CCA} = 4.5 V to 5.5 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CCB} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}	propagation delay An to Bn	see Figs 5 and 7	2.7	1.0	3.6	6.3	ns
			3.0 to 3.6	1.0	3.3[2]	6.3	ns
	propagation delay Bn to An		2.7	1.0	3.4	6.1	ns
			3.0 to 3.6	1.0	3.4[2]	6.1	ns
t_{PLH}	propagation delay An to Bn		2.7	1.0	3.3	6.7	ns
			3.0 to 3.6	1.0	2.8[2]	6.5	ns
	propagation delay Bn to An		2.7	1.0	3.0	5.0	ns
			3.0 to 3.6	1.0	3.0[2]	5.0	ns
t_{PZL}	3-state output enable time $\overline{OE}$ to An	see Figs 6 and 7	2.7	1.0	4.5	9.0	ns
			3.0 to 3.6	1.0	4.5[2]	9.0	ns
	3-state output enable time $\overline{OE}$ to Bn		2.7	1.0	4.4	8.7	ns
			3.0 to 3.6	1.0	3.8[2]	8.1	ns
t_{PZH}	3-state output enable time $\overline{OE}$ to An		2.7	1.0	4.5	8.1	ns
			3.0 to 3.6	1.0	4.5[2]	8.1	ns
	3-state output enable time $\overline{OE}$ to Bn		2.7	1.0	4.3	8.7	ns
			3.0 to 3.6	1.0	3.2[2]	8.1	ns
t_{PLZ}	3-state output disable time $\overline{OE}$ to An	see Figs 6 and 7	2.7	1.0	2.9	7.0	ns
			3.0 to 3.6	1.0	2.9[2]	7.0	ns
	3-state output disable time $\overline{OE}$ to Bn		2.7	1.0	3.9	7.7	ns
			3.0 to 3.6	1.0	3.5[2]	7.7	ns
t_{PHZ}	3-state output disable time $\overline{OE}$ to An		2.7	1.0	2.8	5.8	ns
			3.0 to 3.6	1.0	2.8[2]	5.8	ns
	3-state output disable time $\overline{OE}$ to Bn		2.7	1.0	3.3	7.8	ns
			3.0 to 3.6	1.0	2.9[2]	7.8	ns
$t_{sk(0)}$	skew	note 3		–	–	1.0	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CCB} (V)				
T_{amb} = −40 °C to +125 °C							
t_{PHL}	propagation delay An to Bn	see Figs 5 and 7	2.7	1.0	–	8.0	ns
			3.0 to 3.6	1.0	–	8.0	ns
	propagation delay Bn to An		2.7	1.0	–	8.0	ns
			3.0 to 3.6	1.0	–	8.0	ns
t_{PLH}	propagation delay An to Bn		2.7	1.0	–	8.5	ns
			3.0 to 3.6	1.0	–	8.5	ns
	propagation delay Bn to An		2.7	1.0	–	6.5	ns
			3.0 to 3.6	1.0	–	6.5	ns
t_{PZL}	3-state output enable time $\overline{OE}$ to An	see Figs 6 and 7	2.7	1.0	–	11.5	ns
			3.0 to 3.6	1.0	–	11.5	ns
	3-state output enable time $\overline{OE}$ to Bn		2.7	1.0	–	11.0	ns
			3.0 to 3.6	1.0	–	10.5	ns
t_{PZH}	3-state output enable time $\overline{OE}$ to An		2.7	1.0	–	10.5	ns
			3.0 to 3.6	1.0	–	10.5	ns
	3-state output enable time $\overline{OE}$ to Bn		2.7	1.0	–	11.0	ns
			3.0 to 3.6	1.0	–	10.5	ns
t_{PLZ}	3-state output disable time $\overline{OE}$ to An	see Figs 6 and 7	2.7	1.0	–	9.0	ns
			3.0 to 3.6	1.0	–	9.0	ns
	3-state output disable time $\overline{OE}$ to Bn		2.7	1.0	–	10.0	ns
			3.0 to 3.6	1.0	–	10.0	ns
t_{PHZ}	3-state output disable time $\overline{OE}$ to An		2.7	1.0	–	7.5	ns
			3.0 to 3.6	1.0	–	7.5	ns
	3-state output disable time $\overline{OE}$ to Bn		2.7	1.0	–	10.0	ns
			3.0 to 3.6	1.0	–	10.0	ns
$t_{sk(0)}$	skew	note 3		–	–	1.5	ns

Notes

1. Typical values are measured at V_{CCA} = 5.0 V and T_{amb} = 25 °C.
2. Typical values measured at V_{CCB} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS

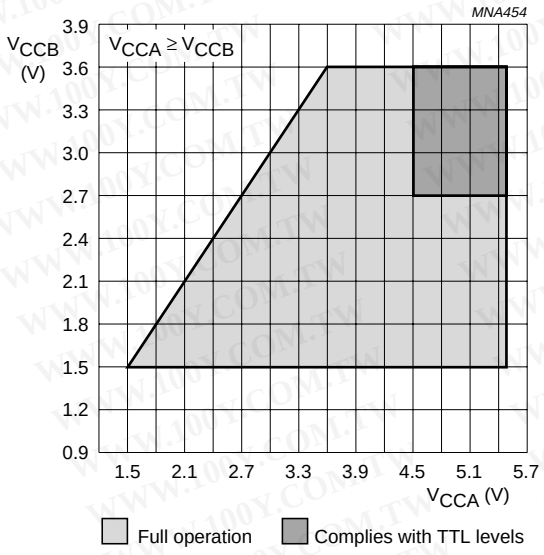
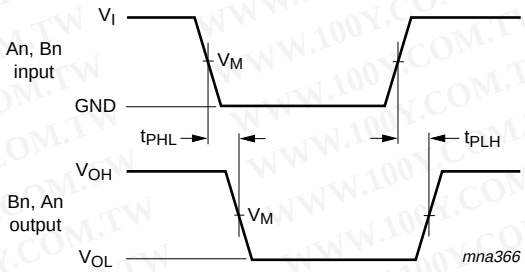
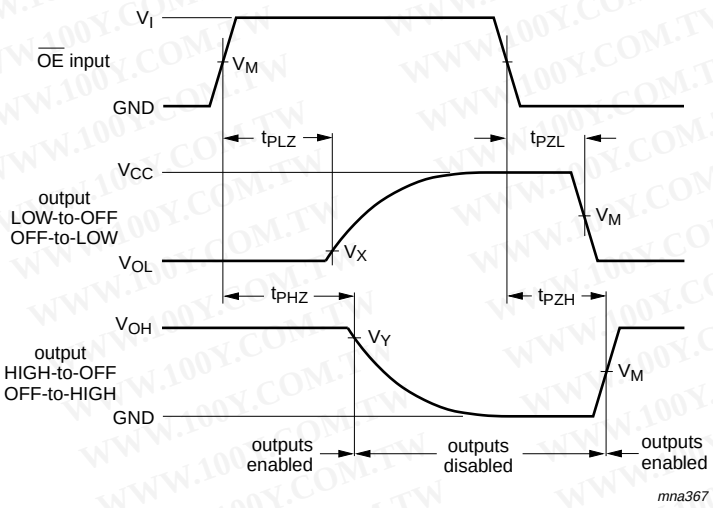


Fig.4 Supply operation area.



V_M = 1.5 V at 2.7 V ≤ V_{CCB} ≤ 3.6 V;
V_M = 0.5V_{CCA} at V_{CCA} ≥ 4.5 V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

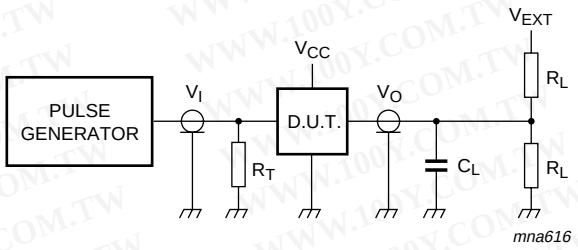
Fig.5 Input (An, Bn) to output (Bn, An) propagation delays.



V_M = 1.5 V at 2.7 V ≤ V_{CCB} ≤ 3.6 V;
V_M = 0.5V_{CCA} at V_{CCA} ≥ 4.5 V;
V_X = V_{OL} + 0.3 V at V_{CCB} ≥ 2.7 V;
V_Y = V_{OH} − 0.3 V at V_{CCB} ≥ 2.7 V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.



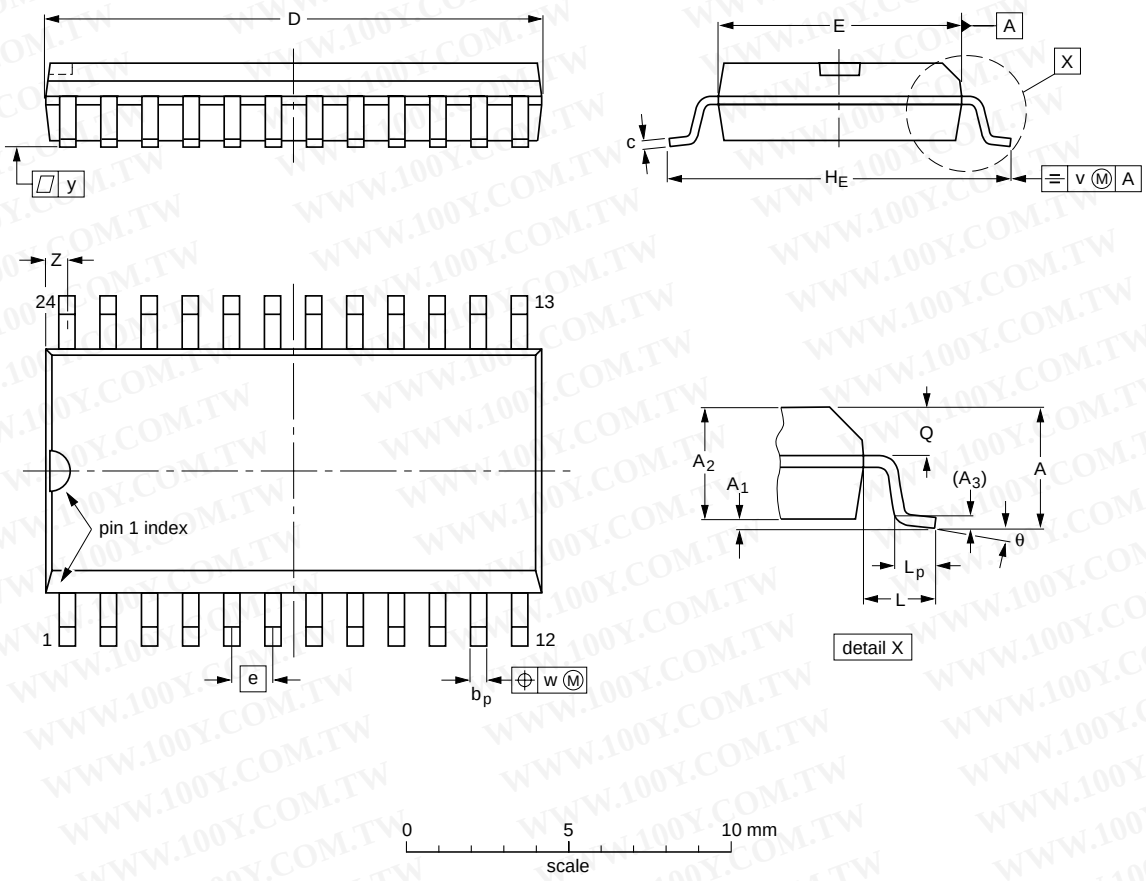
V_{CCA}	V_{CCB}	V_I	C_L	R_L	V_{EXT}		
					t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
< 2.7 V	< 2.7 V	V_{CC}	50 pF	500 Ω	open	GND	2 × V_{CC}
–	2.7 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V_{CC}
4.5 V to 5.5 V	–	3.0 V	50 pF	500 Ω	open	GND	2 × V_{CC}

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

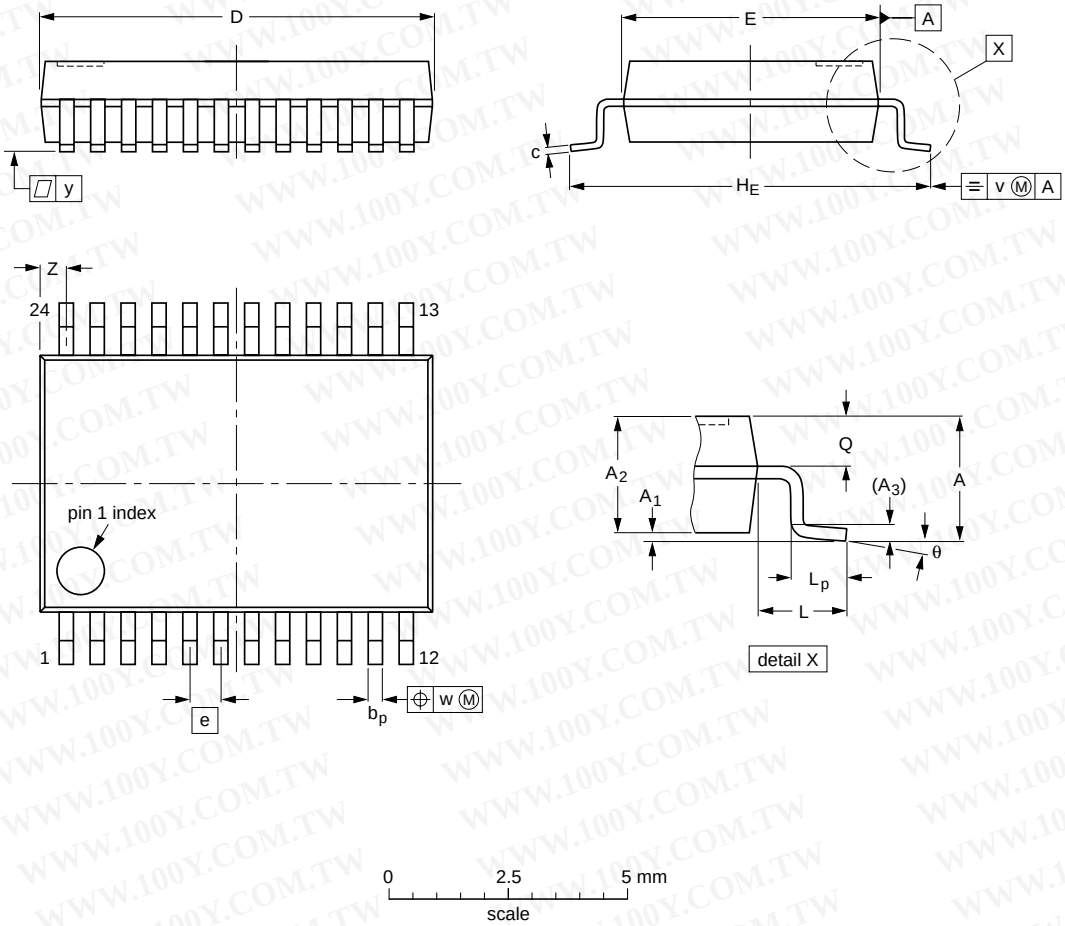
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

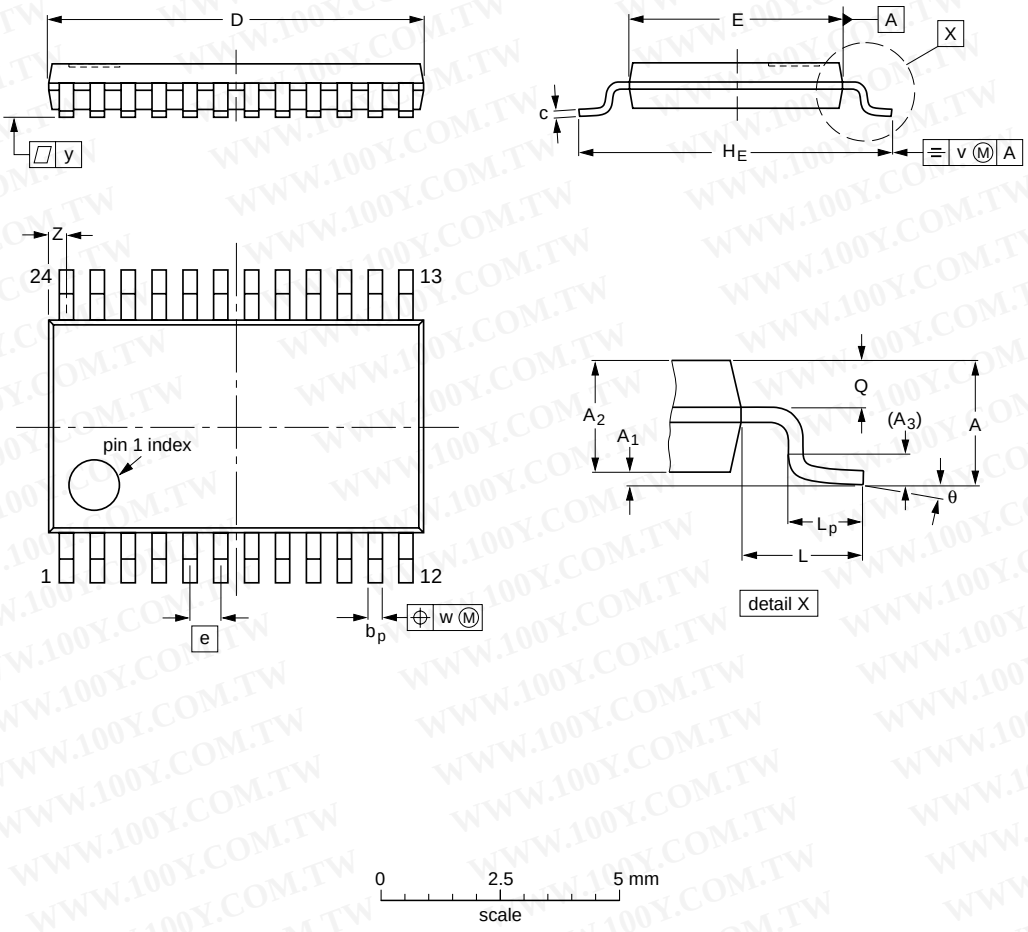
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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