Octal D-type transparent latch; 3-state 74LVC573

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC573 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '573' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '573' is functionally identical to the '373', but the '373' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF V_{CC} = 3.3 V	4.3 4.6	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC573D	20	SO	plastic	SO20/SOT163A
74LVC573DB	20	SSOP	plastic	SSOP20/SOT339
74LVC573PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

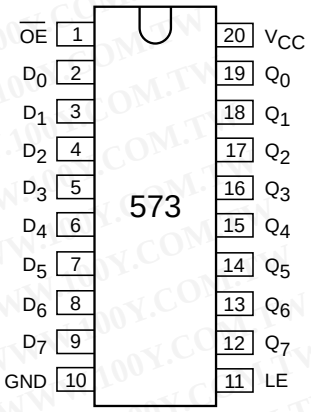


Fig.1 Pin configuration.

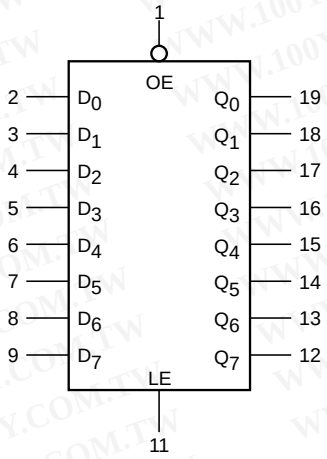


Fig.2 Logic symbol.

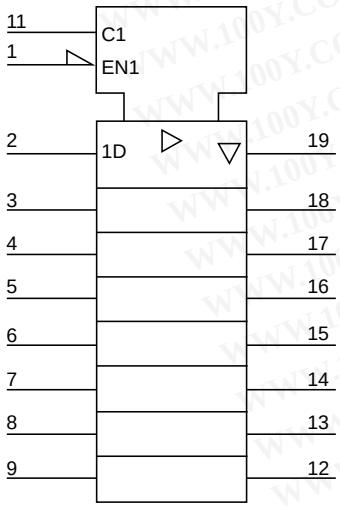


Fig3. IEC logic symbol.

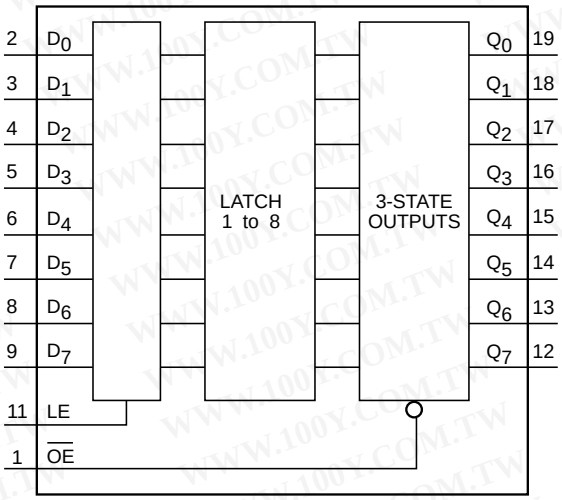


Fig.4 Functional diagram.

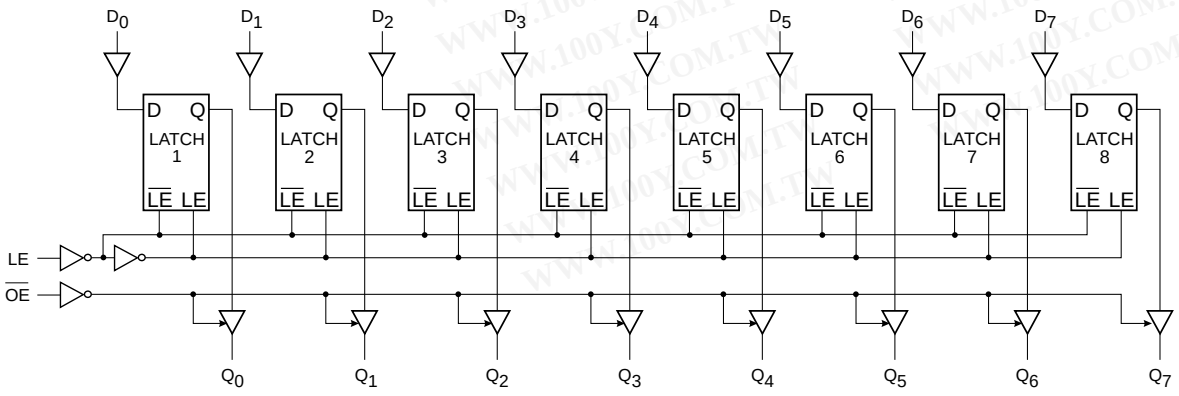


Fig.5 Logic diagram.

FAMILY DESCRIPTION

The LVC family comprises very fast low-power logic ICs fabricated in a sub-micron CMOS process.
LVC ICs with 3.3 V ±0.3 V supply operate at the same speed as FAST bipolar logic and consumes only a fraction of the power. The LVC family functions with supply voltages down to 2.7 V. The reduction from the conventional 5.0 V to 3.3 V reduces the output swing leading to a much lower dynamic power dissipation. Pin and function compatibility with FAST ensures an easy transfer of existing systems into new 3.3 V systems.

RECOMMENDED OPERATING CONDITIONS FOR THE LVC FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage (for max. speed performance)	2.7	3.6	V	
V_{CC}	DC supply voltage (for low-voltage applications)	1.2	3.6	V	
V_I	DC input voltage range	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC}	V	
V_O	DC output voltage range	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	0 0	20 10	ns/V	V_{CC} = 1.2 to 2.7 V V_{CC} = 2.7 to 3.6 V

LIMITING VALUES FOR THE LVC FAMILY (Note 1)

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+4.6	V	
I_{IK}	DC input diode current	−	−50	mA	V_I < 0
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	−	±50	mA	V_O > V_{CC} or V_O < 0
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	−	±50	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	−	±100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	− −	500 500	mW mW	above + 70°C derate linearly with 8 mW/K above + 60°C derate linearly with 5.5 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LVC FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CC} (V)	V_I	OTHER
V_{IH}	HIGH level input voltage	V_{CC} 2.0	− −	− −	V	1.2 2.7 to 3.6		
V_{IL}	LOW level input voltage	− −	− −	GND 0.8	V	1.2 2.7 to 3.6		
V_{OH}	HIGH level output voltage	V_{CC} − 0.5 V_{CC} − 0.2 V_{CC} − 0.6 V_{CC} − 1.0	− V_{CC} − −	− − − −	V	2.7 3.0 3.0 3.0	V_{IH} or V_{IL}	I_O = −12 mA I_O = −100 µA I_O = −12 mA I_O = −24 mA
V_{OL}	LOW level output voltage	− − −	− − −	0.40 0.20 0.55	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
I_I	input leakage current	−	±0.1	±5	µA	3.6	5.5 V or GND	not for I/O pins
I_{IHZ}/I_{ILZ}	input current for common I/O pins	−	±0.1	±15	µA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	−	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current	−	0.1	20	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin	−	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0

Note: All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LVC573

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC573

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	− 1.5 1.5	21 4.7 4.3*	− 8.0 7.8	ns	1.2 2.7 3.0 to 3.6	Figs 6, 10
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	− 1.5 1.5	23 5.3 4.6*	− 10 8.5	ns	1.2 2.7 3.0 to 3.6	Figs 7, 10
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	− 1.5 1.5	17 4.4 3.8*	− 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 8, 10
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	− 1.5 1.5	8.0 4.0 3.5*	− 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Figs 8, 10
t_W	LE pulse width HIGH	− −	3.0 3.0*	− −	ns	2.7 3.0 to 3.6	Fig.7
t_{su}	set-up time D_n to LE	1.0 1.0	0.2 0.2*	− −	ns	2.7 3.0 to 3.6	Fig.9
t_h	hold time D_n to LE	1.0 1.0	0 0*	− −	ns	2.7 3.0 to 3.6	Fig.9

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

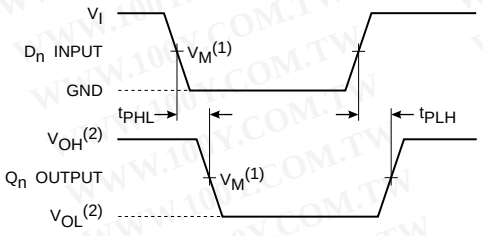


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

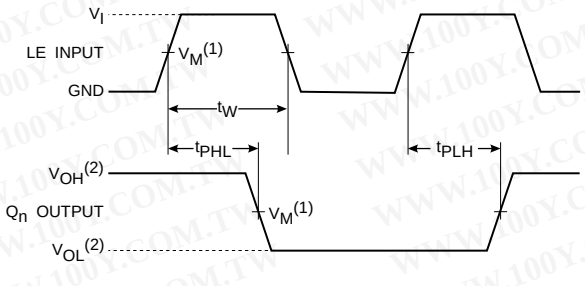


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

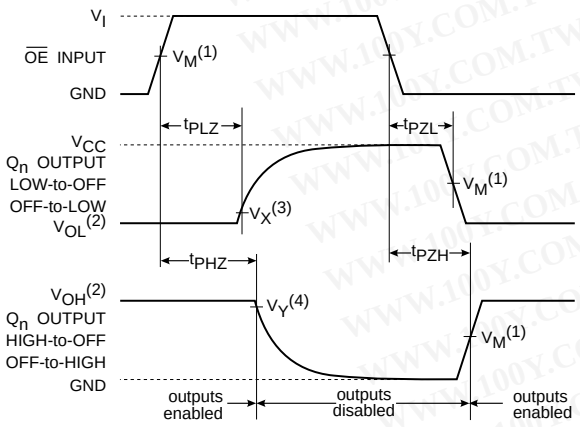


Fig.8 Waveforms showing the 3-state enable and disable times

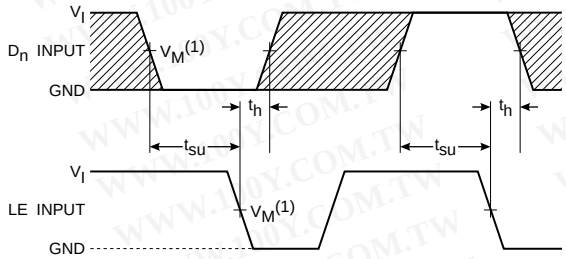
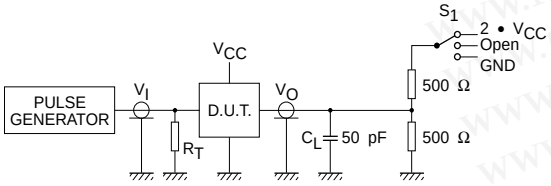


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

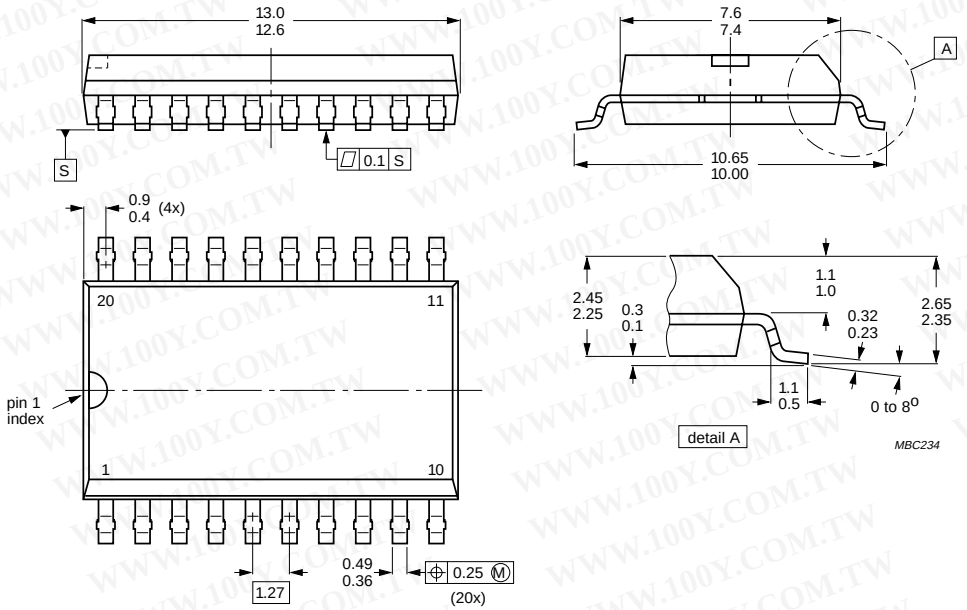


Fig.11 20-lead mini-pack; plastic (SO20/SOT163A).

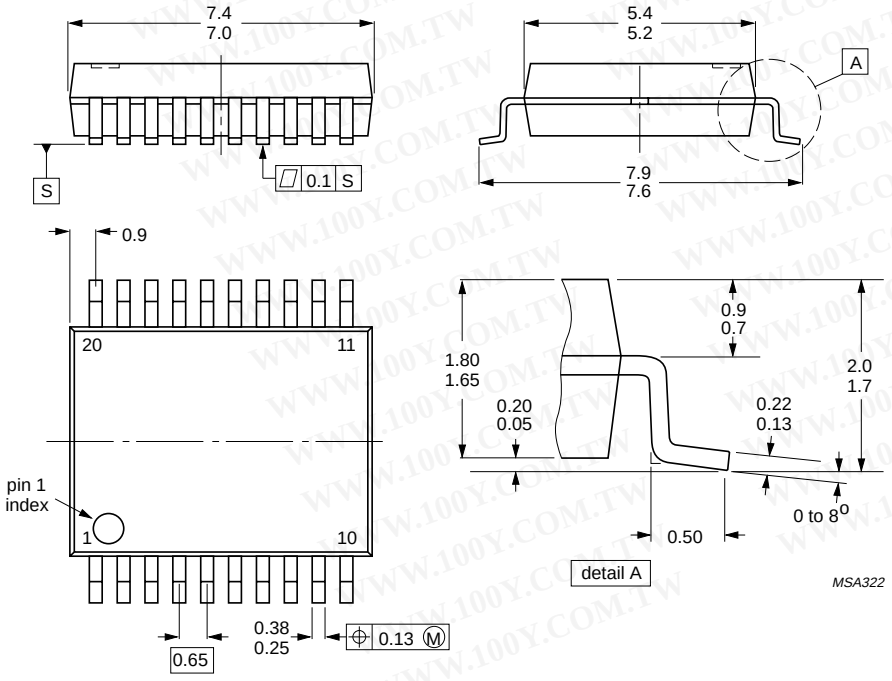


Fig.12 20-lead plastic medium-shrink SO (SSOP II 20; SOT339).

SOLDERING

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operating of the device at these or any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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