National Semiconductor

December 1996

74LVX161284
Low Voltage IEEE 161284 Transceiver

General Description

The 74LVX161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE P1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in an Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

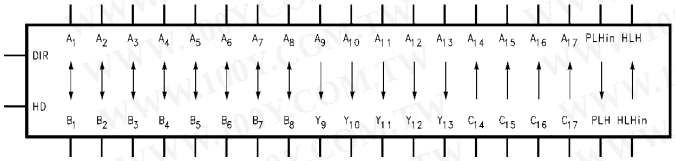
Outputs on the cable side can be configured to be either open drain or high drive (± 14 mA) and are connected to a separate power supply pin (V_{CC}—cable) to allow these outputs to be driven by a higher supply voltage than the A-side. The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, all inputs (except HLH) and outputs on the cable side contain internal pull-up resistors connected to the V_{CC}—cable supply to provide proper termination and pull-ups for open drain mode.

Outputs on the Peripheral side are standard low-drive CMOS outputs designed to interface with 3V logic. The DIR input controls data flow on the A_1–A_8/B_1–B_8 transceiver pins.

Features

- Supports IEEE P1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- Replaces the function of two (2) 74ACT1284 devices
- All inputs have hysteresis to provide noise margin
- B and Y output resistance optimized to drive external cable
- B and Y outputs in high impedance mode during power down
- Inputs and outputs on cable side have internal pull-up resistors
- Flow-through pin configuration allows easy interface between the Peripheral and Host

Logic Symbol

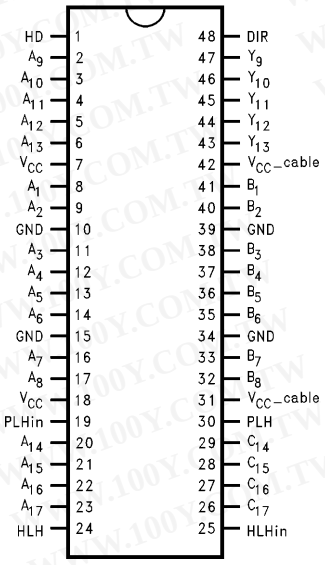


TL/F/12145–2

	SSOP JEDEC
Order Number	74LVX161284MEA 74LVX161284MEAX
See NS Package Number	MS48A

Connection Diagram

Pin Assignment for SSOP



TL/F/12145–1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

  RRD-B30M17/Printed in U. S. A.

Pin Descriptions

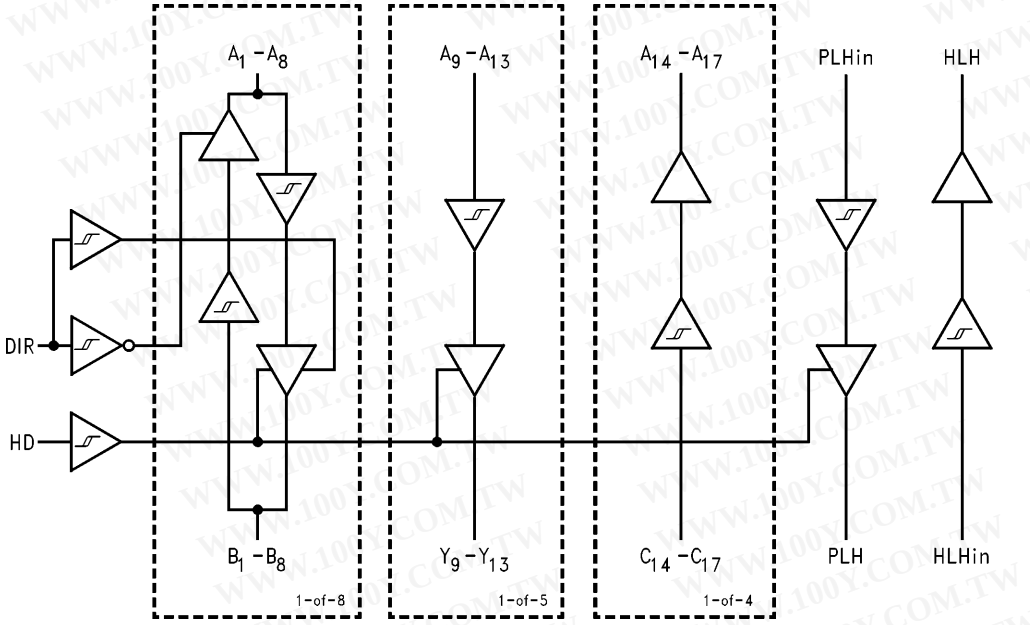
Pin Names	Description
HD	High Drive Enable Input (Active High)
DIR	Direction Control Input
A_1–A_8	Inputs or Outputs
B_1–B_8	Inputs or Outputs
A_9–A_{13}	Inputs
Y_9–Y_{13}	Outputs
A_{14}–A_{17}	Outputs
C_{14}–C_{17}	Inputs
PLH_{IN}	Peripheral Logic High Input
PLH	Peripheral Logic High Output
HLH_{IN}	Host Logic High Input
HLH	Host Logic High Output

Truth Table

Inputs		Outputs
DIR	HD	
L	L	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13}* C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
L	H	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}
H	L	A_1–A_8 Data to B_1–B_8** A_9–A_{13} Data to Y_9–Y_{13}* C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
H	H	A_1–A_8 Data to B_1–B_8 A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}

Note: *Y_9–Y_{13} Open Drain Outputs
**B_1–B_8 Open Drain Outputs

Logic Diagram



TL/F/12145–3

Absolute Maximum Ratings (Note 1)

Supply Voltage
- V_{CC} −0.5V to +5.5V
- $V_{CC—Cable}$ −0.5V to +7.0V
- $V_{CC—Cable}$ Must Be ≥ V_{CC}

Input Voltage (V_I)—(Note 2)
- A_1–A_{13}, PLH_{IN}, DIR, HD −0.5V to V_{CC} + 0.5V
- B_1–B_8, C_{14}–C_{17}, HLH_{IN} −0.5V to +5.5V (DC)
- B_1–B_8, C_{14}–C_{17}, HLH_{IN} −2.0V to +7.0V*
  *40 ns Transient

Output Voltage (V_O)
- A_1–A_8, A_{14}–A_{17}, HLH −0.5V to V_{CC} +0.5V
- B_1–B_8, Y_9–Y_{13}, PLH −0.5V to +5.5V (DC)
- B_1–B_8, Y_9–Y_{13}, PLH −2.0V to +7.0V*
  *40 ns Transient

DC Output Current (I_O)
- A_1–A_8, HLH ±25 mA
- B_1–B_8, Y_9–Y_{13} ±50 mA
- PLH (Output LOW) 84 mA
- PLH (Output HIGH) −50 mA

Input Diode Current (I_{IK})—(Note 2)
- DIR, HD, A_9–A_{13}, PLH, HLH, C_{14}–C_{17} −20 mA

Output Diode Current (I_{OK})
- A_1–A_8, A_{14}–A_{17}, HLH ±50 mA
- B_1–B_8, Y_9–Y_{13}, PLH −50 mA

DC Continuous V_{CC} or Ground Current ±200 mA

Storage Temperature −65°C to +150°C

ESD (HBM) Last Passing Voltage 2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. National does not recommend operation outside the databook specifications.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Supply Voltage
- V_{CC} 3.0V to 3.6V
- $V_{CC—Cable}$ 3.0V to 5.5V

DC Input Voltage (V_I) 0V to V_{CC}

Open Drain Voltage (V_O) 0V to 5.5V

Operating Temperature (T_A) −40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$V_{CC—Cable}$ (V)	74LVX161284 T_A = 0°C to +70°C	74LVX161284 T_A = −40°C to +85°C	Units	Conditions
					Guaranteed Limits			
V_{IK}	Input Clamp Diode Voltage		3.0	3.0	−1.2	−1.2	V	I_i = −18 mA
V_{IH}	Minimum High Level Input Voltage	A_n, B_n, PLH_{IN}, DIR, HD	3.0–3.6	3.0–5.5	2.0	2.0	V	V_T(Pos) ≥ 2.0V V_T(Pos) ≥ 2.4V
		C_n	3.0–3.6	3.0–5.5	2.3	2.3		
		HLH_{IN}	3.0–3.6	3.0–5.5	2.6	2.6		
V_{IL}	Maximum High Level Input Voltage	A_n, B_n, PLH_{IN}, DIR, HD	3.0–3.6	3.0–5.5	0.8	0.8	V	V_T(Neg) ≤ 1.2V V_T(Neg) ≤ 1.9V
		C_n	3.0–3.6	3.0–5.5	0.8	0.8		
		HLH_{IN}	3.0–3.6	3.0–5.5	1.6	1.6		
ΔV_T	Minimum Input Hysteresis	A_n, B_n, PLH_{IN} DIR, HD	3.3	3.0–5.5	0.4	0.4	V	$V_T^+ - V_T^-$ $V_T^+ - V_T^-$
		C_n	3.0–3.6	3.0–5.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	A_n, HLH	3.0 3.0	3.0 3.0	2.8 2.4	2.8 2.4	V	I_{OH} = −50 μA I_{OH} = −4 mA
		B_n, Y_n	3.0	3.0	2.23	2.23	V	I_{OH} = −14 mA I_{OH} = −500 μA
		PLH	3.15	3.15	3.1	3.1		
V_{OL}	Maximum Low Level Output Voltage	A_n, HLH	3.0 3.0	3.0 3.0	0.2 0.4	0.2 0.4	V	I_{OL} = 50 μA I_{OL} = 4 mA
		B_n, Y_n	3.0	3.0	0.77	0.77	V	I_{OL} = 14 mA I_{OL} = 84 mA
		PLH	3.0	3.0	0.8	0.9		
RD	Maximum Output Impedance	B_1–B_8, Y_9–Y_{13}	3.3 3.3	3.3 5.0	55 55	55 55	Ω	(Notes 1, 2, 4)
	Minimum Output Impedance	B_1–B_8, Y_9–Y_{13}	3.3 3.3	3.3 5.0	35 35	35 35	Ω	(Notes 1, 2, 4)

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$V_{CC—Cable}$ (V)	74LVX161284 $T_A = 0°C$ to $+70°C$ Guaranteed Limits	74LVX161284 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
R_P	Maximum Pull-Up Resistance	$B_1–B_8$, $Y_9–Y_{13}$, $C_{14}–C_{17}$	3.3 3.3	3.3 5.0	1650 1650	1650 1650	Ω	(Note 2)
	Minimum Pull-Up Resistance	$B_1–B_8$, $Y_9–Y_{13}$ $C_{14}–C_{17}$	3.3 3.3	3.3 5.0	1150 1150	1150 1150	Ω	(Note 2)
I_{IH}	Maximum Input Current in High State	$A_9–A_{13}$, PLH_{IN}, HD, DIR, HLH_{IN}	3.6	3.6	1.0	1.0	μA	$V_I = 3.6V$
		$C_{14}–C_{17}$	3.6	3.6	50.0	50.0	μA	$V_I = 3.6V$
		$C_{14}–C_{17}$	3.6	5.5	100	100	μA	$V_I = 5.5V$
I_{IL}	Maximum Input Current in Low State	$A_9–A_{13}$, PLH_{IN}, HD, DIR, HLH_{IN}	3.6	3.6	−1.0	−1.0	μA	$V_I = 0.0V$
		$C_{14}–C_{17}$	3.6	3.6	−3.5	−3.5	mA	$V_I = 0.0V$
		$C_{14}–C_{17}$	3,6	5.5	−5.0	−5.0	mA	$V_I = 0.0V$
I_{OZH}	Maximum Output Disable Current (High)	$A_1–A_8$	3.6	3.6	20	20	μA	$V_O = 3.6V$
		$B_1–B_8$	3.6	3.6	50	50	μA	$V_O = 3.6V$
		$B_1–B_8$	3.6	5.5	100	100	μA	$V_O = 5.5V$
I_{OZL}	Maximum Output Disable Current (Low)	$A_1–A_8$	3.6	3.6	−20	−20	μA	$V_O = 0.0V$
		$B_1–B_8$	3.6	3.6	−3.5	−3.5	mA	
		$B_1–B_8$	3.6	5.5	−5.0	−5.0	mA	
I_{OFF}	Power Down Output Leakage	$B_1–B_8$, $Y_9–Y_{13}$, PLH	0.0	0.0	100	100	μA	$V_O = 5.5V$
I_{OFF}	Power Down Input Leakage	$C_{14}–C_{17}$, HLH_{IN}	0.0	0.0	100	100	μA	$V_I = 5.5V$
$I_{OFF—ICC}$	PowerDown Leakage to V_{CC}		0.0	0.0	250	250	μA	(Note 3)
$I_{OFF—ICC2}$	Power Down Leakage to $V_{CC—Cable}$		0.0	0.0	250	250	μA	(Note 3)
I_{CC}	Maximum Supply Current		3.6 3.6	3.6 5.5	45 70	45 70	mA mA	$V_I = V_{CC}$ or GND $V_I = V_{CC}$ or GND

Note 1: Output impedance is measured with the output active low and active high (HD = high).

Note 2: Resistance is calculated using the following formula:

$$\text{Resistance} = \frac{1V}{(\text{Current at 2V on pin}) - (\text{Current at 1V on pin})}$$

Note 3: Power-down leakage to V_{CC} or $V_{CC—Cable}$ is tested by simultaneously forcing all pins on the cable-side ($B_1–B_8$, $Y_9–Y_{13}$, PLH, $C_{14}–C_{17}$ and HLH_{IN}) to 5.5V and measuring the resulting I_{CC} or $I_{CC—Cable}$.

Note 4: This parameter is guaranteed but not tested, characterized only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = 3.0V–3.6V$, $V_{CC—Cable} = 3.0V–5.5V$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 3.0V–3.6V$, $V_{CC—Cable} = 3.0V–5.5V$		Units	Fig. No.
		Min	Max	Min	Max		
t_{PHL}	$A_1–A_8$ to $B_1–B_8$	2.0	40.0	2.0	44.0	ns	1
t_{PLH}	$A_1–A_8$ to $B_1–B_8$	2.0	40.0	2.0	44.0	ns	2
t_{PHL}	$B_1–B_8$ to $A_1–A_8$	2.0	40.0	2.0	44.0	ns	3
t_{PLH}	$B_1–B_8$ to $A_1–A_8$	2.0	40.0	2.0	44.0	ns	3
t_{PHL}	$A_9–A_{13}$ to $Y_9–Y_{13}$	2.0	40.0	2.0	44.0	ns	1
t_{PLH}	$A_9–A_{13}$ to $Y_9–Y_{13}$	2.0	40.0	2.0	44.0	ns	2

AC Electrical Characteristics (Continued)

Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = 3.0V–3.6V$, $V_{CC—Cable} = 3.0V–5.5V$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 3.0V–3.6V$, $V_{CC—Cable} = 3.0V–5.5V$		Units	Fig. No.
		Min	Max	Min	Max		
t_{PHL}	$C_{14}–C_{17}$ to $A_{14}–A_{17}$	2.0	40.0	2.0	44.0	ns	3
t_{PLH}	$C_{14}–C_{17}$ to $A_{14}–A_{17}$	2.0	40.0	2.0	44.0	ns	3
t_{SKEW}	LH-LH or HL-HL		10.0		12.0	ns	(Note 1)
t_{PHL}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	1
t_{PLH}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	2
t_{PHL}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	3
t_{PLH}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	3
t_{PHZ} t_{PLZ}	Output Disable Time DIR to $A_1–A_8$	2.0 2.0	15.0 15.0	2.0 2.0	18.0 18.0	ns	7
t_{PZH} t_{PZL}	Output Enable Time DIR to $A_1–A_8$	2.0 2.0	50.0 50.0	2.0 2.0	50.0 50.0	ns	8
t_{PHZ} t_{PLZ}	Output Disable Time DIR to $B_1–B_8$	2.0 2.0	50.0 50.0	2.0 2.0	50.0 50.0	ns	9
t_{pEN}	Output Enable Time HD to $B_1–B_8$, $Y_9–Y_{13}$	2.0 2.0	25.0 25.0	2.0 2.0	28.0 28.0	ns	2
t_{pDis}	Output Disable Time HD to $B_1–B_8$, $Y_9–Y_{13}$	2.0 2.0	25.0 25.0	2.0 2.0	28.0 28.0	ns	2
$t_{pEn}–t_{pDis}$	Output Enable- Output Disable		10.0		12.0	ns	
t_{SLEW} t_{PLH} t_{PHL}	Output Slew Rate $B_1–B_8$, $Y_9–Y_{13}$	 0.05 0.05	 0.40 0.40	 0.05 0.05	 0.40 0.40	V/ns	 5 4
t_r, t_f	t_{RISE} and t_{FALL} $B_1–B_8$*, $Y_9–Y_{13}$*		120 120		120 120	ns	6 (Note 2)

*Open Drain

Note 1: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type:

(i) $A_1–A_8$ to $B_1–B_8$, $A_9–Y_{13}$ to $Y_9–Y_{13}$

(ii) $B_1–B_8$ to $A_1–A_8$

(iii) $C_{14}–C_{17}$ to $A_{14}–A_{17}$

Note 2: This parameter is guaranteed but not tested, characterized only.

Note: Pulse Generator for all pulses; Rate $\leq$1.0 MHz; $Z_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0.0V$ (HD, DIR, $A_9–A_{13}$, $C_{14}–C_{17}$, PLH_{IN} and HLH_{IN})
$C_{I/O}$ (Note)	I/O Pin Capacitance	12	pF	$V_{CC} = 3.3V$

Note: $C_{I/O}$ is measured at frequency = 1 MHz, per MIL-STD-883B, Method 3012

AC Loading and Waveforms

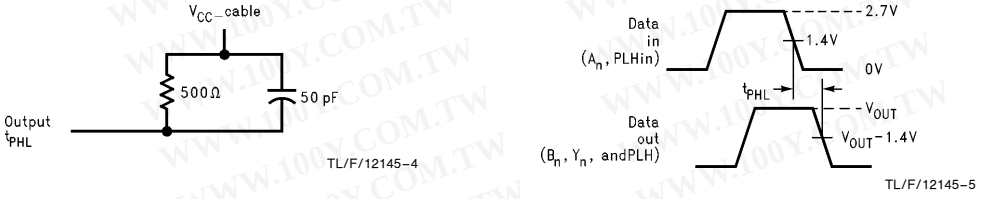
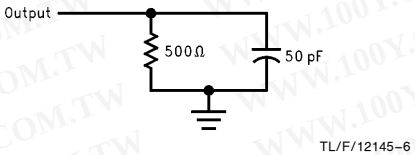
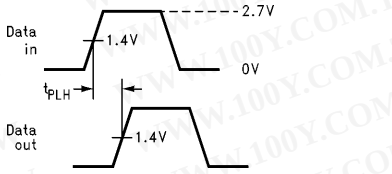


FIGURE 1. t_{PHL} Test Load and Waveforms
$A_1–A_8$ to $B_1–B_8$
$A_9–A_{13}$ to $Y_9–Y_{13}$
PLHin to PLH

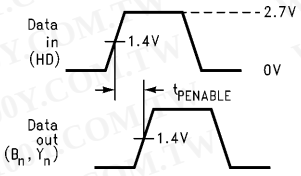
AC Loading and Waveforms (Continued)



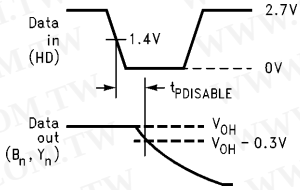
TL/F/12145–6



TL/F/12145–7

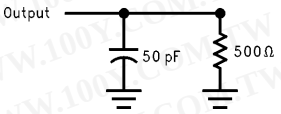


TL/F/12145–8

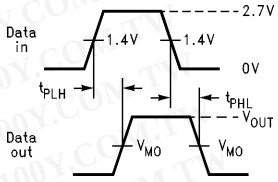


TL/F/12145–9

FIGURE 2. t_{PLH}, t_{pEn}, t_{pDis} Test Load and Waveforms
A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}
PLHin to PLH, HD to B_1–B_8, Y_9–Y_{13}, PLH



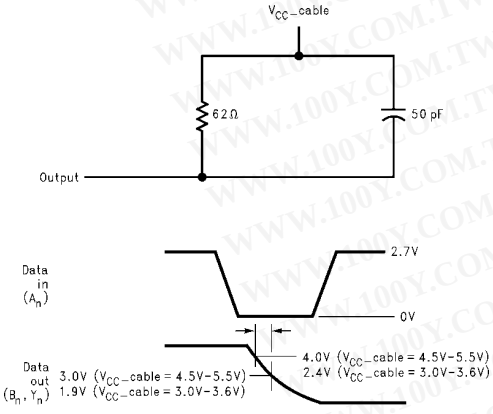
TL/F/12145–10



TL/F/12145–11

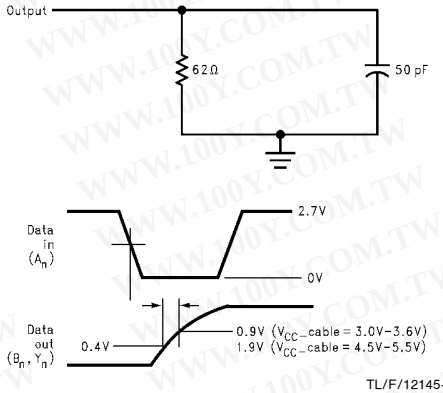
V_{MO} = 50% V_{CC}

FIGURE 3. t_{PHL}, t_{PLH} Test Load and Waveforms
B_1–B_8 to A_1–A_8, C_{14}–C_{17} to A_{14}–A_{17}, HLHin to HLH



TL/F/12145–14

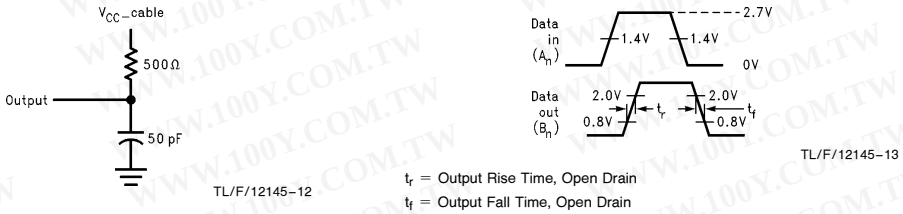
FIGURE 4. t_{SLEW} HL Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}



TL/F/12145–15

FIGURE 5. t_{SLEW} LH Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}

AC Loading and Waveforms (Continued)



t_r = Output Rise Time, Open Drain
t_f = Output Fall Time, Open Drain

FIGURE 6. t_{RISE} and t_{FALL} Test Load and Waveforms for Open Drain Outputs A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}

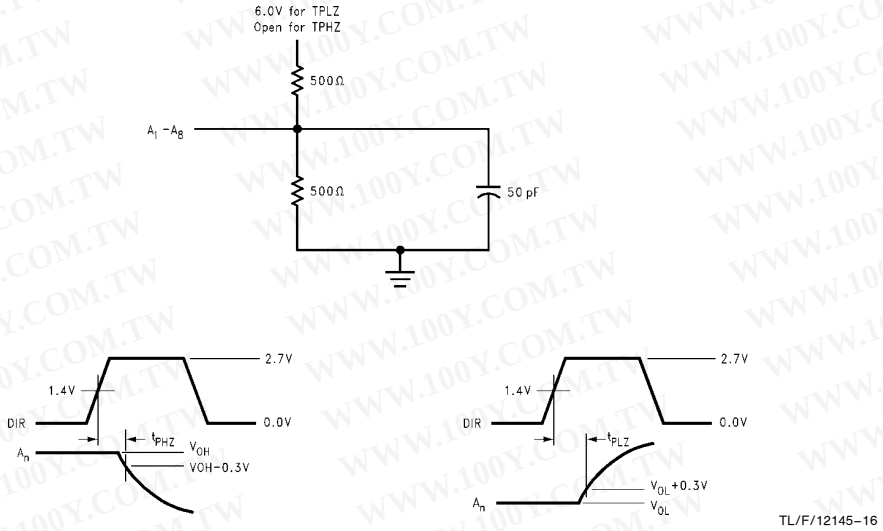


FIGURE 7. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to A_1–A_8

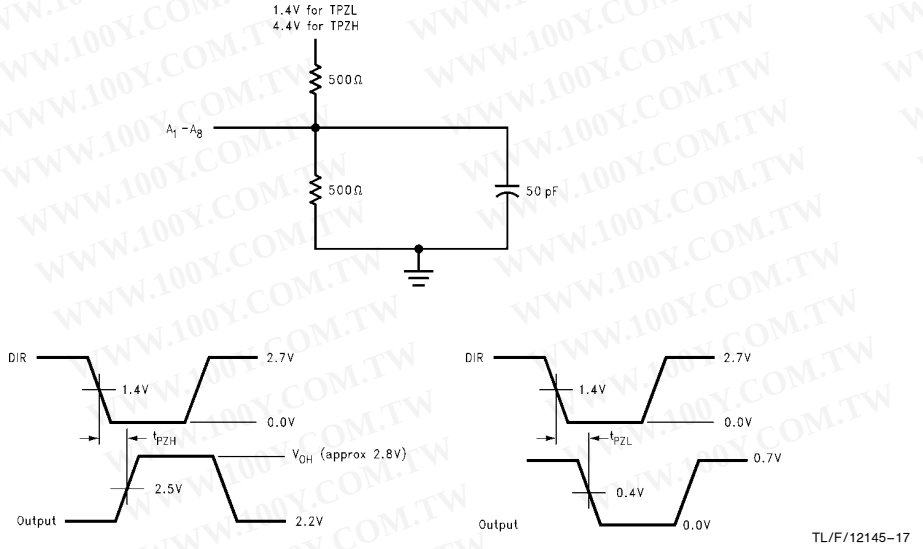
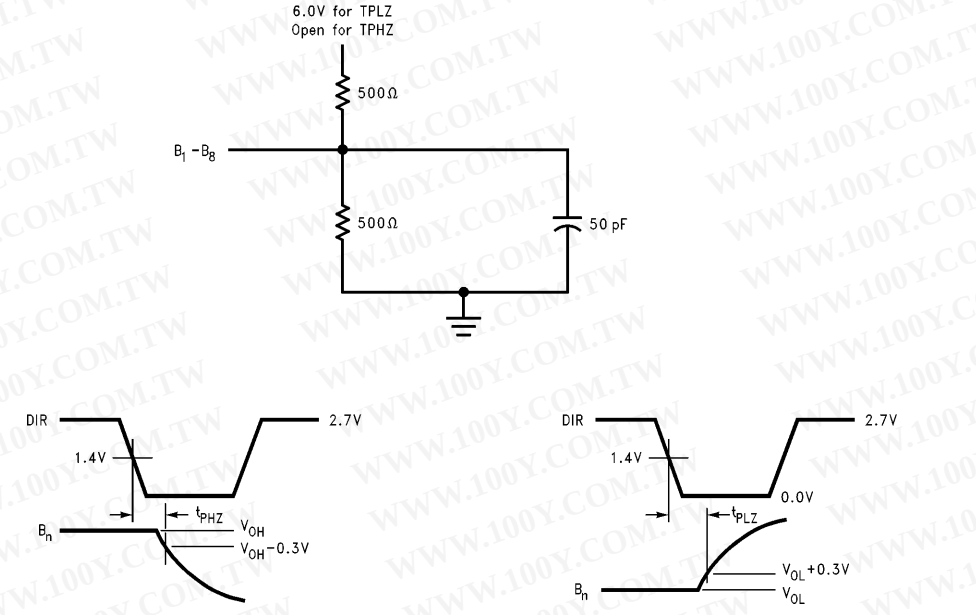


FIGURE 8. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to to A_1–A_8

AC Loading and Waveforms (Continued)

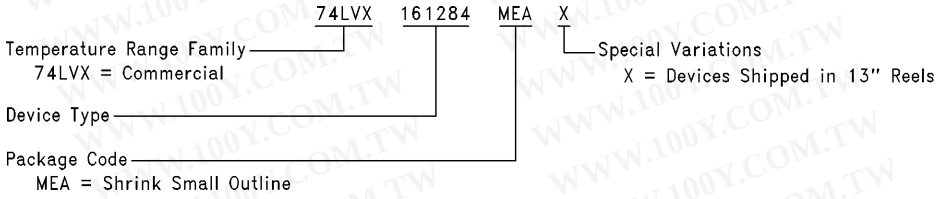


TL/F/12145–18

FIGURE 9. t_{PHZ} and t_{PLZ} Test Load and Waveforms DIR to to B_1–B_8

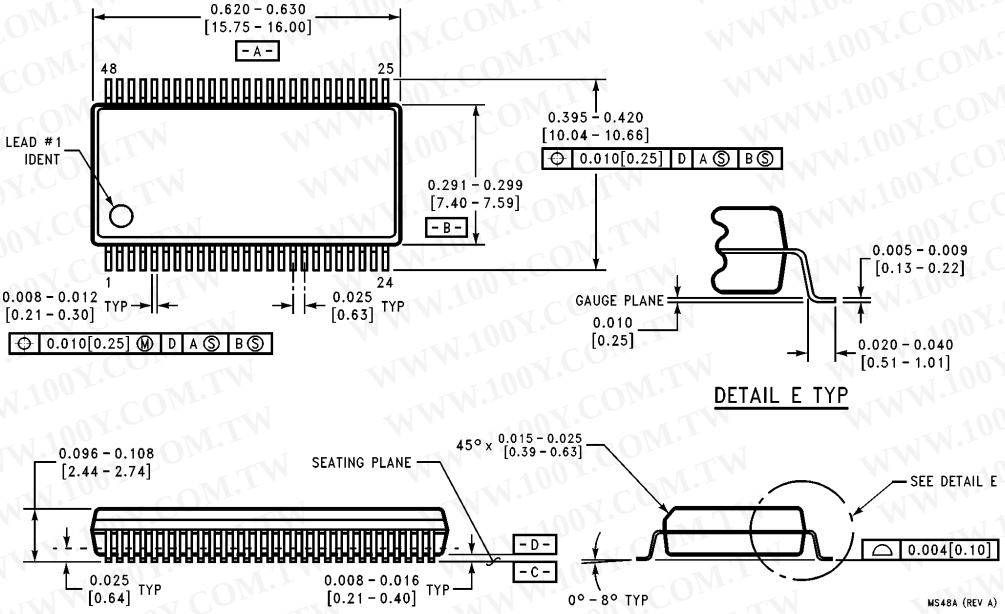
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12145–19

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead (0.300″ Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS48A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.