FAIRCHILD
SEMICONDUCTOR™

November 1992
Revised April 1999

74VHC04
Hex Inverter

General Description

The VHC04 is an advanced high speed CMOS Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This cir-

cuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 3.8 ns (typ) at V_{CC} = 5V
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (Min)
- Power down protection is provided on all inputs
- Low Noise: V_{OLP} = 0.4V (typ)
- Low power dissipation: I_{CC} = 2 μA (Max) @ T_A = 25°C
- Pin and function compatible with 74HC04

Ordering Code:

Order Number	Package Number	Package Description
74VHC04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
74VHC04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
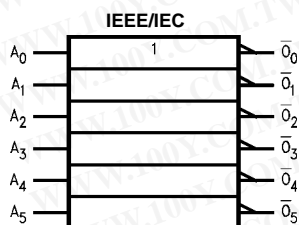
Connection Diagram
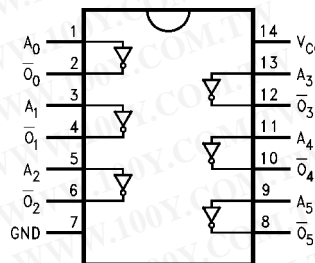
Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	$\overline{O}$
L	H
H	L

74VHC04

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions	
V_{IH}	HIGH Level	2.0	1.50			1.50		V		
	Input Voltage	3.0 − 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level	2.0			0.50		0.50	V		
	Input Voltage	3.0 − 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9			V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
	Output Voltage	3.0	2.9	3.0		2.9		V		
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level	2.0		0.0	0.1		0.1		V_{IN} = V_{IH} or V_{IL}	I_{OL} = +50 µA
	Output Voltage	3.0		0.0	0.1		0.1	V		
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 − 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	µA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = 25°C Limits	Units	Conditions
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.4	0.8	V	C_L = 50 pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.4	−0.8	V	C_L = 50 pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

| Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PHL}	Propagation Delay	3.3 ± 0.3		5.0	7.1	1.0	8.5	ns	$C_L = 15$ pF
t_{PLH}				7.5	10.6	1.0	12.0		$C_L = 50$ pF
		5.0 ± 0.5		3.8	5.5	1.0	6.5	ns	$C_L = 15$ pF
				5.3	7.5	1.0	8.5		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	$V_{CC} = $ OPEN
C_{PD}	Power Dissipation Capacitance			18				pF	(Note 4)

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) $= C_{PD} * V_{CC} * f_{IN} + I_{CC}/6$ (per gate).

74VHC04

Physical Dimensions inches (millimeters) unless otherwise noted
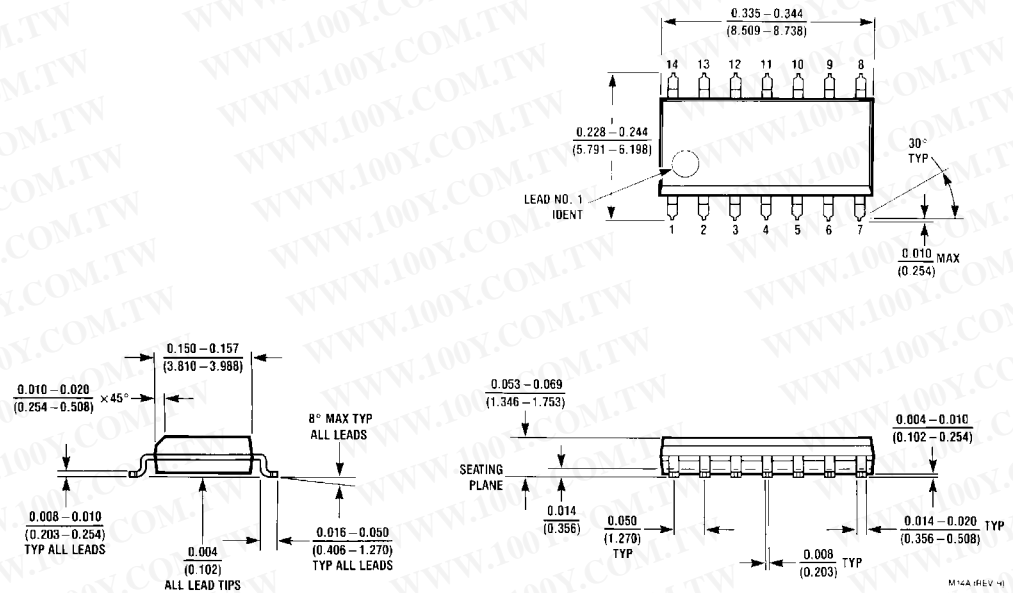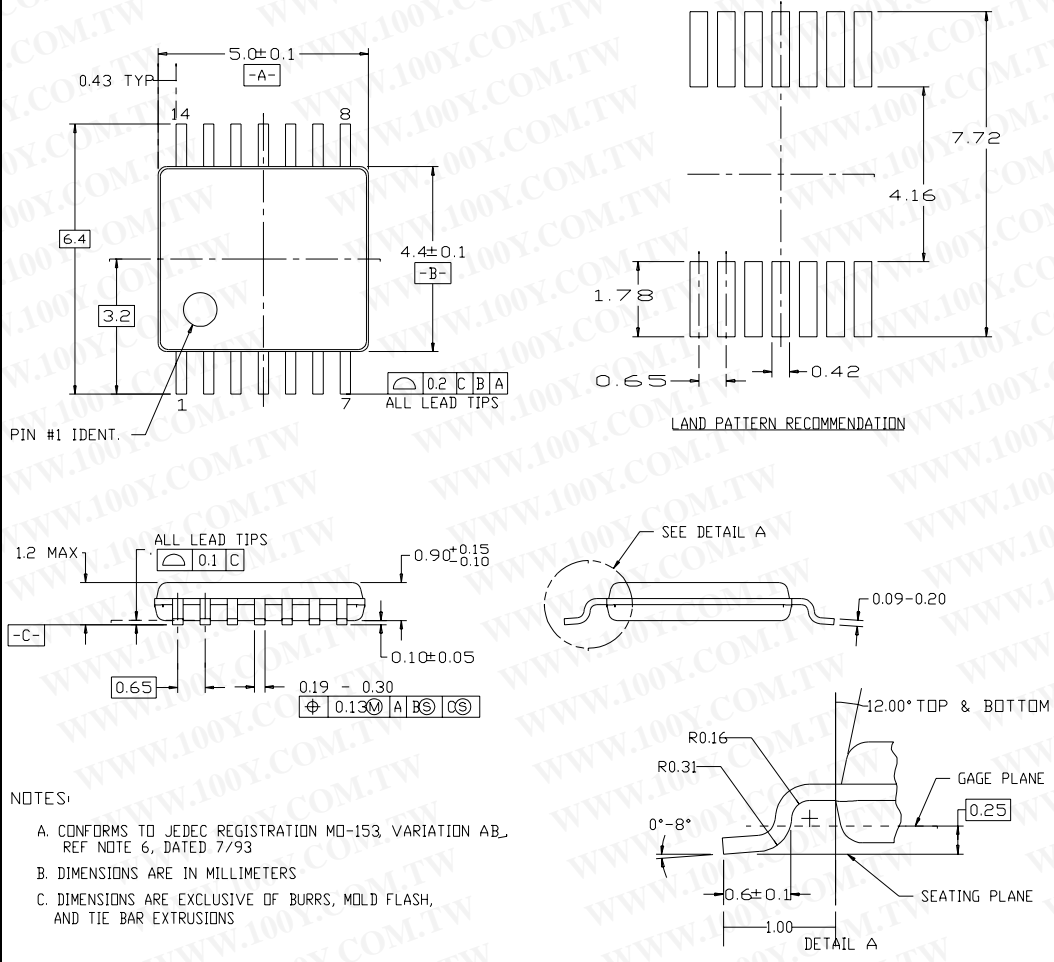

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A
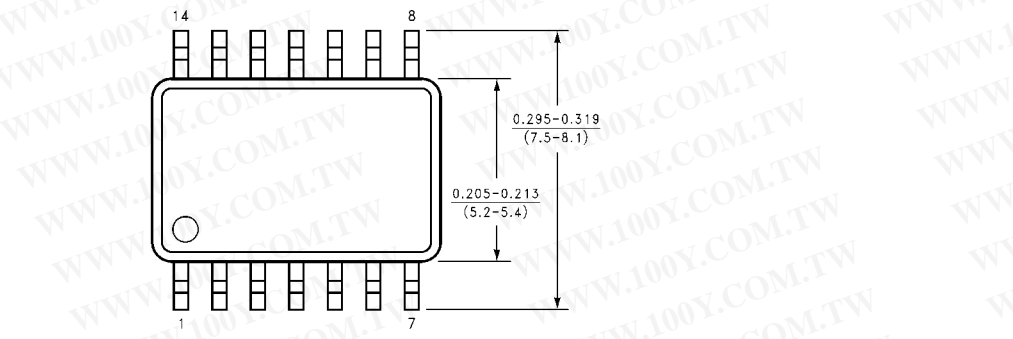
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


LAND PATTERN RECOMMENDATION

SEE DETAIL A

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

5

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
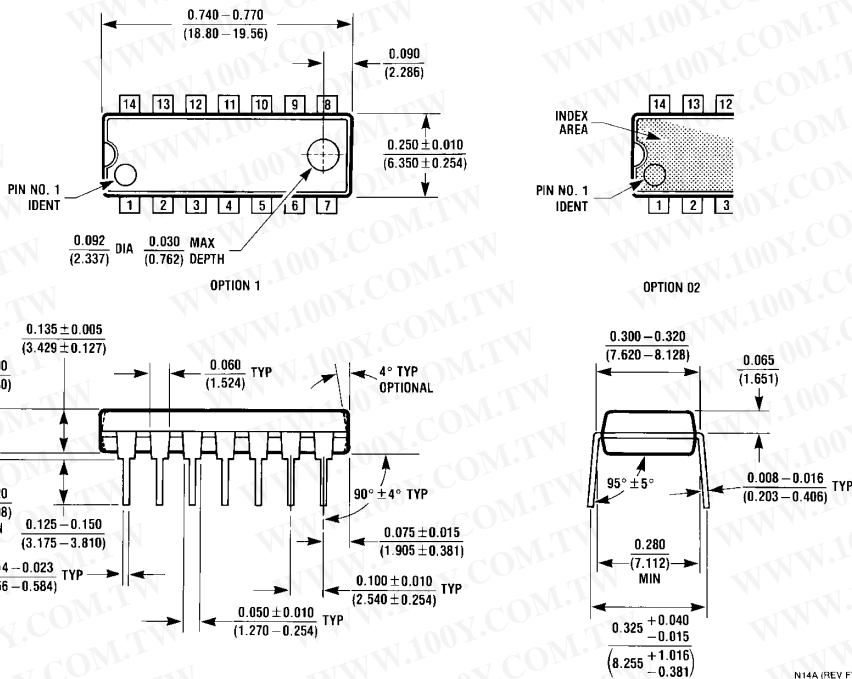
14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.