

74VHC273 Octal D Flip-Flop

General Description

The VHC273 is an advanced high speed CMOS Octal D-type flip-flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The register has a common buffered Clock (CP) which is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The Master Reset (MR) input will clear all flip-flops simultaneously. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input.

An input protection circuit insures that 0V to 7V can be applied to the inputs pins without regard to the supply voltage.

This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

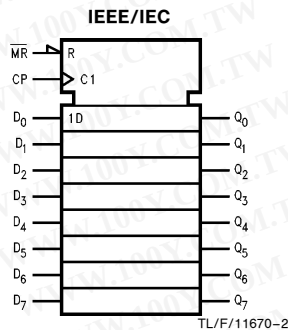
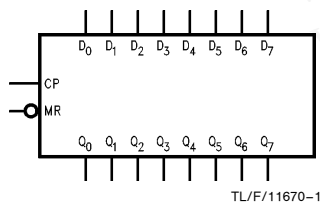
Features

- Low power dissipation:
 $I_{CC} = 4 \mu A$ (max) at $T_A = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Low noise: $VOLP = 0.9V$ (max)
- Pin and function compatible with 74HC273

Commercial	Package Number	Package Description
74VHC273M	M20B	20-Lead Molded JEDEC SOIC
74VHC273SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC273MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHC273N	N20A	20-Lead Molded DIP
74VHC273MSC	MSC20	20-Lead Molded EIAJ Type I SSOP

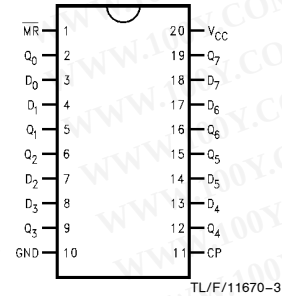
Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram

Pin Assignment for DIP, SSOP
TSSOP and SOIC



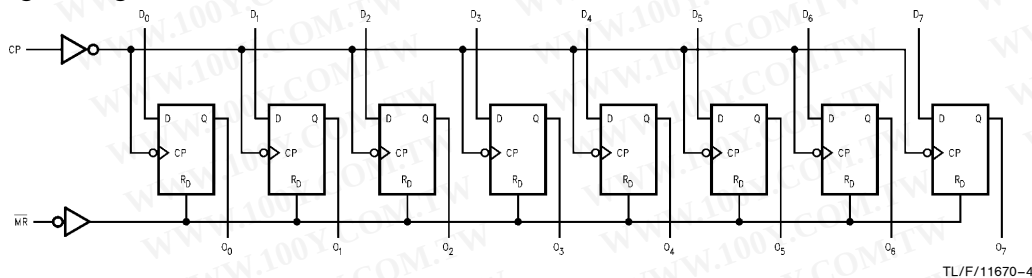
Pin Names	Description
D ₀ -D ₇	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↘	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$
Input Diode Current (I_{IK})	-20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC} /GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	$V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$ 0 ~ 100 ns/V 0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC				Units	Conditions		
			T _A = 25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min				Max
V _{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V _{CC}			1.50 0.7 V _{CC}		V		
V _{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V _{CC}		0.50 0.3 V _{CC}	V		
V _{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V _{IN} = V _{IH} or V _{IL} I _{OH} = −50 μA	
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V		
		3.0 4.5	2.58 3.94			2.48 3.80				
V _{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V		
		3.0 4.5		0.36 0.36			0.44 0.44			
I _{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V _{IN} = V _{CC} or GND	

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DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC T _A = 25°C		Units	Conditions
			Typ	Limits		
V _{OLP} *	Quiet Output Maximum Dynamic V _{OL}	5.0	0.6	0.9	V	C _L = 50 pF
V _{OLV} *	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.6	-0.9	V	C _L = 50 pF
V _{IHD} *	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C _L = 50 pF
V _{ILD} *	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C _L = 50 pF

*Parameter guaranteed by design.

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AC Electrical Characteristics for 'VHC

Symbol	Parameter	V _{CC} (V)	74VHC				Units	Conditions		
			T _A = 25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min				Max
f _{MAX}	Maximum Clock Frequency	3.3 ± 0.3	75	120		65	MHz		C _L = 15 pF	
			50	75		45			C _L = 50 pF	
		5.0 ± 0.5	120	165		100	MHz		C _L = 15 pF	
			80	110		70			C _L = 50 pF	
t _{PLH} , t _{PHL}	Propagation Delay Time (CK-Q)	3.3 ± 0.3		8.7	13.6	1.0	16.0	ns		C _L = 15 pF
				11.2	17.1	1.0	19.5			C _L = 50 pF
		5.0 ± 0.5		5.8	9.0	1.0	10.5	ns		C _L = 15 pF
				7.3	11.0	1.0	12.5			C _L = 50 pF
t _{PHL}	Propagation Delay Time (MR-Q)	3.3 ± 0.3		8.9	13.6	1.0	16.0	ns		C _L = 15 pF
				11.4	17.1	1.0	19.5			C _L = 50 pF
		5.0 ± 0.5		5.2	8.5	1.0	10.0	ns		C _L = 15 pF
				6.7	10.5	1.0	12.0			C _L = 50 pF
t _{OSLH} , t _{OSHL}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 1)	C _L = 50 pF
		5.0 ± 0.5			1.0		1.0			C _L = 50 pF
C _{IN}	Input Capacitance			4	10		10	pF	V _{CC} = Open	
C _{PD}	Power Dissipation Capacitance			31				pF	(Note 2)	

Note 1: Parameter guaranteed by design $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: $I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F). The total C_{PD} when n pieces of the Flip Flop operates can be calculated by the equation: $C_{PD}(total) = 22 + 9n$.

AC Operating Requirements for 'VHC

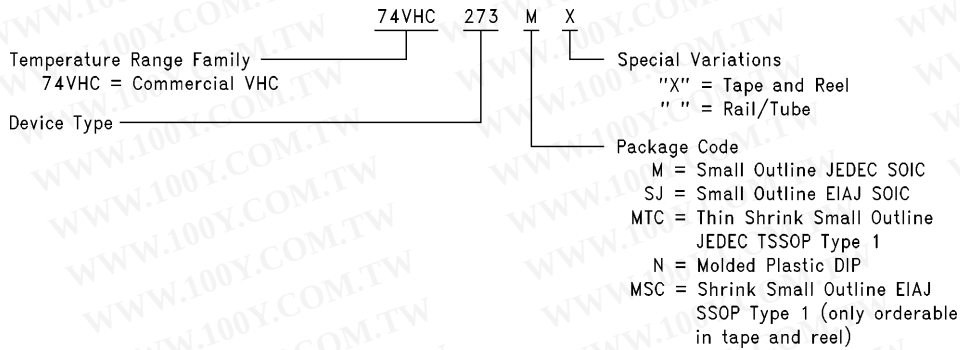
Symbol	Parameter	*V _{CC} (V)	74VHC			Units	Conditions
			T _A = 25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Minimum			
t _{W(L)} t _{W(H)}	Minimum Pulse Width (CK)	3.3 5.0		5.5 5.0	6.5 5.0	ns	
t _{W(L)}	Minimum Pulse Width (MR)	3.3 5.0		5.0 5.0	6.0 5.0	ns	
t _S	Minimum Setup Time	3.3 5.0		5.5 4.5	6.5 4.5	ns	
t _H	Minimum Hold Time	3.3 5.0		1.0 1.0	1.0 1.0	ns	
t _{rem}	Minimum Removal Time (MR)	3.3 5.0		2.5 2.0	2.5 2.0	ns	

*V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

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Ordering Information

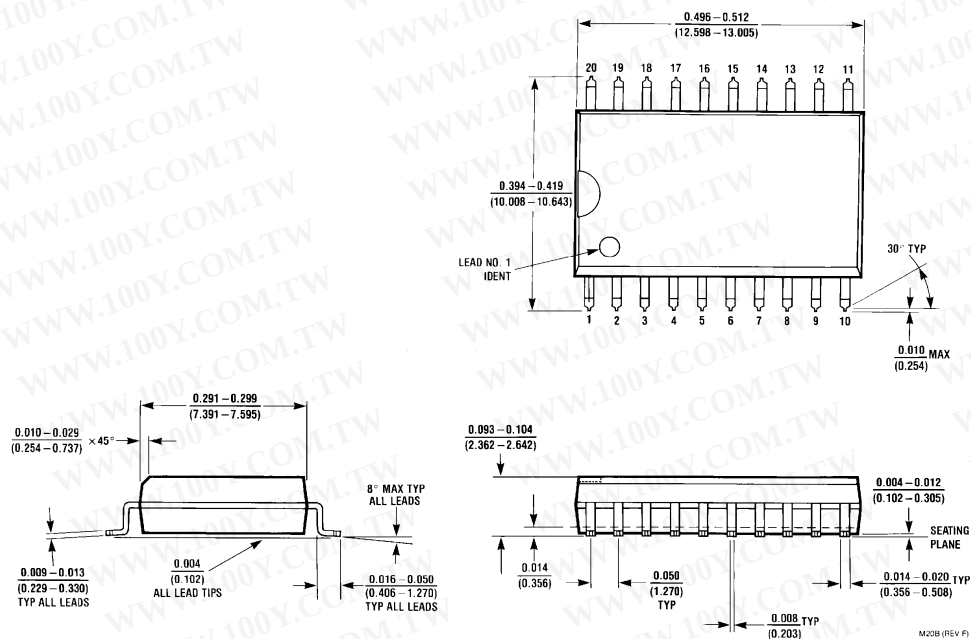
The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



TL/F/11670-5

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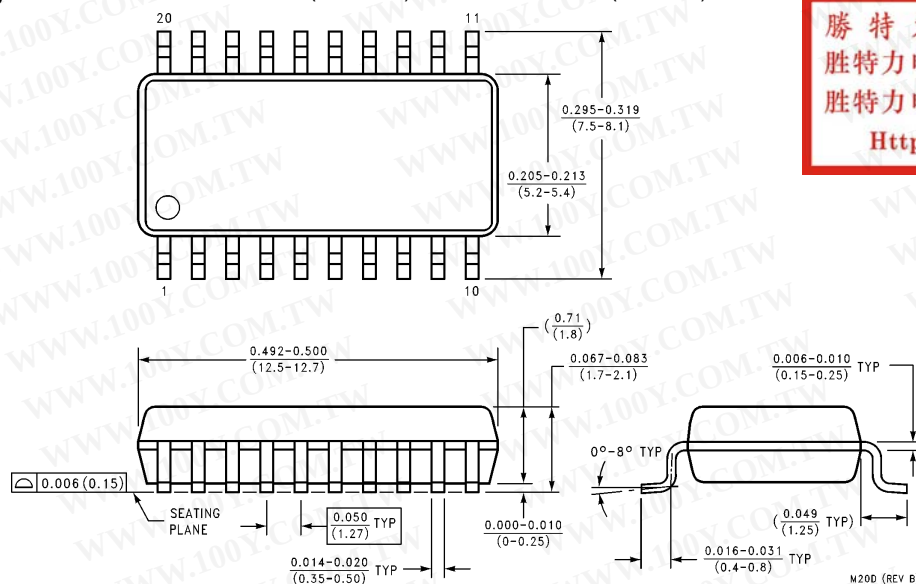
Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)
Order Number 74VHC273M or 74VHC273MX
NS Package Number M20B

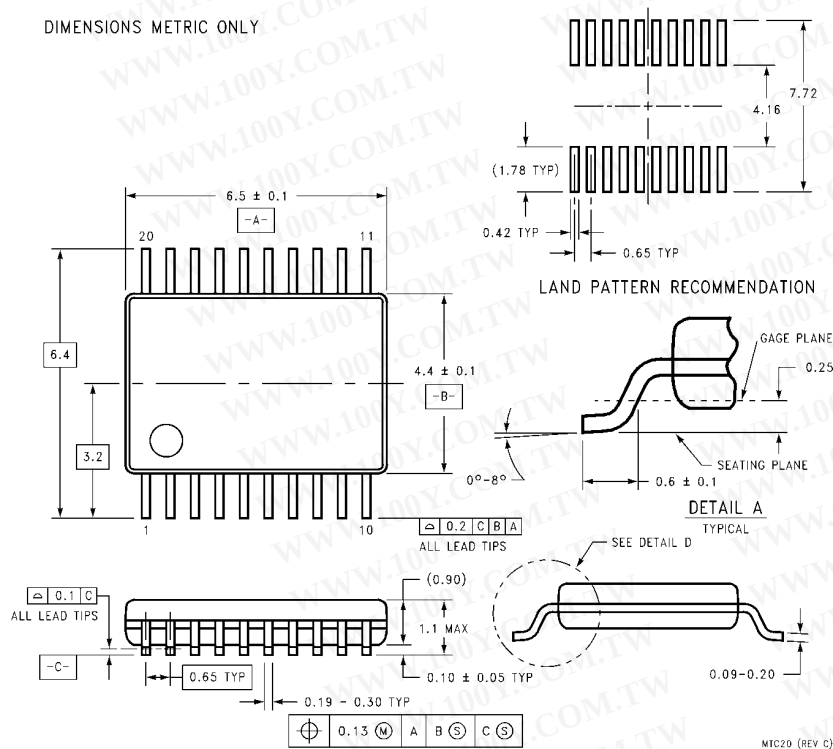
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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic EIAJ SOIC (SJ)
Order Number 74VHC273SJ or 74VHC273SJX
NS Package Number M200

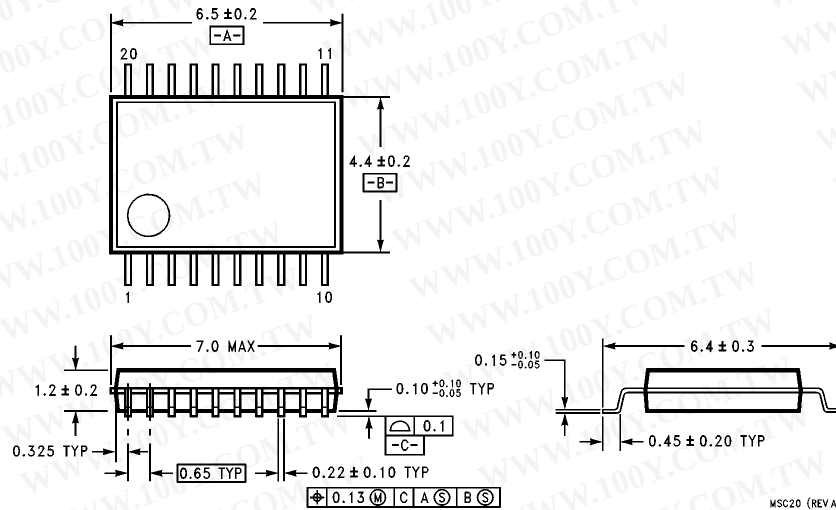
DIMENSIONS METRIC ONLY



20-Lead Molded Thin Shrink Small Outline JEDEC Type I (TSSOP)
Order Number 74VHC273MTC
NS Package Number MTC20

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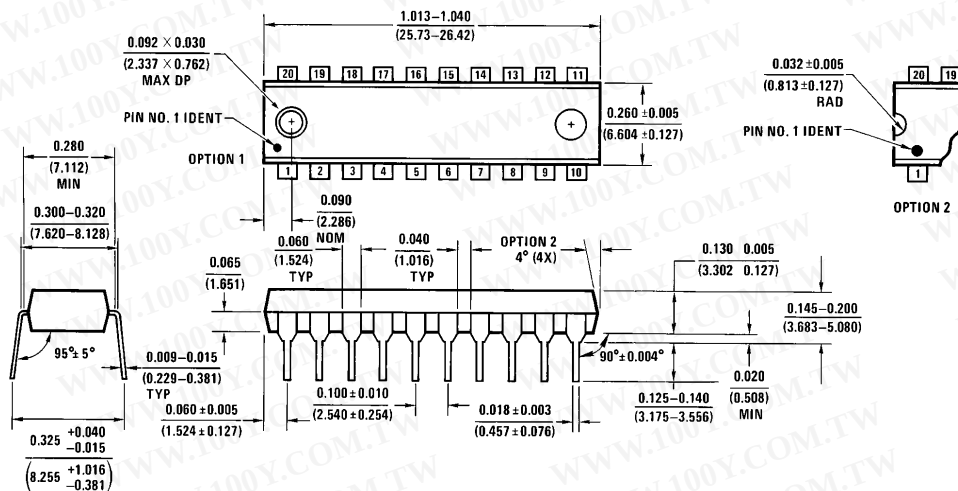
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20-Lead Molded EIAJ, Type I (SSOP)
Order Number 74VHC273MSC
NS Package Number MSC20

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead (0.300" Wide) Molded Dual-In-Line Package
 Order Number 74VHC273N
 NS Package Number N20A

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