Virtex-5 LXT/SXT PCI Express Evaluation Platform Board

TB-5V-LX50T/LX110T/SX50T/FX70T-PCIEXP

Virtex-5 LXT/SXT is the High-performance FPGA with advanced serial connectivity.
TB-5V-LX50T/LX110T/SX50T/FX70T-PCIEXP is an ideal High-speed evaluation platform for 8-lane PCI Express. In addition, it supports multiple High-speed serial transceiver interfaces with SFP and SMA connector ports. On-board Camera Link port is useful for a wide variety of video applications such as image processing. Inrevium's board can easily enhance the I/O function by using the option board. Various option boards are available for customer's evaluation purpose.

▌ Features

FPGA
Xilinx Virtex-5: XC5VLX50T/LX110T/ SX50T/FX70T -1FFG1136

Interfaces
-PCI Express 8 lane (2.5Gbps x8)
-Camera Link Rx Connector x1(Base Configuration)
-SFP x2port (Max3.2Gbps x 2)

Memory
-DDR2 SDRAM (512Mb /400Mbps) 1chip
-DDR2 SO-DIMM: 1pc

For processor (MicroBlaze)
-10/100/1000Mbps Ethernet
-MICTOR Connector x1 (For Debugger)

Power Supply
LTC Power Management Solution
-**LTC3776**
-**LTM4600**
-**LTC3026**
-**LTC3773**
-**LT1761**
-**LTC3407-2**

Others
-MMCX Connector x2(MAX3.2Gbps x2)
-Samtec Connector x1(For LX110T/FX70T ,MAX3.2Gbps x4)
-50 IO Pin Header x2(For LX110T/FX70T)
-Connector for Option Board x3 (For LX50T/SX50T x1)
-Push switch x4/ DIP switch x8/ LED x8

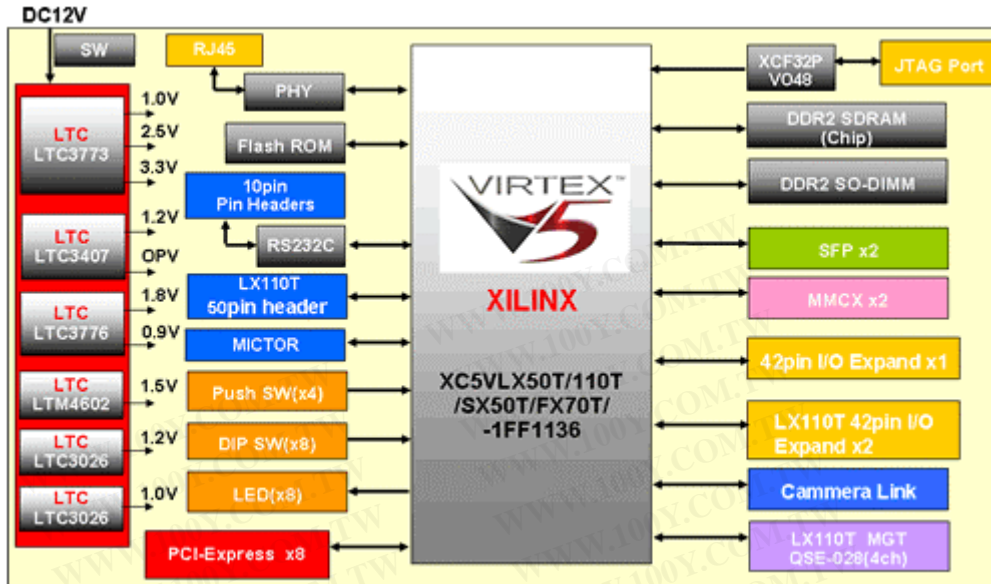**Reference Design, Application and Driver**
-Image data DMA transfer Reference Design (Addin Card-PC)
-Sample Application for Windows XP (Binary)
-Sample Driver for Windows XP (Binary)
-RocketIO Loop Back Reference Design (Aurora,8B10B,PRBS)
-TEMAC Reference Design (For MicroBlaze)

Block Diagram

TB-5V-LX50T/110T/SX50T/FX70T-PCIEXP

User's Manual(Summary)

Rev. 2.01

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■ Repair of the board is carried out by replacing it on a chargeable basis; not repairing the faulty devices.

■ Replacement of initial faults carried out by free of charge, however, it is required for the customer to inform us of relevant problem within two weeks after delivery.

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<<Table of Contents>>

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1. Introduction

This document describes the PCI Express Evaluation Board with a high-speed serial transceiver interface "**TB-5V-LX50T/110T/SX50T/FX70T-PCIEXP**".

2. Accessory

- 12V 5A   AC adapter
- Screw x 8, Spacer x 4

3. Feature

1. FPGA (Xilinx's XC5VLX50T/110T-1FF1136 or XC5VSX50T-1FF1136 or XC5VFX70T-1FF1136)
2. Xilinx's Virtex-5 series PCI Express (x8) for interfacing with a PC
3. DDR2-SDRAM (on Board) x 1
4. DDR2 SO-DIMM connector x 1
5. 10/100/1000Mbps Ethernet MAC & PHY
6. 4ch high-speed serial transceiver interface
   - SFP optical module port (2ch)
   - MMCX connector port (2ch)
7. Power-switching standalone application

4. Safety Precautions

Before using this board, read these safety precautions carefully to assure correct use.

Failure to do so will damage this board or result in fire or personal injury.

This board is designed and manufactured on the assumption that it is used by personnel who have adequate knowledge and experience regarding electronic circuits.

If the board is used by personnel who do not have such knowledge or experience, be sure to use it under proper supervision.

- Do not use this board for improper purposes.

  This board is designed for use in a generic indoor environment.   Do not use it in areas exposed to condensation, metal powder or corrosive, flammable or explosive gases.

- Connecting ICs/LSIs or cables in reverse orientation could damage them or this board.   Before connecting them, be sure to check for proper orientation.   Do not install or connect/disconnect them with the power switch kept ON or without electrostatic protection.

- Do not connect a device to the PCI slot on the motherboard with the power switch kept ON or without electrostatic protection.

  Do not place this board on the conductor such as steel plate or conductive sponge, otherwise onboard ICs/LSIs could be damaged.   Before turning power switch on, be sure to check carefully if there are no flammable dusts or conductive material such as wire chips on the board.

  This board allows two power supply channels, one from the PCI slot and the other from the external power connector.   This can be selected by setting onboard jumper pins.   Before turning the power switch on, be sure to check if they are correctly set.

- Observe rated supply voltage requirement and be careful about voltage polarity.

- Tokyo Electron Device Limited assumes no responsibility or liability for any losses or damages caused by modification of this board or design/implementation of a sub-board.

- Do not place this board in areas exposed to shock or vibration.

- Be careful about fire since the onboard FPGA, CHIP, DIMM and power regulator can generate heat.

- Be careful when inserting a memory device into the onboard DIMM socket.   (Number of connecting/disconnecting to or from the DIMM socket is limited to 25).

5. Board Overview

Board size: 310.0 x 111.15 x 1.6[mm] (Not in compliance with PCI-Express standard)

Board thickness is not included parts width. The board might interfere in PCI Express slot, Please be careful for space with the neighboring PCI Express card.
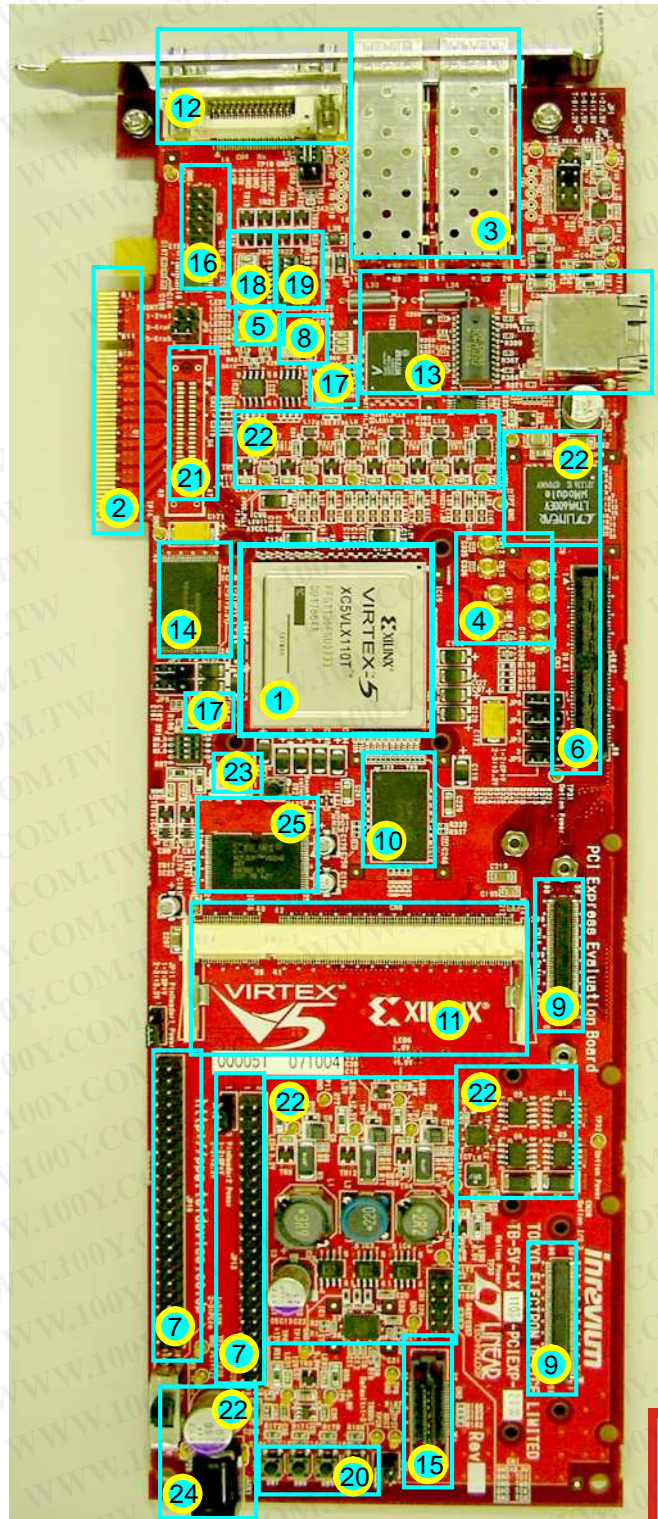
5-1 External View
- TB-5V-LX110T-PCIEXP
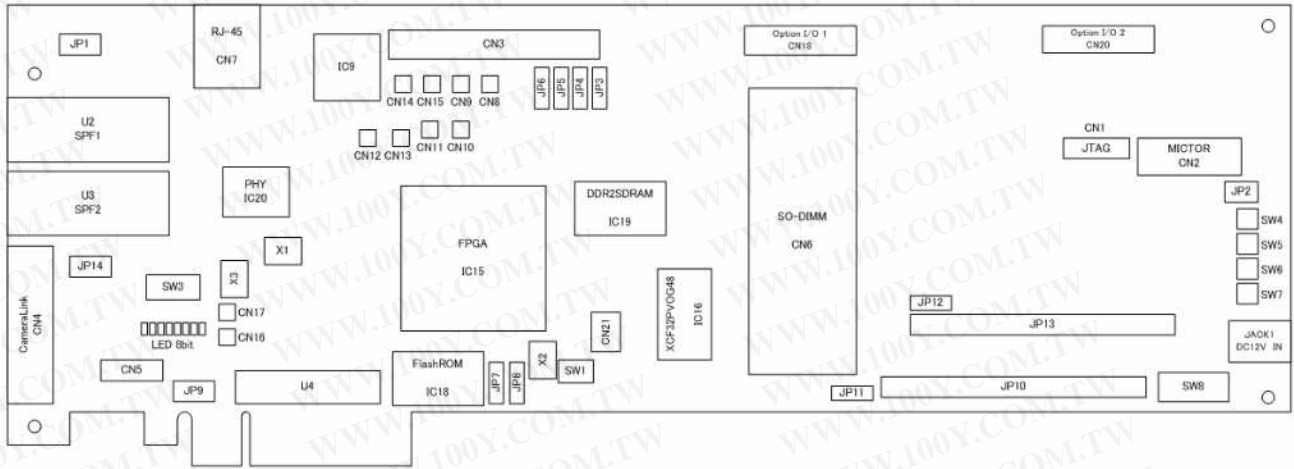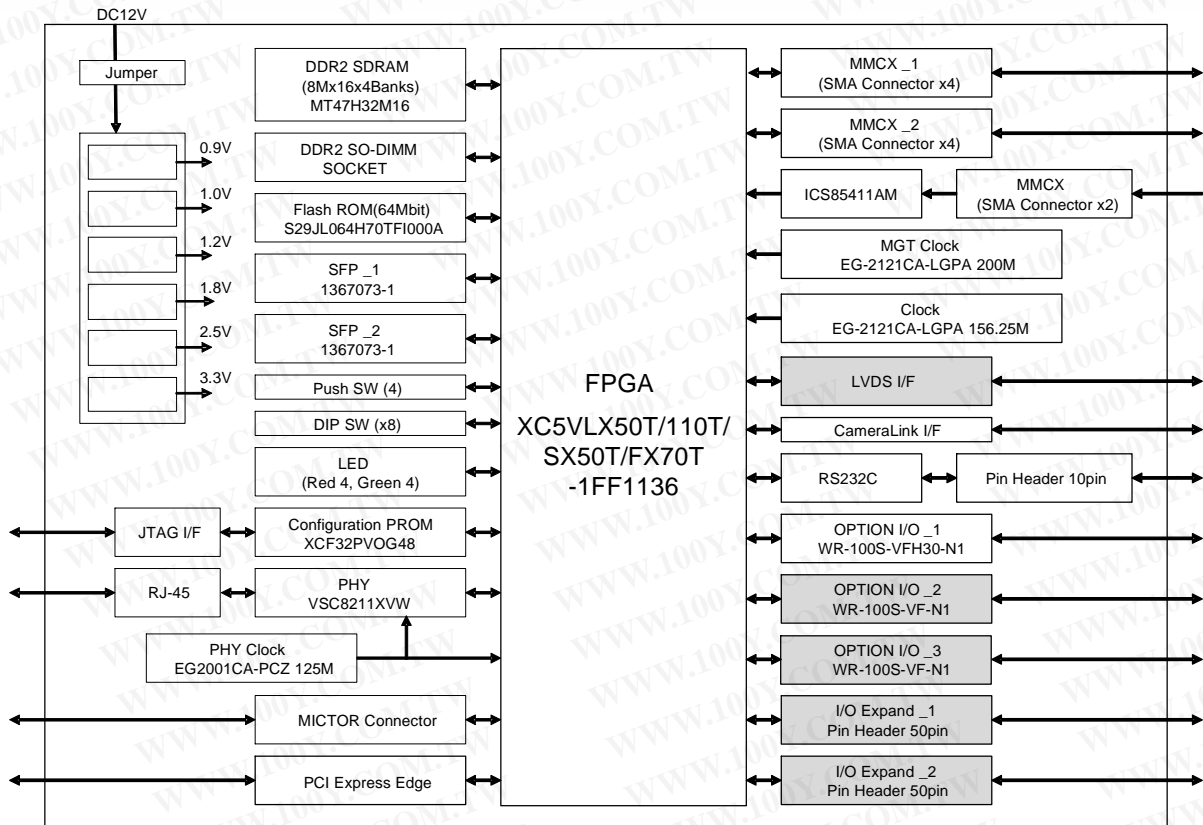

Figure5.1 External View

5-2 Block Diagram

Figure5.2 Board Configuration Diagram

NOTE : Gray Block is available for TB-5V-LX110T/FX70T-PCIEXP only.

Figure5.3 Functional Block Diagram

5-3　Main Components and Functions

5-3-1　XC5VLX50T/110T-1FF1136 , XC5VSX50T-1FF1136 and XC5VFX70T-1FF1136 ①

- Provides interfacing with the PCI Express edge using Xilinx Virtex5LXT/SXT/FXT's PCI Express
 Block function.
- Provides a high-speed serial transceiver interface to connect the SFP optical module port, MMCX connector
 port and Option connector .
- Provides connection to the DDR2-SDRAM Chip with 16 data bits and 15 address (including BANK address)
 bits, Can be possible DDR (Double Data Rate) 400Mbps data transfer.
- Provides connection to the DDR2-SO-DIMM with 64 data bits and 19 address (including BANK address) bits,
 Can be possible DDR (Double Data Rate) 400Mbps data transfer.

For information about FPGA configuration, refer to Section 7.
- Configuration is implemented using the XCF32PVO48 in Master Parallel Mode.
- The JTAG chain is connected to the XCF32PVO48 and the FPGA.

5-3-2 PCI Express Edge ②

- "x8"(8Lane) connection is allowed.
- Some signals have the P/N polarity of FPGA's high-speed I/O "GTP" and the "PCI Express edge" connected
  reversely. Because that is easy to keep signal quality and a function to automatically reverse the polarity at
  the GTP's receiving end is used.　Use the LogiCORE PCIExpress Block Plus.　Refer to Figure 5.4.
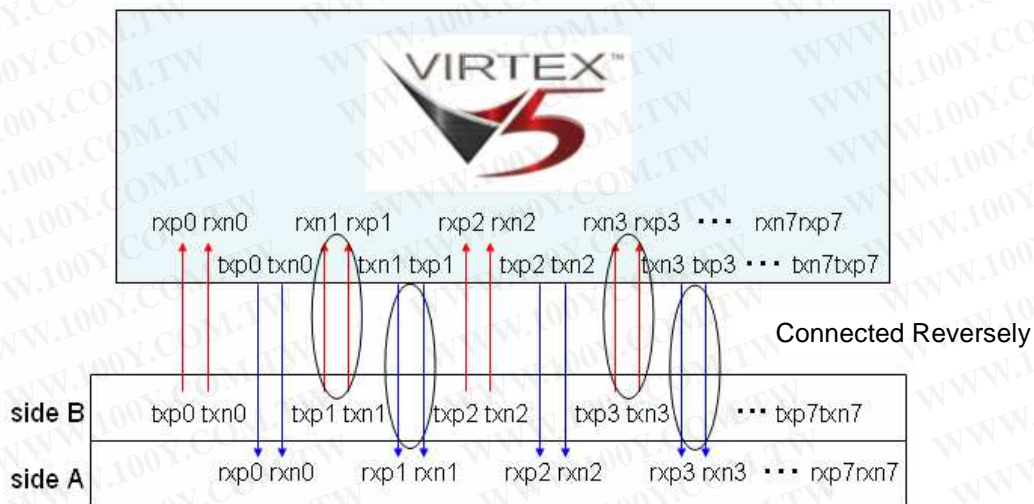

Figure5.4 GTP Signal Connection

5-3-3 SFP Optical Module Port 3

- The SFP optical module is supported.

  The control signals to be connected to the SFP optical module is connected to the onboard through-hole (Φ0.8).

* A loopback evaluation test has been performed using AVAGO's AFBR-57R5APZ optical module.
  [MAX:3.125Gbps]

5-3-4 MMCX Connector Port 4

- MMCX connector: Samtec's MMCX-J-P-H-ST-TH1

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5-3-5 MMCX Connector Port for Clock Input 5

- MMCX connector: Samtec's MMCX-J-P-H-ST-TH1
- The clock signals input from the MMCX connector are divided into two channels using the onboard IDT's ICS85411 and supplied to FPGA's GTP clock pins.

5-3-6 High-Speed Serial Interface (GTP) 6

- GTP connector for channel 4 : Samtec's QSE-028-01-F-D-DP-A
- **Used for TB-5V-LX110T/FX70T-PCIEXP only**

5-3-7 User Pin Header 7

  The board provides two 40-bit I/O pin headers for waveform monitoring by an oscilloscope and signal connection to an external board.   **It is applied to only TB-5V-LX110T/FX70T-PCIEXP.**

5-3-8 GTP Clock 8

- The clock signal from the X3 converts into LVDS and connects it to the FPGA's GTP clock pin using an onboard IDT's ICS85411.
- GTP Clock (X3): Epson Toyocom's EG2121CA-LGPA156.25M

5-3-9 Option I/O 9

- The board provides 3 Option I/Os for connecting the dedicated Option board.
- The Option I/O 1 connects to CN18, Option I/O 2 to CN19 and Option I/O 3 to CN20.

5-3-10 Memory DDR2-SDRAM 10

- The board provides a DDR2-SDRAM (MT47H32M16BT-37E).
- Series resistors are installed at the memory side for DQS/DQ signals and at the FPGA side for address/control signals.

  It is assumed that the ODT at the memory side is used for termination.   The FPGA side is not terminated.

5-3-11 Memory DDR2-SO-DIMM 11

- The board provides a 200pin SO-DIMM connector that allows DDR2-SO-DIMM connections.
- Series resisttors are installed at the memory side for DQS/DQ signals and at the FPGA side for address/control signals.

  It is assumed that the ODT at the memory side is used for termination.   The FPGA side is not terminated.

5-3-12 CameraLink 12
- CameraLink MDR Connector (CN4): 3M's 10226-1A10PE

5-3-13 Ethernet MAC & PHY 13
- The board uses a VITESSE's chip as PHY to enable10/100/1000M Ethernet connections via a RJ-45 connector (CN7).
- PHY Chip (IC20): VITESSE

■ Due to the NDA contract with parts makers, we are not allowed to disclose technical information on the circuits around Ethernet on this board.

5-3-14 FlashRom 14
- FlashROM (IC18): Spansion's S29JL064H70TFI000A

5-3-15 MICTOR Connector 15
- MICTOR Connector: AMP's 2-5767004-2
- JTAG-ICE can be connected through the MICTRO Connector.
  * To connect an ICE, set SW1 and JP2 according to the ICE manual. (ICE : Computex's F-sight)

5-3-16 RS232C 16
- The board uses an RS232C driver to enable serial connections via a pin header (CN5).
- RS232C Driver IC (IC17): MAXIM's MAX3380ECUP

5-3-17 Universal Clock 17
- The board provides a 200MHz low-jitter crystal oscillator for high speed I/O operation.
  It also provides 125MHz low-jitter crystal oscillator for PHY.

5-3-18 User LED 18
- The board provides four red LEDs (LED 19-22) and four green LEDs (LED 23-26).
- All these LEDs will light on in Active High.

5-3-19 User Dip Switch 19
- The board provides an 8bit Dip Switch. The side of the Dip Switch labeled "ON" is Low Level.

5-3-20 User Push Switch 20
- The board provides four Push switches.
- Each switch provides a Low signal while it is kept pressed.

5-3-21 PCI Express MidBUS Probe 21
- The board can connect a MidBUS probe for PCI Express.

5-3-22 External Power Connector + Power Module 22

- The power supply can be switched either to the PCI Express edge or the external power connector using the power selection switch.
- The board generates a variety of different voltage from the 12V using LINEAR TECHNOLOGY's on board power chip.
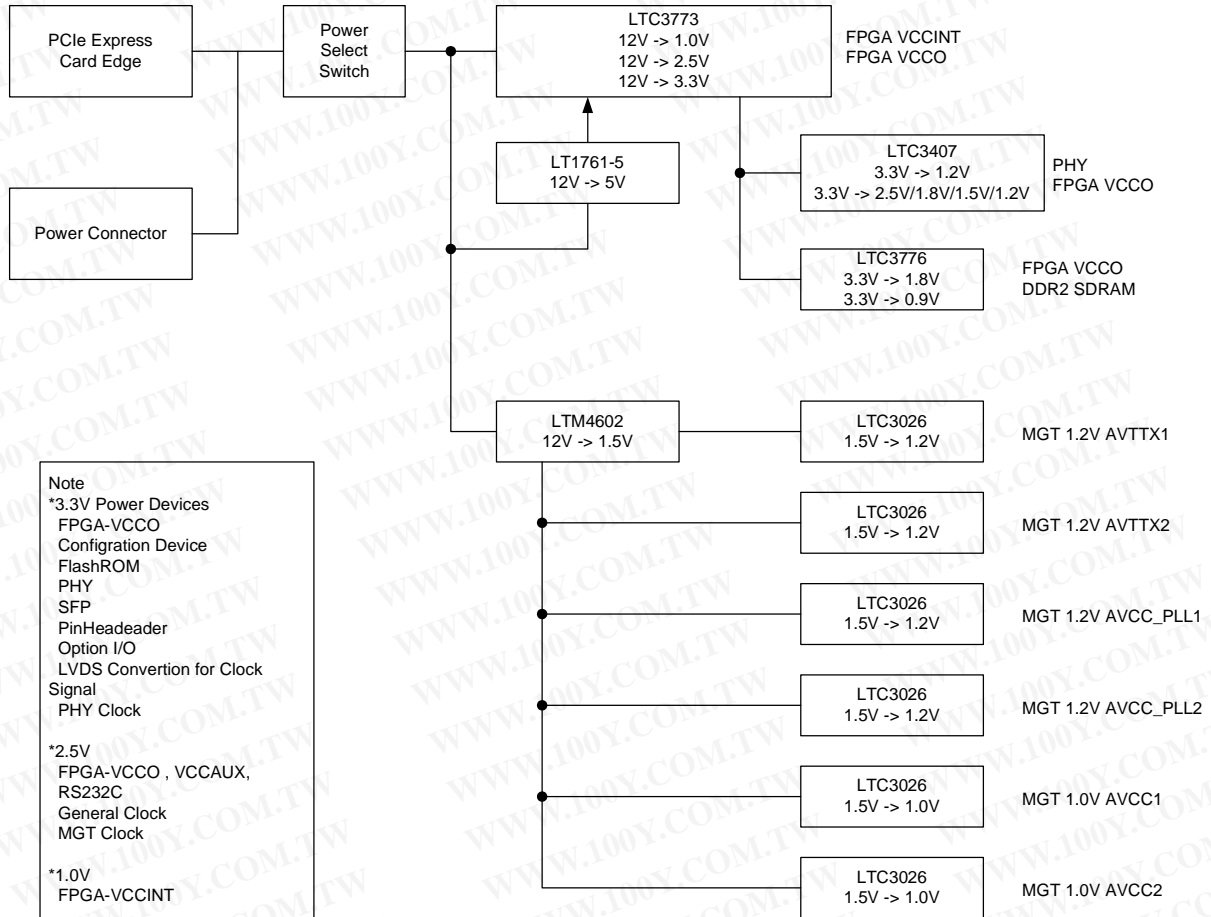

Figure5.11 Power Supply Diagram

5-3-23 Power Connector for Air-Cooling Fan 23

- The board provides a 12V power supply for air-cooling fan.   A fan is not provided.
- Connector: JST's B2B-XH-Ag

6. Jumper Pin Setting

6-1 Jumper Pin Setting

Table6.1 Jumper Pin Setting

Reference	# of Pins	Function	Default	Remarks
JP1	8	Power voltage selection (OP_V)	Open	1-2 2.5V
				3-4 1.8V
				5-6 1.5V
				7-8 1.2V
JP2	4	Configuration selection	1-3Short	1-3 IC16
				Open CN2
JP3	3	VCCO variable function for Bank3	2-3Short	1-2 OP_V
				2-3 3.3V
JP4	3	VCCO variable function for Bank5 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP5	3	VCCO variable function for Bank23 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP6	3	VCCO variable function for Bank20	2-3Short	1-2 OP_V 2-3 3.3V
JP7	3	VCCO variable function for Bank6 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP8	3	VCCO variable function for Bank25 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP9	9	PCI Express edge PRSNT signal selection	1-2Short	1-2 x1 3-4 x4 5-6 x8
JP11	3	Variable function for pin header 1 (JP10) power Only available for TB-LX110T/FX70T -PCIEX	1-2Short	1-2 OP_V 2-3 3.3V
JP12	3	Variable function for pin header 2 (JP13) power Only available for TB-LX110T/FX70T -PCIEX	1-2Short	1-2 OP_V 2-3 3.3V

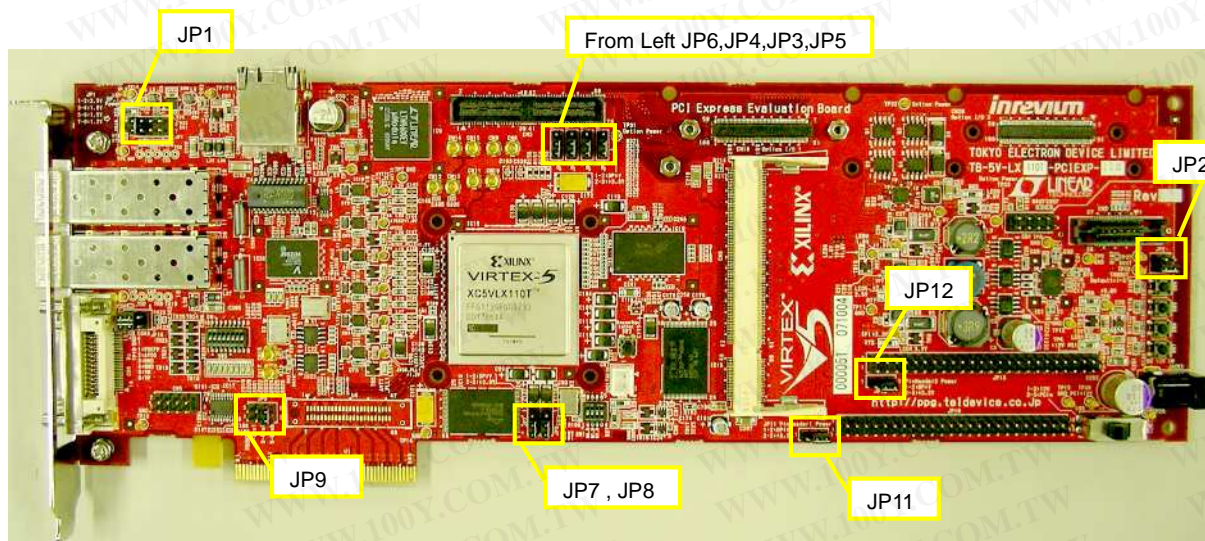**NOTE : Gray Block is available for TB-5V-LX110T/FX70T-PCIEXP only.**

Figure 6.1 Jumper Pin Setting

inrevium

6-2 External Power Connector and Power Selection Switch   24

- The SW8 allows power selection of either the PCI Express edge or the external power jack (JACK1).
  To connect the external power to JACK1, select the +12V.

Table 6.2 Power Selection Switch

Reference	# of Pins	Function	At factory	Remarks
SW8	2	Power selection 1PIN-side: External 3PIN-side: PCI Express edge	1PIN-side	

* In the above picture the power is supplied from the PCI Express edge.

Figure 6.2 External Power Jack and Power Selection Switch

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7. FPGA Configuration 25

- Let's perform FPGA configuration from the XCF32PVO48(IC16).
  Connect a JTAG cable to the 10-pin header(CN1) and download the PROM file created by the Xilinx's iMPACT tool.   Then, turn the power switch on again to configuration FPGA from XCF32PVO48.   If the configuration is successfully, the green-colored LED18 "DONE_LED" will light up.
  To implement the re-configuration, press the SW2.

*   When downloading a file to the XCF32PVO48, make sure that the "Parallel mode" checkbox is checked on the Xilinx's iMPACT tool window.

LED17   DONE_LED

SW1   FPGA MODE SW

CN1   JTAG Pin header

Figure 7.1 Configuration

<<Revision History>>

Revision	Date	Description
Rev.1.00	2007/10/1	Initial release
Rev.1.01	2007/11/12	Add New devise lineup XC5VSX50T-1FF1136. 4. Board Overview 4-3-2. PCI Express signal connection 4-3-22. External Power Connector + Power Module 6. FPGA Configuration
Rev2.00	2008/9/30	FXT series addition Head office address
Rev2.01	2008/10/15	Table 5.1 is changed

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