Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt254

30 MSPS Monolithic CMOS Triple-Channel 8-bit Image Digitizer

Distinguishing Features

- 30, 20 MSPS Operation
- Bt253 Pin Compatible
- Three 8-bit Video A/D Converters
- Two Sets Software-Selectable Analog Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- Genlock Externally Implemented
- Standard MPU Interface
- TTL Compatible
- +5 V CMOS Monolithic Construction
- 84-pin PLCC Package
- Typical Power Dissipation: 1.5 W

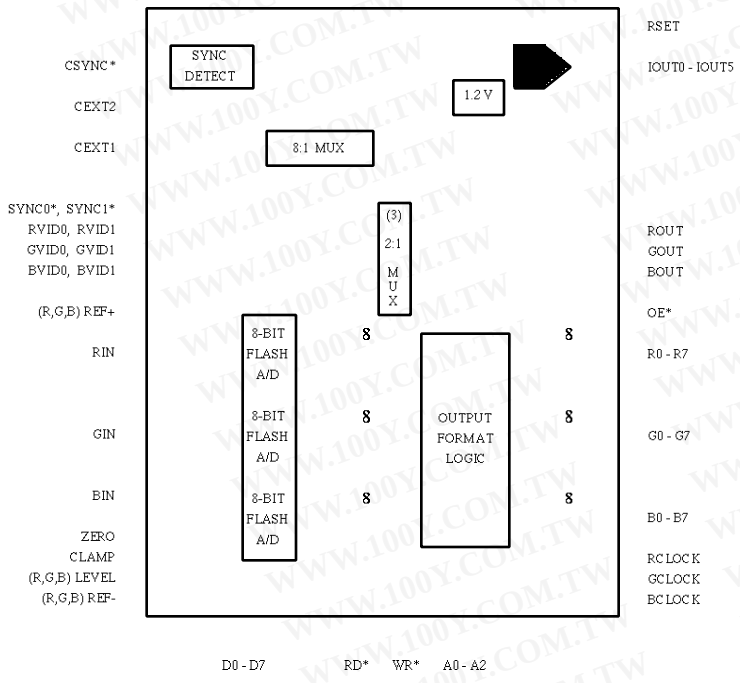
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt252
- Bt261

Functional Block Diagram



Product Description

The Bt254 Image Digitizer is designed to digitize three channels of video signals, such as RGB, YIQ, YUV, etc., generating up to 24 bits of color pixel information. The architecture also supports single-channel digitization of NTSC and CCIR video signals, generating 8 bits of gray-scale pixel information.

The Bt254 supports 24-bit true-color, 15-bit true-color, 8-bit true-color, and 8-bit pseudo-color modes. A standard MPU interface is provided for accessing various control functions.

Six analog inputs (two for each A/D) are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking. A TTL-compatible composite sync signal is output to interface to genlock circuitry. Two additional sync inputs are also provided to support red, green, and blue sync video interfaces.

Optional MPU-controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF- inputs to the A/D converters. Zeroing and clamping signals are available to control the A/D timing for application-specific timing. The clamping levels are externally set via the red, green, and blue LEVEL pins.

Each A/D converter has its own clock input, top/bottom references, and LEVEL pin.

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General Operation

The Bt254 uses three 8-bit flash A/D converters to digitize the video signals. Each A/D digitizes analog signals in the range of REF– ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF–) to $FF (Vin ≥ REF+).

Each A/D converter has its own top and bottom reference: RREF+ and RREF– for the red A/D, GREF+ and GREF– for the green A/D, and BREF+ and BREF– for the blue A/D. Each A/D converter also has its own clock input: RCLOCK for the red A/D, GCLOCK for the green A/D, and BCLOCK for the blue A/D.

RIN, GIN, and BIN may be either DC- or AC-coupled to the video signals. If AC-coupled, the CLAMP and (R,G,B) LEVEL controls may be used to DC-restore the video signals.

Figure 1 shows the internal A/D architecture in detail. Figure 2 shows the input/output timing of each A/D on the Bt254. The samples are taken following the falling edge of (R,G,B) CLOCK. One positive CLOCK edge later, the registered data is output on (R,G,B) 0–7.

MPU Interface

As shown in the functional block diagram, the Bt254 supports a standard MPU interface (D0–D7, RD*, WR*, and A0–A2). MPU operations are asynchronous to the clocks.

A0–A2 address the internal registers, as shown in Table 1.

Analog Signal Selection

The Bt254 supports two analog input sources for each A/D converter: RVID0 and RVID1, GVID0 and GVID1, and BVID0 and BVID1. The MPU specifies which ones are to be digitized via the command register.

The selected video signals are output onto ROUT, GOUT, and BOUT. ROUT, GOUT, and BOUT may be connected directly to RIN, GIN, and BIN, respectively, if no filtering or gain of the video signal is required.

If digitizing only the luminance information of a video signal that contains color subcarrier information, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low-pass filter, notch filter, or comb filter may be used to remove the chroma information.

Note that sync information (if present) will still be present on ROUT, GOUT, and BOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

A2, A1, A0	Addressed by MPU
000	command register
001	IOUT0 data register
010	IOUT1 data register
011	IOUT2 data register
100	IOUT3 data register
101	IOUT4 data register
110	IOUT5 data register
111	reserved

Table 1. Register Addressing.

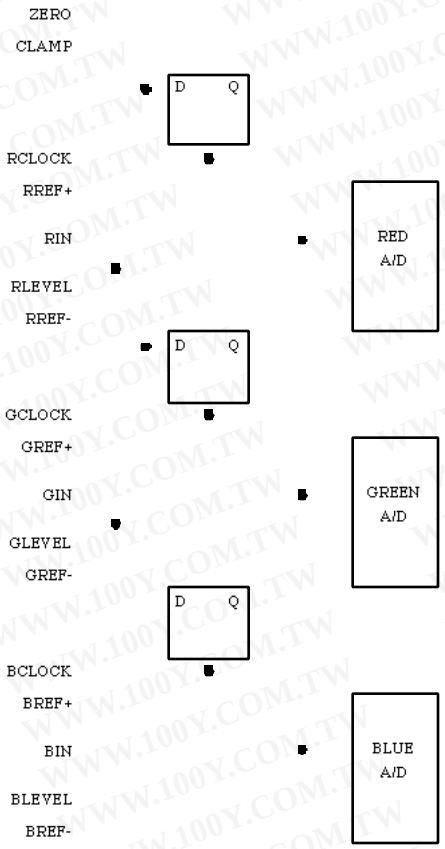


Figure 1. Internal A/D Architecture.

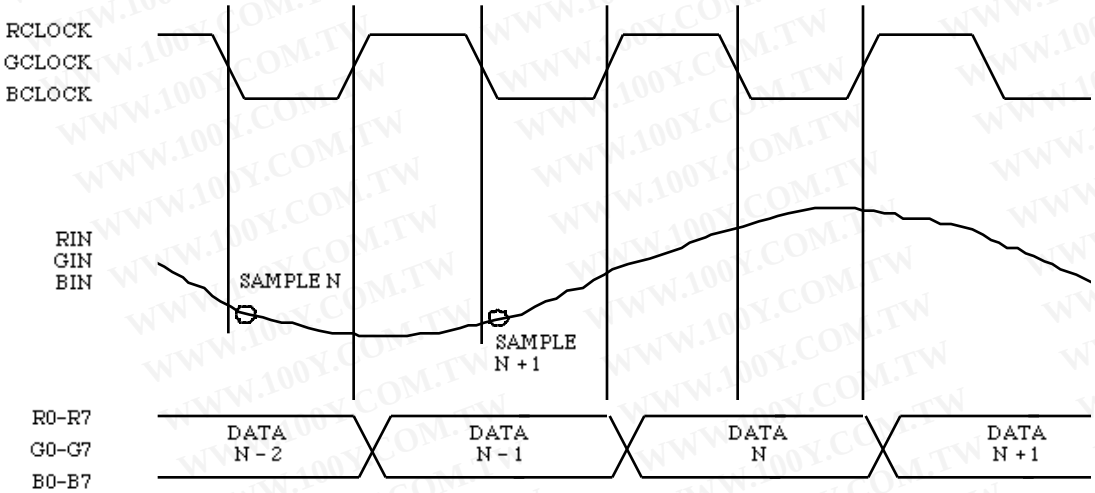


Figure 2. Input/Output Timing.

A/D Reference Generation

As shown in Figure 3, the Bt254 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, RREF+ is connected to a 0.7–1.2 V reference (VREF) and RREF– is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7–1.2 V and no adjustment of gain or offset.

If jumpers J1 and J3 are selected, gain and offset of the video signal may be done via the MPU-adjustable outputs IOUT0 and IOUT1. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations such as contrast enhancement or level adjustments may be implemented. The TLC272 dual CMOS op-amps can be used for single +5 V operation. However, due to limitations of single supply op-amps, REF– may not be able to achieve a voltage below 300 mV with a single 5 V supply. See *Using an External Reference.*

GREF+, GREF–, BREF+, and BREF– may be similarly configured.

IOUT0–IOUT5 are current outputs (0–2.5 mA) generated by six 8-bit D/A converters. A 511 Ω RSET resistor generates a 2.35 mA full-scale output current. The 511 Ω resistors to GND generate a 0–1.2 V level that drives the (R,G,B)REF+ and (R,G,B)REF– inputs through voltage followers.

It is not recommended that the DAC outputs drive the top of the reference ladders directly as the reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of (R,G,B)REF– is desired, the DAC outputs must drive (R,G,B)REF– using a voltage follower.

A/D Zeroing

The ZERO input is used to zero the comparators, and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the R0–R7, G0–G7, and B0–B7 outputs are not updated. They retain the data loaded before the ZERO cycle.

Note that each A/D converter uses its own clock to latch the ZERO signal. Thus, ZERO must be asserted for at least one clock cycle of the slowest clock.

AC-coupled Video and A/D Input Clamping

When AC coupling, capacitors are required on all video inputs. A capacitor may also be needed between (R,G,B)IN and (R,G,B)OUT depending on the filtering implementation. (Refer to Figure 3.) The video mux will DC-adjust the input video to prevent channel-to-channel crosstalk through the video mux.

During clamping, the resistances of the mux and clamp are approximately 100 and 50 Ω, respectively. Incorporation of the 0.1 µF clamp capacitor yields an RC time constant of 15 µs. On power-up or after a transition of the video input, it will take approximately 3–5 time constants to completely DC-restore the video signal. When the clamp is asserted on the back porch for 0.5–1.5 µs, it will take several lines of video to properly DC-restore the signal. For example, clamping the video signal for 1 µs during each line of video will require 75 lines of video for proper DC restoration. This is assuming five time constants are needed.

DC-Coupled Video

When DC coupling, the video levels must be within the digitization range of the A/D. To avoid channel-to-channel crosstalk through the video mux, nonsynchronized video sources must not be allowed to drop more than 100 mV below ground. For example, if the black/blank level of the DC-coupled video is at ground, an external sync clipper must be used to guarantee that the sync tip does not drop below –100 mV. If (R,G,B)IN is DC-coupled to the video signal, all three level pins should float, or the clamp should always be a logical zero.

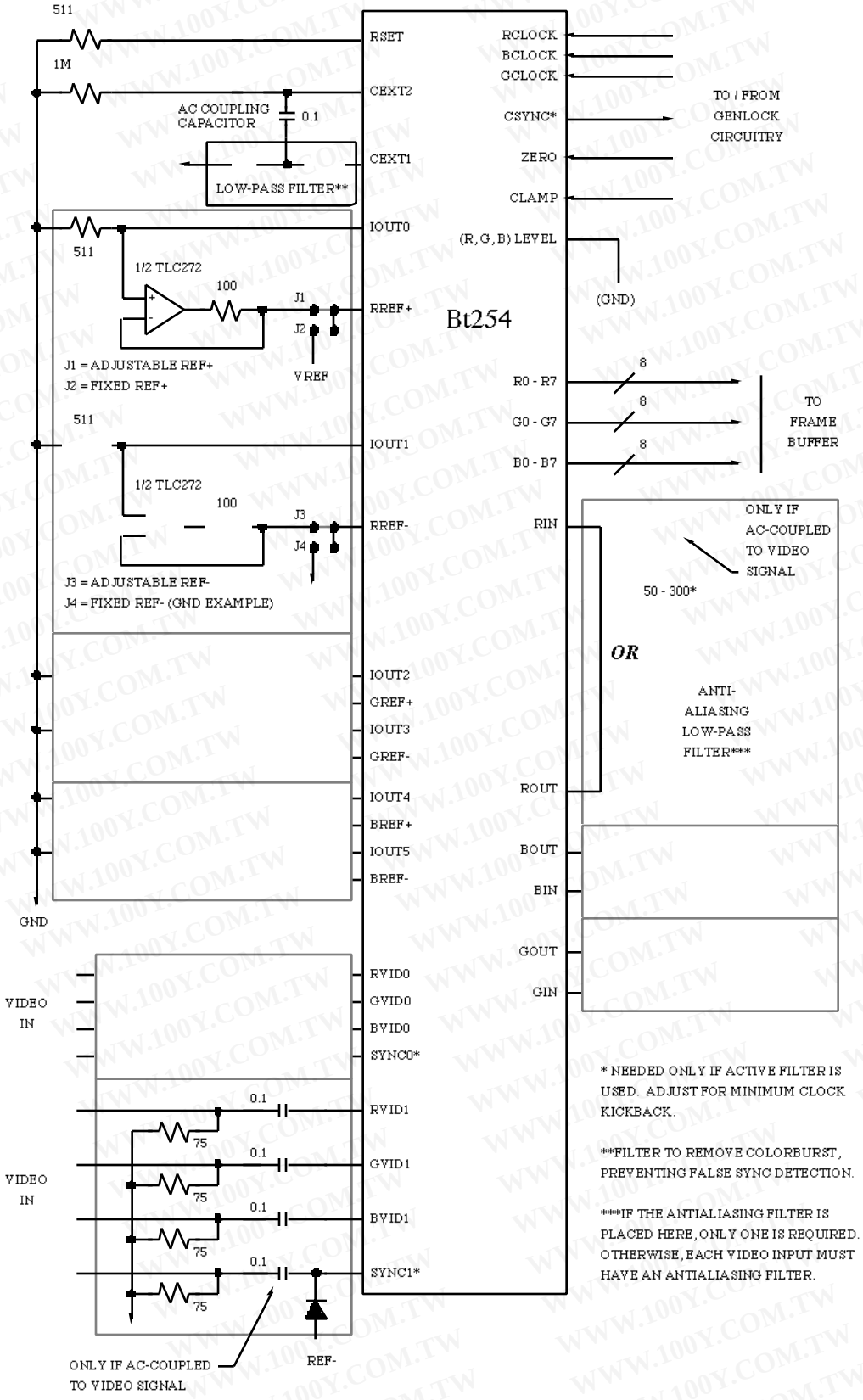


Figure 3. Typical Bt254 External Circuitry.

Antialiasing Filtering and (R,G,B)IN Input Considerations

The input video must be passed through an antialiasing filter to meet Nyquist criteria. The filter can be placed between (R,G,B)IN and (R,G,B)OUT to filter all video sources or on each video input before the MUX. The 50–300 Ω resistor shown in Figure 3 after the low-pass filter is required only if an active low-pass filter is used. It provides isolation from any clock kickback noise on (R,G,B)IN, preventing it from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on (R,G,B)IN. If no filter or a passive low-pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

If DC restoration and low-pass filtering are implemented, a 0.1 µF is required after the low-pass filter. If no filter or a passive low-pass filter is used, the capacitor is not required, as the DC restoration can still be implemented using the 0.1 µF capacitors on the (R,G,B)VID inputs.

Multiplexer Considerations

Maintaining DC levels within the rated compliance range is necessary to obtain the best linearity and crosstalk performance.

Sync Detect Circuitry

The Bt254 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. Note that CSYNC* is output asynchronously to the clock and there are no pipeline delays (the output delay from Vin or SYNC* to CSYNC* is approximately 25 ns).

The MPU specifies from which input to detect sync (negative sync polarity). The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC-couples the video signal to the sync detection circuit. The sync tip is internally clamped to a DC level. The sync detect value determines the threshold above this DC level where the Bt254 detects sync. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero.

Two additional sync inputs are provided (SYNC0* and SYNC1*) to support red, green, and blue sync systems. SYNC0* and SYNC1* may be either TTL or normal video signal levels.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 3).

If the sync detection circuit is not used, CEXT2 should be connected to GND or VAA (CEXT1 may float), or an unused (grounded) video input selected for the sync detector.

External Sync Detection

CEXT1 may be connected to an external sync detector circuit. In this case, CEXT2 should be connected directly to GND or VAA and the CSYNC* output left floating.

The sync analog multiplexer may still be used to select from which video source to detect sync information. As the multiplexer switches analog video signals, the selected video source will be output onto CEXT1.

Color Output Modes

The Bt254 outputs several modes of color information, as shown in Table 2.

R0–R7, G0–G7, and B0–B7 are three-stated while OE* is a logical one.

Output Pins	24-Bit True Color Mode (00)	15-Bit True Color Mode (01)	8-Bit True Color Mode (10)	8-Bit Pseudo Color Mode (11)
R7	R7	0	R7	G7
R6	R6	R7	R6	G6
R5	R5	R6	R5	G5
R4	R4	R5	G7	G4
R3	R3	R4	G6	G3
R2	R2	R3	G5	G2
R1	R1	G7	B7	G1
R0	R0	G6	B6	G0
G7	G7	G5	R7	G7
G6	G6	G4	R6	G6
G5	G5	G3	R5	G5
G4	G4	B7	G7	G4
G3	G3	B6	G6	G3
G2	G2	B5	G5	G2
G1	G1	B4	B7	G1
G0	G0	B3	B6	G0
B7	B7	0	R7	G7
B6	B6	0	R6	G6
B5	B5	0	R5	G5
B4	B4	0	G7	G4
B3	B3	0	G6	G3
B2	B2	0	G5	G2
B1	B1	0	B7	G1
B0	B0	0	B6	G0

Table 2. Color Output Configurations.

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit.

D7	Digitize select (0) xVID0 (1) xVID1	This bit specifies which analog input is to be digitized. The selected signals are output onto ROUT, GOUT, and BOUT.
D6–D4	Sync detect select (000) RVID0 (001) RVID1 (010) GVID0 (011) GVID1 (100) BVID0 (101) BVID1 (110) SYNC0* (111) SYNC1*	Composite sync information detected on the selected input is output onto CSYNC*.
D3, D2	Color output select (00) 24-bit true color (01) 15-bit true color (10) 8-bit true color (11) 8-bit pseudo color	Color output mode select. See Table 2. In mode (11), the red and blue A/D converters are ignored.
D1	Reserved (logical zero)	A logical zero must be written to this bit when writing to the command register.
D0	Sync detect level select (0) 125 mV (1) 50 mV	This bit specifies how much above the sync tip to slice CEXT2 for sync detection.

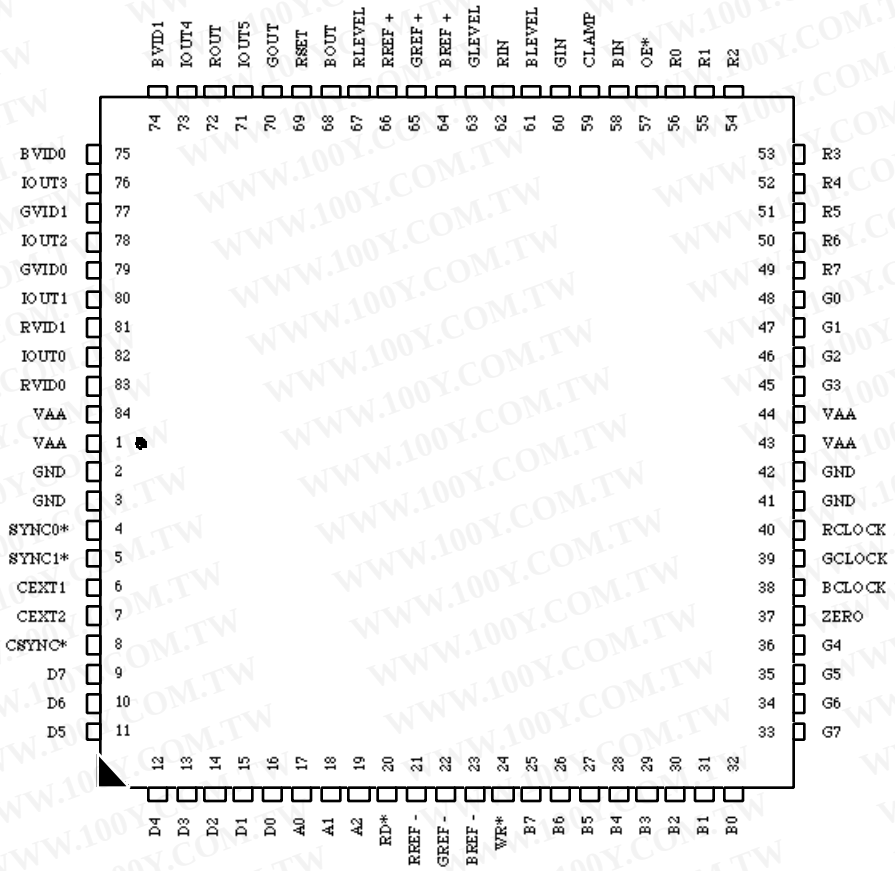
IOUT Data Registers

These six 8-bit registers specify the output current on the IOUT0–IOUT5 outputs, from 0 mA ($00) to full scale ($FF). The 8-bits of data are used to drive the DACs.

These registers may be written to or read by the MPU at any time and are not initialized. D0 is the least significant bit.

Pin Name	Description
General Reference Functions	
RSET	Full-scale adjust control. An external 511 Ω resistor must be connected between this pin and GND. It is used to provide reference information to the internal D/A converters. See Figure 3.
IOUT0–IOUT5	Current outputs. The amount of output current is specified by the IOUT data registers. External 511 Ω resistors are typically connected between these pins and GND. See Figure 3. The relationship between full scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (Ω)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC-couple the video signal to the sync detect circuitry. A 1M Ω resistor must also be connected between CEXT2 and GND. If AC coupled, amplitude is < 2 Vp–p.
A/D Functions	
RREF+, GREF+, BREF+	Red, green, and blue top of resistor ladder (voltage input). These set the (R,G,B)IN voltage level that corresponds to $FF from the appropriate A/D converter. For noise immunity reasons, decoupling capacitors are *not* recommended for the REF+ pins.
RREF–, GREF–, BREF–	Red, green, and blue bottom of resistor ladder (voltage input). These set the Vin voltage level that generates $00 from the appropriate A/D converter.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D converters are zeroed. The red A/D converter latches ZERO on the rising edge of RCLOCK, the green A/D converter latches ZERO on the rising edge of GCLOCK, and the blue A/D converter latches ZERO on the rising edge of BCLOCK. During zeroing cycles, R0–R7, G0–G7, and B0–B7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the RIN, GIN, and BIN inputs are forced to the voltage level on the (R, G, B) LEVEL pins to perform DC restoration of the video signals. In applications where RIN, GIN, and BIN are DC-coupled to the video signals, the LEVEL pins should float or CLAMP should always be a logical zero. CLAMP is asynchronous to the clocks.
RLEVEL, GLEVEL, BLEVEL	Red, green, and blue level control inputs (voltage inputs). These inputs are used to specify what voltage level is to be used for DC restoration while CLAMP is a logical one. In applications where RIN, GIN, and BIN are DC-coupled to the signals, the LEVEL pins should float or CLAMP should always be a logical zero.
Input Selection Functions	
RIN, GIN, BIN	A/D converter inputs. The analog signals to be digitized should be connected to these analog input pins.
RVID0, RVID1, ROUT	Red channel analog inputs and analog output. RVID0 and RVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto ROUT. Unused inputs should be connected to GND.
GVID0, GVID1, GOUT	Green channel analog inputs and analog output. GVID0 and GVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto GOUT. Unused inputs should be connected to GND.

Pin Name	Description
BVID0, BVID1, BOUT	Blue channel analog inputs and analog output. BVID0 and BVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto BOUT. Unused inputs should be connected to GND.
Timing Functions	
RCLOCK, GCLOCK, BCLOCK	Clock inputs (TTL compatible). It is recommended that these pins be connected together and driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected from the xVID0 or xVID1 input (as specified by the command register), converted to TTL levels, and output onto this pin. SYNC0* or SYNC1* may also be selected as inputs to the sync detector. CSYNC* is output asynchronously to the clocks and there are no pipeline delays.
SYNC0*, SYNC1*	Sync inputs. Sync information may be input via these pins and output onto CSYNC*. SYNC0* and SYNC1* may be either TTL or normal video signal levels. Unused inputs should be connected to GND.
Digital Control Functions	
R0–R7, G0–G7, B0–B7	Digitized video data outputs (TTL compatible). R0–R7 are output following the rising edge of RCLOCK, G0–G7 are output following the rising edge of GCLOCK, and B0–B7 are output following the rising edge of BCLOCK. They are three-stated if OE* is a logical one. R0, G0, and B0 are the least significant bits.
OE*	Output enable control input (TTL compatible). A logical one three-states R0–R7, G0–G7, and B0–B7 asynchronously to the clocks.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0–A2	Address control inputs (TTL compatible). A0–A2 address the internal registers as shown in Table 1. They are latched on the falling edge of RD* or WR*.
Power and Ground	
VAA	+5 V power. All VAA pins must be connected together as close to the device as possible. A 0.1-µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible. (Ceramic chip capacitors are preferred.)
GND	Ground. All GND pins must be connected as close to the device as possible.



PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS Digitizer layout examples found in the Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements, application notes AN-13, 14, and 15, respectively. These application notes can be found in the *Brooktree Applications Handbook*

The layout should be optimized for lowest noise on the Bt254 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

A single ground plane covering both digital and analog logic should be used. The ground plane area should encompass all Bt254 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt254, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt254.

Power Planes

The Bt254 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt254.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt254 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Best performance is obtained using a dedicated linear regulator to provide power to the Bt254.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. These capacitors should also be placed as close as possible to the device. Ceramic chip capacitors are preferred.

Each group of VAA pins should have a 0.1 µF ceramic chip capacitor to GND, located as close as possible to the device.

Digital Signal Interconnect

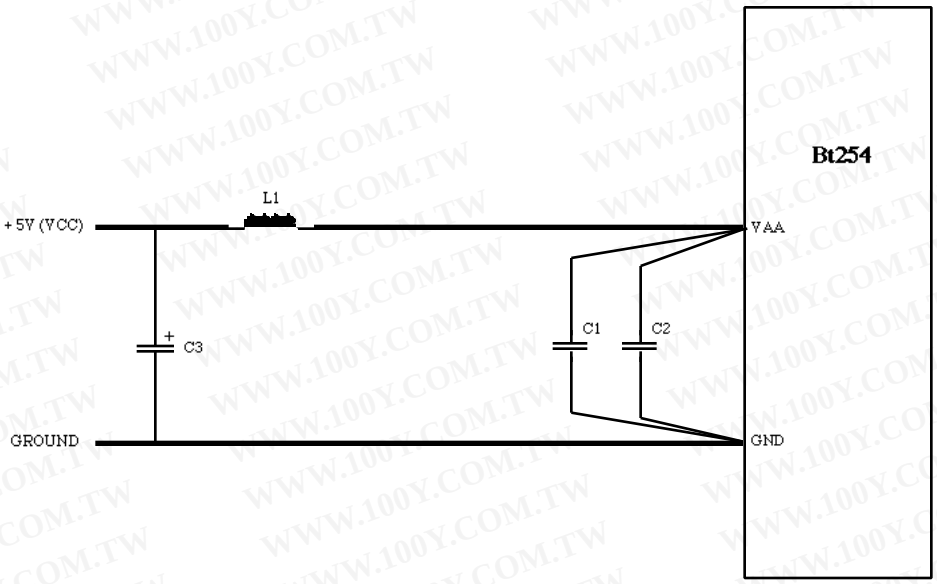
The digital signals of the Bt254 should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs. Microstrip techniques should be employed to keep video trace impedance at 75 Ω.

Also, avoid routing high-speed TTL signals close to the analog signals to minimize noise coupling.



Location	Description	Vendor Part Number
C1, C2* C3 L1	0.1 µF ceramic capacitor 10 µF tantalum capacitor ferrite bead	Erie RPE112Z5U104M50V Mallory CSR13G106KM Fair-Rite 2743001111

*A 0.1-µF ceramic capacitor should be connected between *each group of VAA pins* and GND, as close to the device as possible. (Ceramic chip capacitors are preferred.)

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt254.

Figure 4. Typical Connection Diagram and Parts List.

Zeroing

As the comparators on the Bt254 must be periodically zeroed, it is convenient to assert ZERO during each horizontal blanking interval.

Note that before using the Bt254 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications, this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt254.

As long as the recommended zeroing interval is maintained, the Bt254 will meet linearity specifications. *The longer the time between zeroing intervals, the more the linearity error increases.*

Increasing the Resolution of DACs

With a 511 Ω resistor connected between each DAC output (IOUT0–OUT5) and GND, the resolution of the ladder adjustment is 4.5 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 5 shows a circuit that allows adjustment of the REF+ inputs from 0.714–1 V with 1.125 mV resolution. With the DAC data = $00, 0.714 V is output; if the DAC data = $FF, 1 V is output.

As the typical maximum DAC output current is 2.35 mA (RSET = 511 Ω), if a 0.286 V adjustable range is desired, R1 || R2 must equal 121 Ω. The minimum output voltage desired determines the ratio of R1 and R2:

$$V_{min} = V_{REF} * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF–) may be adjusted from 0–0.286 V with 1.125 mV resolution by using a 121 Ω resistor to ground rather than a 511 Ω resistor. As long as the minimum range is 0 V, the resistor to ground may be used to adjust the total range, and thus the resolution.

Using An External Reference

Figure 6 illustrates the use of a 1.2 V LM385 and a TLC272 to generate a 0 V–1.2 V reference for applications that require a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that is capable of operating from a single +5 V supply.

To prevent the TLC272 from ringing due to clock kickback, a 100-Ω resistor is recommended as shown in Figure 6. If an op-amp is chosen that has a better transient response than the TLC272, the resistor may not be needed. This circuit may also be used to drive the Ref– if a value other than ground is desired. Due to limitations of single-supply op-amps, Ref– may not be set below ~300 mV. To drive Ref– to true 0 V in the op-amp configuration, a dual supply must be used. *Extreme care must be used in power sequencing to ensure all positive supplies (op-amp and A/D) power-on before the negative supply. This will prevent latchup of the A/D.*

Input Ranges

Table 3 shows some common video signal amplitudes. For signals that exceed 1.2 V, the signal should be attenuated using a resistor divider network.

When digitizing with a full-scale range less than 0.7 V, the Bt254's integral linearity errors are constant in terms of voltage, regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

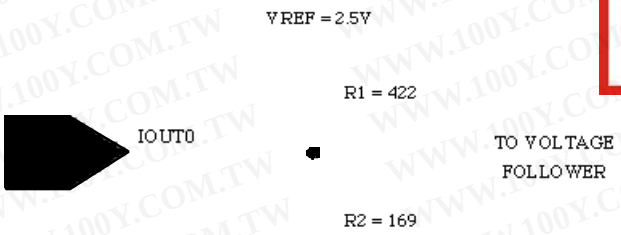


Figure 5. Increasing DAC Output Resolution.

For example, by setting the reference difference to 0.6 V, 0.6 V video signals may be digitized. However, the integral linearity error will increase to about ±1.8 LSB and the SNR will be about 40 db. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB and the SNR will be about 39 db.

Output Noise

Although the A/D does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

The output noise of the A/D may be reduced by adjusting the duty cycle of the clock—this is especially true above 10 MHz clock operation. Note that uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2 inch VCR.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 643066-2.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat “leaky” inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid ADC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

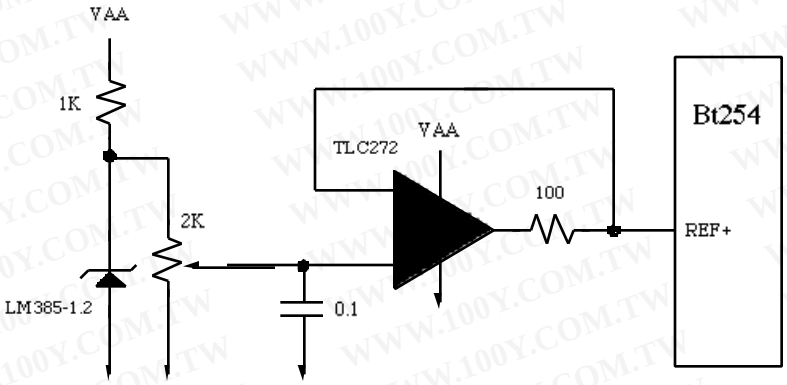


Figure 6. Using an External Reference.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/ sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 3. Video Signal Tolerances.

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Voltage References					
Top	xREF+	0.7	1	2.0	V
Bottom	xREF–	0	0	1.3	V
Difference (Top–Bottom)		0.7	1	1.2	V
VID0–VID1 Amplitude Range		0.5		VAA–0.5	V
Multiplexer Compliance (DC)		–0.2		+2.2	V
(R,G,B) IN Amplitude Range		0.7	1	1.2	V
(R,G,B) IN Input Range			REF– to REF+		V
CEXT AC Amplitude		0.2 Vp–p		2.0 Vp–p	V
(R,G,B) LEVEL Input Voltage		GND–0.5	REF–	REF+	V
Zeroing Interval			60	150	µs
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	V
Analog Input Voltage	VIN, VIDx	GND–0.5		VAA + 0.5	V
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (Note 1)	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
A/D Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C
A/D to A/D Matching			tbd		%
A/D Coding (Table 4)					Binary
No Missing Codes			guaranteed		
(R,G,B) IN Inputs (Note 2)					
CLAMP = 0					
Input Impedance	RIN	10			MΩ
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
(R,G,B) VID0,1 Inputs (Note 3)					
Input Impedance to (R,G,B) OUT					
Input Selected			100		Ω
Input Deselected			10		MΩ
Input Capacitance			tbd		pF
(R,G,B) REF+ Reference Inputs					
Input Current			1		mA
Input Impedance			500		Ω
Clock Kickback (Note 4)			tbd		pV - sec
Digital Inputs					
Input High Voltage	VIH	2.0			V
Input Low Voltage	VIL			0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
RGB (0–7) Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
CSYNC* Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Output Capacitance	COUT		10		pF

See test conditions on next page.

Parameter	Symbol	Min	Typ	Max	Units
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0–IOUT5 Outputs					
DAC Output Current		0		2.5	mA
DAC Output Impedance			100		kΩ
DAC Output Capacitance			20		pF
DAC Output Compliance		–0.2		+1.2	V
DAC Accuracy					
Differential Linearity Error	DL			tbd	LSB
Integral Linearity Error	IL			tbd	LSB
Monotonicity			guaranteed		
A/D Power Supply Rejection Ratio (f = 1 kHz)	PSRR		tbd		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1 V and (R,G,B)REF– = GND. REF– ≤ Vin ≤ REF+, (R,G,B) LEVEL = float. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Best-fit linearity (offset independent). Averaged value evaluated using a closed loop system.
Note 2: (R,G,B)LEVEL = GND.
Note 3: ROUT, GOUT, BOUT connected to GND.
Note 4: Measurement of noise coupled onto RIN, GIN, and BIN due to clocking (Rs = 75 Ω). Typically occurs over a 5-ns interval.

Vin* (V)	(R,G,B) 0–7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

*With (R,G,B)REF+ = 1.000 V and (R,G,B)REF– = 0.000 V. Ideal center values.
1 LSB = 3.9063 mV.

Table 4. A/D Coding Example.

		30 MHz Devices			20 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Conversion Rate	Fs			30			30	MHz
Multiplexer Switching Time	Tmux		100			100		ns
Clock Cycle Time Clock Low Time Clock High Time	1 2 3	33.3 12 12			33.3 12 12			ns ns ns
R,G,B(0–7) Output Delay Time R,G,B(0–7) Output Hold Time OE* Asserted to Pixel Data Valid OE* Negated to Pixel Data 3-Stated	4 5 6 7	tbd		15 20 20	tbd		40 20 20	ns ns ns ns
ZERO Setup Time ZERO Hold Time ZERO, CLAMP High Time (Note 1)	8 9	0 20 1			0 20 1			ns ns Clock
Aperture Delay Aperture Jitter Full Power Input Bandwidth	10 BW		10 50	 Fs / 2		10 50	 6	ns ps MHz
Transient Response (Note 2) Overload Recovery (Note 3) Zero Recovery Time (Note 4)				1 1 1			1 1 1	Clock Clock Clock
RMS Signal to Noise Ratio Fin = 4.2 MHz, Fs = 14.32 MHz Fin = 2.75 MHz, Fs = 6.75 MHz Fin = 5.75 MHz, Fs = 13.5 MHz Fin = 4.2 MHz, Fs = 17.72 MHz Fin = 15 MHz, Fs = 30 MHz	SNR		 tbd tbd tbd tbd tbd			 tbd tbd tbd tbd tbd		 db db db db db
Analog Multiplexer Crosstalk All Hostile Crosstalk (Figure 7) Single Channel Crosstalk (Figure 8) Adjacent Input Crosstalk (Figure 9)			 –50 –50 –50			 –50 –50 –50		 db db db
IOUT0, IOUT5 Settling Time to ±1 LSB			100			100		ns
Differential Gain Error (Note 5) Differential Phase Error (Note 5)	DG DP		2 1			2 1		% Degree
Supply Current (Note 6) (Excluding REF+)	IAA		tbd	tbd		tbd	tbd	mA

See test conditions on next page.

Parameter	Symbol	Min	Typ	Max	Units
A0–A2 Setup Time	11	10			ns
A0–A2 Hold Time	12	10			ns
RD*, WR* High Time	13	50			ns
RD* Asserted to Data Bus Driven	14	5			ns
RD* Asserted to Data Valid	15			40	ns
RD* Negated to Data Bus 3-Stated	16			20	ns
WR* Low Time	17	70			ns
Write Data Setup Time	18	10			ns
Write Data Hold Time	19	10			ns
Pipeline Delay (Note 7)		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1 V and (R,G,B)REF– = GND. REF– ≤ Vin ≤ REF+, (R,G,B) LEVEL = float. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0–D7 output load ≤ 75 pF. CSYNC*, R0–R7, G0–G7, and B0–B7 output load ≤ 75 pF. ROUT, GOUT, BOUT, IOUT0–IOUT5 output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V. See timing waveforms (Figures 10 and 11).

Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.25 V, Fin = 15 MHz, Fs = 30 MHz.
Note 7: Pipeline delay is defined as discrete clock period delays in addition to the half cycle sampling delays.

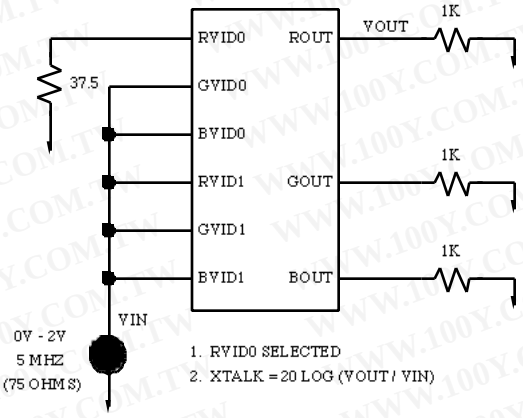


Figure 7. All Hostile Crosstalk Test Circuit.

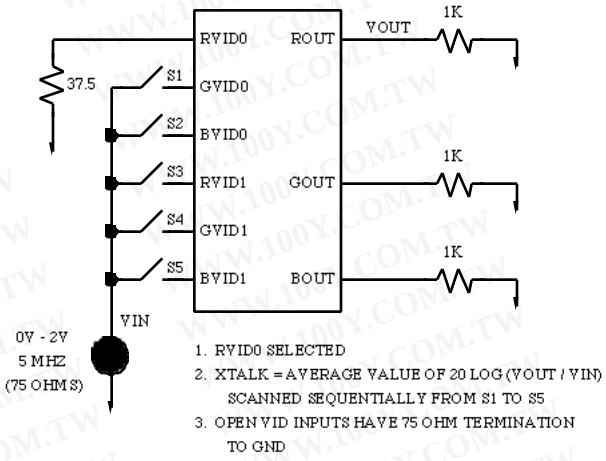


Figure 8. Single Channel Crosstalk Test Circuit.

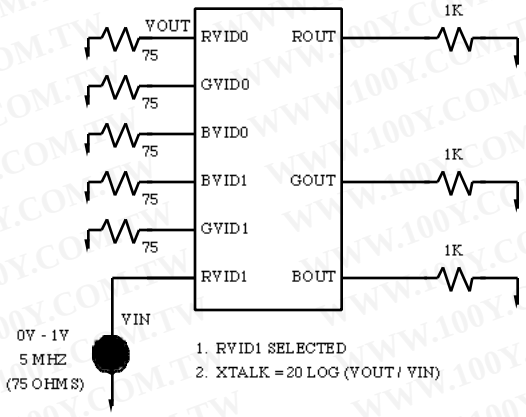


Figure 9. Adjacent Input Crosstalk Test Circuit.

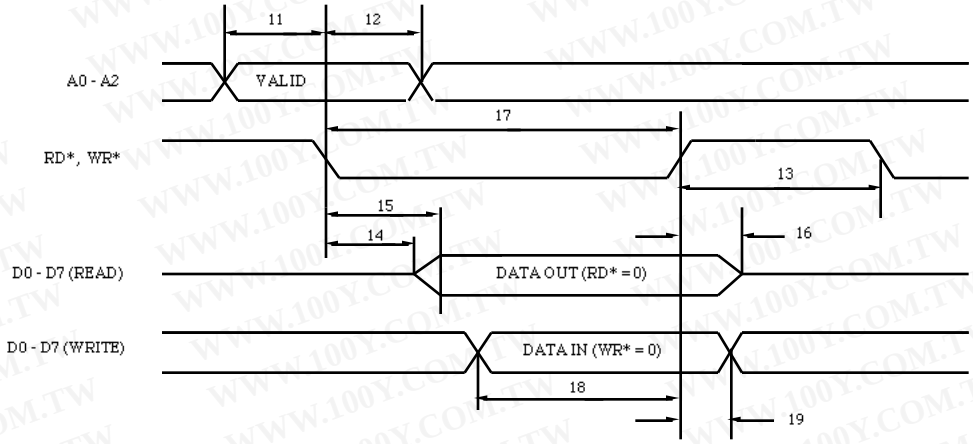


Figure 10. MPU Read/Write Timing.

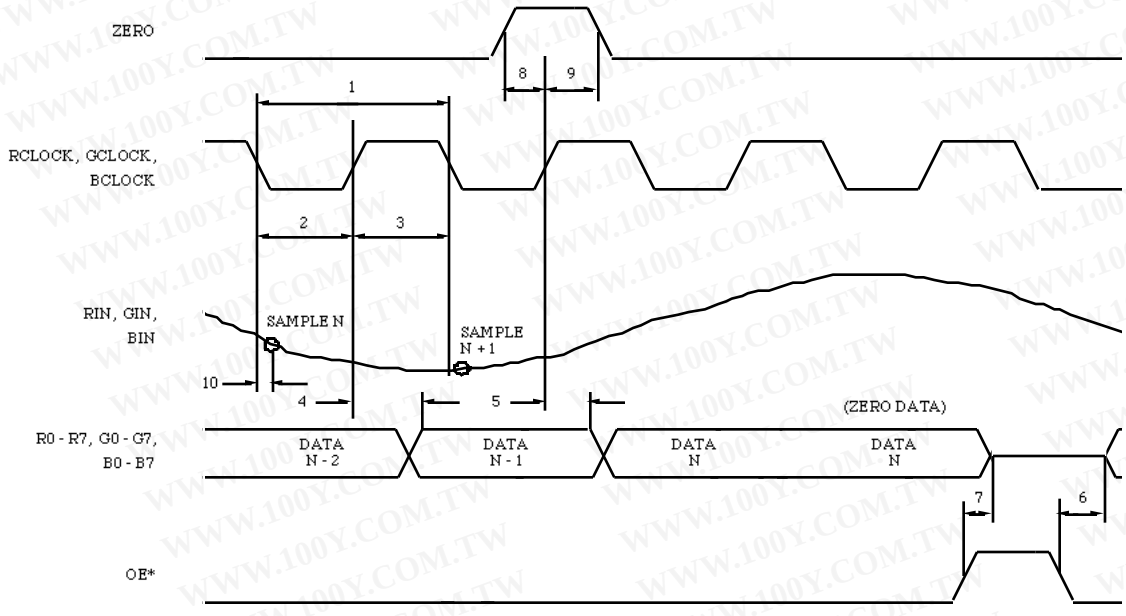
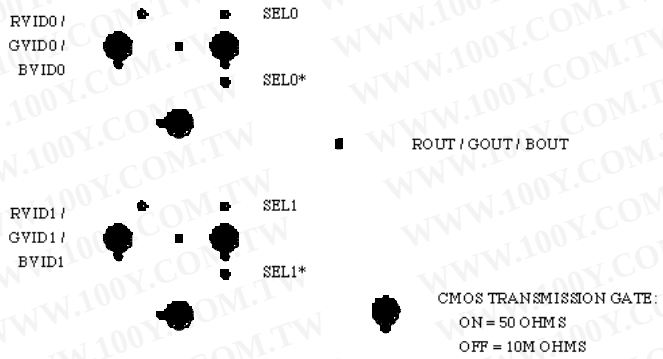


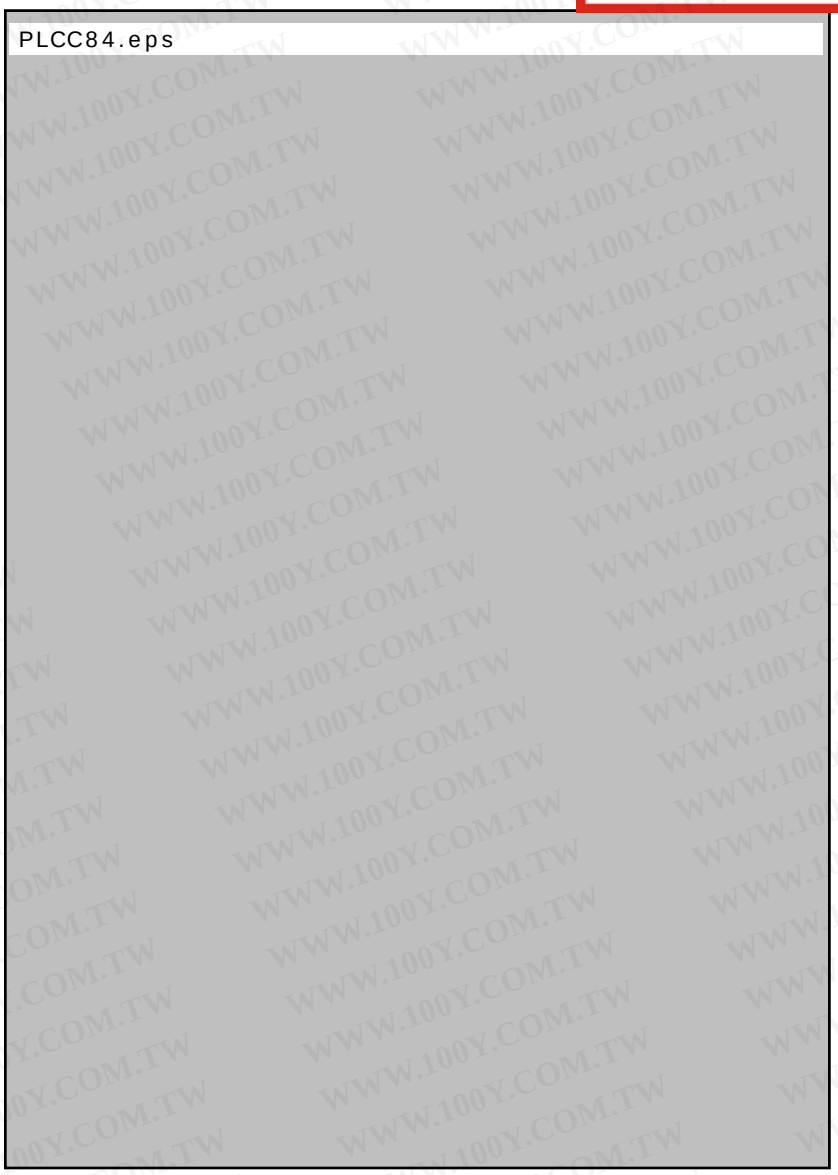
Figure 11. Video Input/Output Timing.



Revision	*Change from Previous Revision*
B	General Operation section and Figure 2 added. Description of DAC operation changed to indicate 8-bit resolution. New diagram for "Using an External Reference" (Figure 5). Expanded discussion of AC coupling. WR* low time changed to 70 ns. REF+ input impedance changed to 500 Ω. For 20 MHz part: Digital Output Delay changed to 40 ns. Maximum input bandwidth changed to 6 MHz.

Model Number	Speed	Package	Ambient Temperature Range
Bt254KPJ30	30 MHz	84-pin Plastic J-Lead	0° to +70° C
Bt254KPJ20	20 MHz	84-pin Plastic J-Lead	0° to +70° C
Bt254EVM	Evaluation Board for the Bt254. Includes a Bt254KPJ30.		

Package Drawing—84–pin Plastic J-Lead (PLCC)



NOTES: Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

CAUTION

ESD sensitive device. Permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
Do not insert this device into powered sockets.
Remove power before insertion or removal.

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