Development Board EPC9150 Quick Start Guide

EPC2034C

200 V High Current Pulsed Laser Diode Driver

Revision 2.0

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EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9150 demonstration board is primarily intended to drive laser diodes with high current pulses with total pulse widths of < 3 ns possible (half amplitude full width). The board is shipped with a EPC2034C enhancement mode (eGaN®) field effect transistor (FET). The EPC2034C is a 200 V FET capable of current pulses up to 214 A. The EPC9150 ships with the EPC9989 interposer board. The EPC9989 has a collection of break-away 5 mm square interposer PCBs with footprints for different lasers and a collection of other footprints. The use of the interposers allows many different lasers or other loads to be mounted while still being able to use the EPC9150. The boards do not include a laser diode or load, which must be supplied by the user.

The power stage of the EPC9150 comprises a ground-referenced eGaN FET driven by a Texas Instruments LMG1020 gate driver. The printed circuit board is designed to minimize the power loop inductance while maintaining mounting flexibility for the laser diode or other load. It includes multiple on-board passive probes for voltages and discharge capacitor current, and is equipped with high bandwidth SMA connectors for input and sensing. In addition, the board includes a narrow pulse generator capable of sub-nanosecond precision, or the user can simply send the input to the gate drive directly. As shipped, the board is designed to operate from 3.3 V logic, but is equipped with both a logic level translator and a differential receiver to accommodate different use cases. Finally, the board can also be used for other applications requiring a ground-referenced eGaN FET, e.g. Class E amplifiers or similar. A complete block diagram of the circuit is given in Figure 1, and a detailed schematic in Figures 7, 8, and 9.

For more information on the EPC2034C eGaN FET, please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide. In addition, EPC provides an application note: ***AN027 eGaN FETs for Lidar – Getting the Most Out of the EPC9126 Laser Driver***. While the note discusses Rev. 2 of the EPC9126, most of the methods and analysis are applicable to the EPC9150.

Table 1: Performance Summary (T_A = 25°C) EPC9150

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{Logic}	Gate drive and logic supply		5.5		12	V
V_{BUS}	Bus Input Voltage Range		0		160	
Z_{IN}	Input impedance			50		Ω
V_{INPUT}	Input pulse range		0		5	V
T_{Pin}	Input pulse width		1			ns

LASER SAFETY WARNING: This board is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

QUICK START PROCEDURE

The EPC9150 demonstration board is easy to set up to evaluate the performance of the EPC2034C eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. **Review laser safety considerations. Observe all necessary laser safety requirements including the use of personal protection equipment (PPE) as required. Refer to qualified safety personnel as necessary.**
2. With power off, install laser diode U2 or other load. The use of one of the interposers from the included EPC9989 be used to mount the laser or other load, and this is discussed in the section **LASER DIODE OR LOAD CONSIDERATIONS**.
3. With power off, connect the input power supply bus to $+V_{BUS}$ (J11) and ground / return to $–V_{BUS}$ (J11) or GND.
4. With power off, connect the logic supply (5.5-12 V_{DC}) to $+V_{Logic}$ (J10) and ground return to $–V_{Logic}$ (J10) or GND.
5. With power off, connect the signal pulse generator to the input J7. J7 is terminated with 50 Ω on the EPC9150, and is designed for a 3.3 V logic input as shipped. This can be changed as discussed in Section **OTHER FEATURES** of this guide.
6. Connect the remaining measurement SMA outputs to an oscilloscope, using 50 Ω cables and with the scope inputs set to 50 Ω impedance. See section **MEASUREMENT CONSIDERATIONS** for more information, including the attenuation values for each output.
7. Turn on the logic supply voltage to a value within the specifications.
8. Turn on the bus voltage to a value within the specification.
9. Turn on the pulse source and observe switching operation via the outputs and any additional desired probing. Laser diode output may be observed with an appropriate electro-optical receiver.
10. Once operational, adjust the bus voltage, input pulse width, and pulse repletion frequency (PRF) as desired within the operating range and observe the system behavior.
11. For shutdown, please follow steps in reverse.

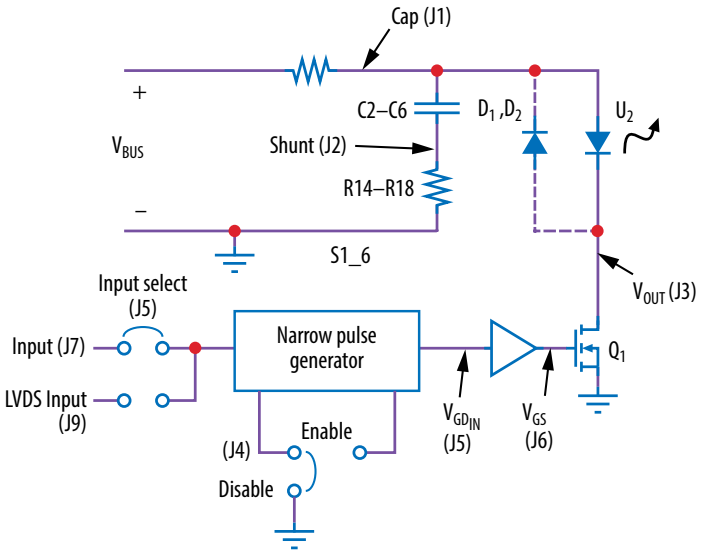

Figure 1: Block diagram of EPC9150 development board

OPERATING PRINCIPLE

The EPC9150 is intended as both a demonstration board and a flexible development platform. It is functional out of the box, but is designed to be easily modified to accommodate a broad range of applications. ***It is highly recommended that the user read the entire guide, but especially the section OTHER FEATURES, in order to get maximum value from the EPC9150.***

The EPC9150 is shipped as a capacitive discharge laser diode driver. Please refer to the block diagram (figure 2) and the schematic (figure 4). It has several possible modifications (section **OTHER FEATURES**), but only the basic operation will be covered in this section. The EPC9150 basic operating principle is to discharge energy storage capacitance {C2, C3, C4, C5, C6} through the laser diode, and then recharge {C2, C3, C4, C5, C6} through the resistor bank {R1, R3, R6, R7} and ferrite beads {FB1, FB2}. As shipped, it is designed to generate resonant half-sine current pulses when used with modern surface mount lasers. The discharge capacitance and the parasitic power loop inductances form the resonant network. Please see ***AN027 eGaN FETs for Lidar – Getting the Most Out of the EPC9126 Laser Driver*** for more information.

The discharge pulse can be controlled from two different inputs. As shipped, it is controlled via an input pulse that is delivered to SMA connector J7, which is terminated on the demo board with 50 Ω. Input J7 feeds a level translator U5, and the output of the level translator is passed to an input select jumper. This pulse PLS_IN is delivered to gate driver U3 through the narrow pulse generator (NPG). When the input goes high, the gate driver turns on Q1, allowing {C2, C3, C4, C5, C6} to discharge through the laser diode U2. If the NPG is disabled, then when the input goes low, Q1 turns off. If there is current remaining in the power loop, optional diodes D1-D5 can conduct and help prevent overvoltage of the laser and FET. If the NPG is enabled, the user can get a short output pulse to the lower limit of the gate drive IC U3's capability. This allows the use of lower cost signal generators while working with the EPC9150. Details are given in Section **OTHER FEATURES**.

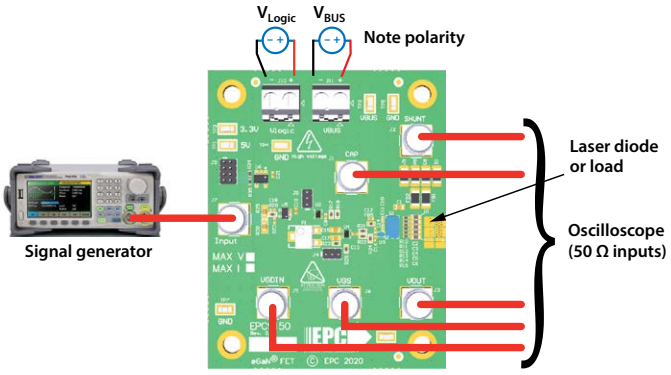

Figure 2: Connection and measurement setup

The alternate input for LVDS systems is provided via J9, which provides an LVDS-compatible input. This will be discussed in the Section **OTHER FEATURES**. J9 may also be used to supply the input logic supply V_{Logic}, and it makes the EPC9150's V3V3 (3.3 V) and V5V0 (5.0 V) regulator outputs available to the end user.

Measurements of many of the main waveforms can be made through the SMA test points provided. These test points can provide waveform measurements with equivalent bandwidths > 3 GHz. As a result, they have requirements and properties that differ from most conventional oscilloscope probes. More details on the usage of these test points is provided in section **MEASUREMENT CONSIDERATIONS**.

For further details on lidar driver circuits, it is recommended to read the application note ***"Getting the Most out of eGaN FETs and Your EPC9150 Laser Driver"*** (AN027), available at www.epc-co.com. While this application note refers to V2.5 of the EPC9150, the basic principles and design methods are still applicable.

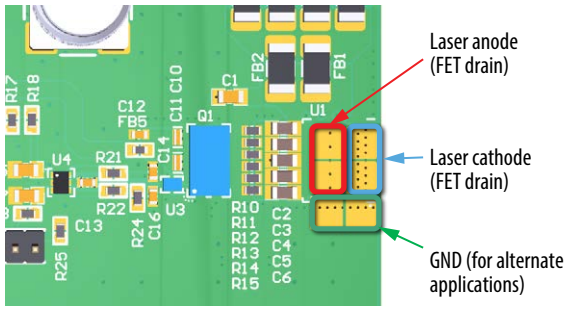

Figure 3: Output terminals of EPC9150

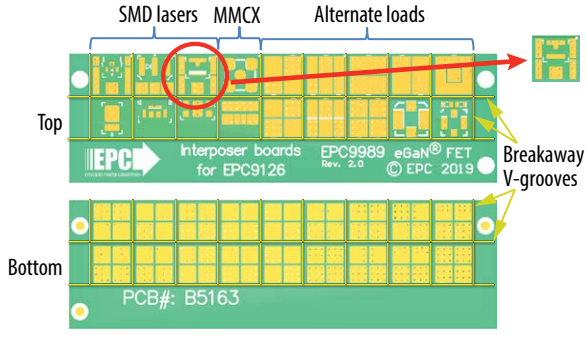

Figure 4: EPC9989 interposer PCB for mounting different lasers and loads

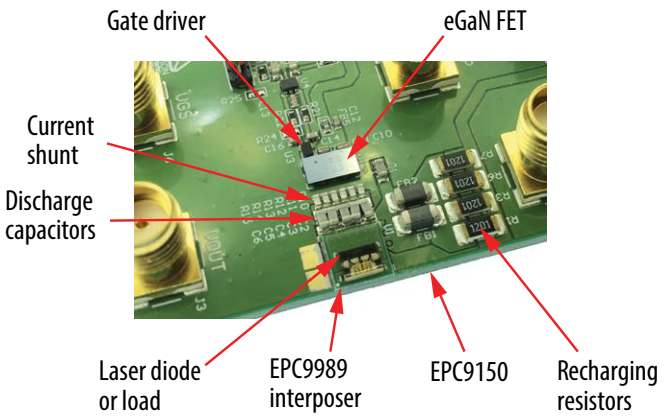

Figure 5: Laser mounted with EPC9989 interposer

LASER DIODE OR LOAD CONSIDERATIONS

The EPC9150 can be used as is to mount a laser diode or other load. Figure 3 highlights the output pad locations. However, many laser suppliers have different mounting footprints, making it difficult to optimize the performance of the driver and still maintain the desired flexibility. The use of an interposer PCB provides a solution to this problem with only a small added performance penalty. The EPC9150 Rev. 2 ships with the EPC9989 interposer PCB, shown in Figure 4. The EPC9989 has an assortment of 5 mm square interposer PCBs that can be snapped off the board. These interposers have various footprints on the top side that can accommodate several surface mount laser diodes, an MMCX connector, and several patterns designed to accommodate a wide variety of possible loads. These interposers mount between the EPC9150 and the laser diode or other load. Figure 5 shows an example of a quad laser SMD package mounted with one of the interposers.

The recommended use of the interposer is the following:

1. Apply solder paste to the U2 pads on the EPC9150 PCB.
2. Apply solder paste to the appropriate pads on the top side of the interposer.
3. Carefully position the desired interposer with the bottom side facing the top side of the EPC9150 on the U2 footprint.
4. Place the laser diode or desired load on the interposer.
5. Reflow with the recommended temperature profile for the solder used. The use of a reflow oven that can meet the recommended soldering specifications is highly recommended. Other reflow methods may also be used based on the experience of the user.

The power loop inductance, including that of the laser diode, is a primary factor that determines the shape of the laser pulse. Considerable effort has been made to minimize power loop inductance while maximizing the choice of laser diode and its orientation. The discharge caps, current sense resistors, and the eGaN FET must all be mounted in close proximity to minimize inductance. As a result, the user must take care not to damage any components when mounting the laser or changing other components in the power loop.

Laser diode current pulses can result in peak powers of several hundred watts to over 1 kW. Laser diodes for lidar applications are designed with this in mind, but thermal limitations of the laser package mean that pulse widths, duty cycles, and pulse repetition frequency limitations must be observed. Read laser diode data sheets carefully and follow any manufacturers' recommendations.

MEASUREMENT CONSIDERATIONS

SMA jacks are provided to measure several voltages in the circuit, including gate drive IC input, Q1 gate voltage, Q1 drain voltage, charge voltage of the energy storage cap, and the sense voltage of the discharge cap current measurement shunt. All measurement points are designed to be terminated in 50 Ω, hence when viewing waveforms, the oscilloscope inputs should be set to a 50 Ω input. Ideally, unused inputs should be also terminated with a 50 Ω load to prevent the probes from creating additional resonances. The Q1 drain voltage and the discharge cap sense voltage have on-board terminations to greatly reduce this effect, and in practice, the remaining resonances may be small or otherwise tolerable. It is recommended that the user verify this for their own requirements.

All sense measurement SMA connectors, except for the shunt measurement, use the transmission line voltage probe principle to obtain waveform fidelity at sub-ns time scales. They have been verified to produce near-identical results to a Tektronix P9158 3 GHz transmission line probe. As a result of their design, they have a built-in attenuation factor. The impedance of the probes at the measurement node is relatively small (~ 1 kΩ to 2 kΩ). In order to minimize the effects of the low probe impedance on the operation of the demo board and prevent overheating of the probe input resistors, the output voltage (J3) and capacitor voltage (J1) probes have DC blocking capacitors on the PCB. As a result, measured pulse waveforms will exhibit droop as pulse widths and other waveform features approach the RC time constant of the probe. The user should keep these factors in mind if accustomed to more conventional oscilloscope probes. If long pulse widths are used, the droop will become substantial, and an external probe may be used to measure these slower waveforms.

Table 2: Key properties of SMA test points

Designator	PCB label	Description	Attenuation factor	DC blocking cap	LF time constant	Internal 50 Ω termination
J1	CAP	Discharge capacitor voltage (VCHARGE on schematic)	81 V/V	2.2 nF	4.4 µs	YES
J2	SHUNT	Discharge shunt voltage	120 A/V	NO	N/A	NO
J3	V_{OUT}	Q1 drain voltage	81 V/V	2.2 nF	4.4 µs	YES
J5	$V_{GD_{IN}}$	Gate drive IC input sense	20	NO	N/A	NO
J6	V_{GS}	Q1 gate voltage	20	NO	N/A	NO

The current shunt is designed to estimate the discharge capacitor current. Substantial effort has been made to reduce the inductive effects of the current shunt, both through the use of carefully selected resistors and a compensation network to help compensate for the shunt equivalent series resistance. However, the shunt is a compromise between current measurement accuracy and minimizing the impact on the laser driver performance. If a more accurate shunt waveform measurement is desired, the shunt resistors may be replaced with ones that provide higher accuracy at the bandwidth required. This will require higher resistor values which will contribute to errors in the capacitor voltage measurement and increase power dissipation. Finally, note that the capacitor current also includes the current due to D1-D5 (if included), and PCB capacitance.

Table 2 summarizes the properties of the SMA test points for ease of reference.

OTHER FEATURES

Narrow pulse generator:

Many signal generators cannot produce an accurate, short pulse. The EPC9150 includes a narrow pulse generator (NPG) function to obtain narrow output pulses of adjustable width, following a method given in Section 8.2.2.2 of the Texas Instruments LMG1020 data sheet. This is controlled through Potentiometer P1.

The NPG is enabled by moving the jumper on J4 to the leftmost position. With the NPG enabled, the input pulse signal is split into separate turn-on and turn-off paths. See Figure 6. The turn-on path goes through buffer U2, a fixed RC delay {R18, C15} and buffer U4 on to the IN+ (non-inverting) input of gate driver U3, which turns output Q1 on. The turn-off path is similar, but has an adjustable RC delay {P1, R23, C17}. This delayed pulse is sent to the IN- (inverting) input of U3. The longer delay of the second path means that after some interval, the IN- input of U3 goes high, and Q1 is turned off, ending the output pulse. Potentiometer P1 is used to adjust this turn-off delay and the resulting output pulse width. Note that the minimum delay setting causes both turn-on and turn-off paths to have an approximately equal delay, which would result in a zero-width pulse. Since the gate driver U3 has a minimum pulse width specification of > 1 ns, it is U3 that determines the minimum attainable output pulse width. Small errors in the delay path do not significantly impact the output. The maximum pulse width that can be obtained with the NPG is approximately 20 ns.

When using the NPG, the input pulse should be at least 10 ns longer than the desired output pulse. If possible, an input pulse of 40 ns will allow sufficient margin to adjust the NPG over its full range without requiring additional adjustments beyond P1.

LVDS input:

The EPC9150 has the option to be controlled via an LVDS input. This input is available to the user through the 8-pin header J9. Please consult the schematic (Figure 7) for the pinout. In order to enable the LVDS input, move the jumper on J4 to the upper position (Figure 6).

Modifications:

Space is left on the EPC9150 to mount clamp diodes (D1-D5). While diodes can provide some protection to FET Q1 and laser D3, they have parasitic inductance and capacitance that can reduce performance at the very fastest speeds. Hence, they are not populated, and it is left to the user to determine whether they are necessary for a particular application.

The value of the shunt resistors can be increased up to a point to improve the discharge cap current sense accuracy. This will require a change in shunt compensation capacitor C7 to accommodate the changes in resistance and inductance. Note that accurate measurement of current while inserting extremely low inductance into the power loop is extremely challenging, and many factors must be considered. For the lowest possible inductance, the resistors can be replaced with copper foil if no sensing is needed.

The value of the energy storage cap {C2, C3, C4, C5, C6} can be modified as desired, as well as the recharge resistor {R1, R3, R6, R7}. In the extreme case, the resistor may be reduced to 0 Ω for cases where a capacitive discharge pulse is not desired.

The input logic level can be reduced from 3.3 V logic to 2.5 V or 1.8 V by changing R31. Please see the U5 datasheet for further details.

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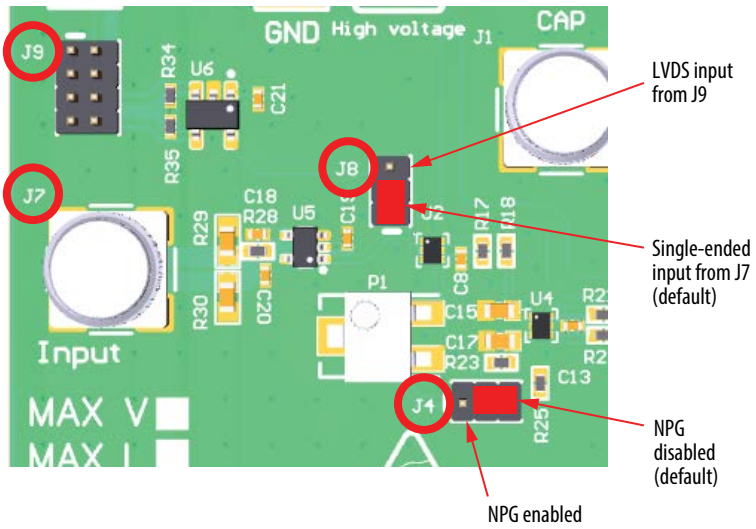

Figure 6. Jumper locations to control input and pulse settings

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9150 landing page at: https://epc-co.com/epc/Products/DemoBoards/EPC9150.aspx