# 300V, 64-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

## Ordering Information

| Device | Recommended Operating $V_{PP}$ Max* | Package Options | |
|---|---|---|---|
| | | 80-Lead Plastic Gullwing | Die |
| HV507 | 300V | HV507PG | HV507X |

* Please consult factory for higher voltage operation.

## Features

- HVCMOS® technology
- Operating output voltage of 300V
- Low power level shifting from 5V to 300V
- Shift register speed 8MHz @ $V_{DD}$ = 5V
- 64 latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

## General Description

The HV507 is a low voltage serial to high voltage parallel converter with 64 high voltage push-pull outputs. This device has been designed for use as a printer driver for electrostatic applications. It can also be used in any application requiring multiple high voltage outputs, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, $D_{IO4}$ is Data In and $D_{IO8}$ is Data Out; data is shifted from $HV_{OUT}$64 to $HV_{OUT}$1. When DIR is at logic high, $D_{IO8}$ is Data In and $D_{IO4}$ is Data Out: data is then shifted from $HV_{OUT}$1 to $HV_{OUT}$64. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$, $\overline{BL}$, or the $\overline{POL}$ inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

## Absolute Maximum Ratings[1]

| | |
|---|---|
| Supply voltage, $V_{DD}$ | -0.5V to +6V |
| Supply voltage, $V_{PP}$ | $V_{DD}$ to 320V |
| Logic input levels | -0.5V to $V_{DD}$ +0.5V |
| Ground current[3] | 0.5A |

## Electrical Characteristics (for $V_{DD}$ = 5V, $V_{PP}$ = 300V, $T_A$ = 25ºC)

### DC Characteristics

| Symbol | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ supply current | | | | 15 | mA | $f_{CLK}$ = 8MHz, $f_{DATA}$ = 4MHz<br>$\overline{LE}$ = LOW |
| $I_{DDQ}$ | Quiescent $V_{DD}$ supply current | | | | 200 | µA | All $V_{IN}$ = 0V or $V_{DD}$ |
| $I_{PP}$ | High voltage supply current | | | | 0.50 | mA | $V_{PP}$ = 300V All outputs high |
| | | | | | 0.50 | mA | $V_{PP}$ = 300V All outputs low |
| $I_{IH}$ | High-level logic input current | | | | 10 | µA | $V_{IH}$ = $V_{DD}$ |
| $I_{IL}$ | Low-level logic input current | | | | -10 | µA | $V_{IL}$ = 0V |
| $V_{OH}$ | High-level output | $HV_{OUT}$ | 265 | | | V | $V_{PP}$ = 300V, $IHV_{OUT}$ = -1mA |
| | | Data out | $V_{DD}$ -1V | | | V | $ID_{OUT}$ = -100µA |
| $V_{OL}$ | Low-level output | $HV_{OUT}$ | | | 35 | V | $V_{DD}$ = 5V, $IHV_{OUT}$ = 1mA |
| | | Data out | | | 1.0 | V | $ID_{OUT}$ = 100µA |
| $V_{OC}$ | $HV_{OUT}$ clamp voltage | | | | $V_{PP}$ +1.5 | V | $I_{OC}$ = 1mA |
| | | | | | -30 | V | $I_{OC}$ = -1mA |

### AC Characteristics[1] (For $V_{DD}$ = 5V, $V_{PP}$ = 300V, $T_A$ = 25°C)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $f_{CLK}$ | Clock frequency | | | 8 | MHz | |
| $t_W$ | Clock width high and low | 62 | | | ns | |
| $t_{SU}$ | Data setup time before clock rises | 35 | | | ns | |
| $t_H$ | Data hold time after clock rises | 30 | | | ns | |
| $t_{WLE}$ | Width of latch enable pulse | 80 | | | ns | |
| $t_{DLE}$ | $\overline{LE}$ delay time after rising edge of clock | 35 | | | ns | |
| $t_{SLE}$ | $\overline{LE}$ setup time before rising edge of clock | 40 | | | ns | |
| $t_{ON}$, $t_{OFF}$ | Time from latch enable to $HV_{OUT}$ | | | 4 | µs | $C_L$ = 20pF |
| $t_{DHL}$ | Delay time clock to data out high to low | | | 125 | ns | $C_L$ = 20pF |
| $t_{DLH}$ | Delay time clock to data out low to high | | | 125 | ns | $C_L$ = 20pF |
| $t_r$, $t_f$ | All logic inputs | | | 5 | ns | |

**Note:**
1. Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Logic supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{PP}$ | High voltage supply | 60 | | 300 | V |
| $V_{IH}$ | High-level input voltage | $V_{DD}$ -0.9 | | $V_{DD}$ | V |
| $V_{IL}$ | Low-level input voltage | 0 | | 0.9 | V |
| $T_A$ | Operating free-air temperature | 0 | | +70 | °C |

**Notes:**
Power-up sequence should be the following:
1. Connect ground.
2. Apply $V_{DD}$.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply $V_{PP}$.
5. The $V_{PP}$ should not drop below $V_{DD}$ or float during operation.

Power-down sequence should be the reverse of the above.

## Function Table

| Function | Inputs | | | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Data | CLK | $\overline{LE}$ | $\overline{BL}$ | $\overline{POL}$ | DIR | Shift Reg 1 | Shift Reg 2…64 | HV Outputs 1 | HV Outputs 2…64 | Data Out |
| All on | X | X | X | L | L | X | * | *…* | H | H…H | * |
| All off | X | X | X | L | H | X | * | *…* | L | L…L | * |
| Invert mode | X | X | L | H | L | X | * | *…* | $\overline{*}$ | $\overline{*}$…$\overline{*}$ | * |
| Load S/R | H or L | ↑ | L | H | H | X | H or L | *…* | * | *…* | * |
| Store data in latches | X | X | ↓ | H | H | X | * | *…* | * | *…* | * |
| | X | X | ↓ | H | L | X | * | *…* | $\overline{*}$ | $\overline{*}$…$\overline{*}$ | * |
| Transparent latch mode | L | ↑ | H | H | H | X | L | *…* | L | *…* | * |
| | H | ↑ | H | H | H | X | H | *…* | H | *…* | * |
| I/O relation | $D_{IOA}$ | ↑ | X | X | X | L | $Q_n \rightarrow$ | $Q_{n+1}$ | — | | $D_{IOB}$ |
| | $D_{IOB}$ | ↑ | X | X | X | H | $Q_n \rightarrow$ | $Q_{n+1}$ | — | | $D_{IOA}$ |

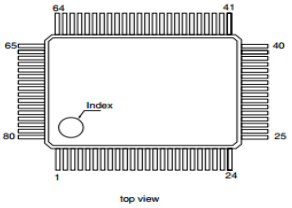
**Notes:**
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

## Pin Configurations

**HV507**
**80 Pin Gullwing Package**

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | $HV_{OUT}$ 41 | 41 | $HV_{OUT}$ 1 |
| 2 | $HV_{OUT}$ 42 | 42 | $HV_{OUT}$ 2 |
| 3 | $HV_{OUT}$ 43 | 43 | $HV_{OUT}$ 3 |
| 4 | $HV_{OUT}$ 44 | 44 | $HV_{OUT}$ 4 |
| 5 | $HV_{OUT}$ 45 | 45 | $HV_{OUT}$ 5 |
| 6 | $HV_{OUT}$ 46 | 46 | $HV_{OUT}$ 6 |
| 7 | $HV_{OUT}$ 47 | 47 | $HV_{OUT}$ 7 |
| 8 | $HV_{OUT}$ 48 | 48 | $HV_{OUT}$ 8 |
| 9 | $HV_{OUT}$ 49 | 49 | $HV_{OUT}$ 9 |
| 10 | $HV_{OUT}$ 50 | 50 | $HV_{OUT}$ 10 |
| 11 | $HV_{OUT}$ 51 | 51 | $HV_{OUT}$ 11 |
| 12 | $HV_{OUT}$ 52 | 52 | $HV_{OUT}$ 12 |
| 13 | $HV_{OUT}$ 53 | 53 | $HV_{OUT}$ 13 |
| 14 | $HV_{OUT}$ 54 | 54 | $HV_{OUT}$ 14 |
| 15 | $HV_{OUT}$ 55 | 55 | $HV_{OUT}$ 15 |
| 16 | $HV_{OUT}$ 56 | 56 | $HV_{OUT}$ 16 |
| 17 | $HV_{OUT}$ 57 | 57 | $HV_{OUT}$ 17 |
| 18 | $HV_{OUT}$ 58 | 58 | $HV_{OUT}$ 18 |
| 19 | $HV_{OUT}$ 59 | 59 | $HV_{OUT}$ 19 |
| 20 | $HV_{OUT}$ 60 | 60 | $HV_{OUT}$ 20 |
| 21 | $HV_{OUT}$ 61 | 61 | $HV_{OUT}$ 21 |
| 22 | $HV_{OUT}$ 62 | 62 | $HV_{OUT}$ 22 |
| 23 | $HV_{OUT}$ 63 | 63 | $HV_{OUT}$ 23 |
| 24 | $HV_{OUT}$ 64 | 64 | $HV_{OUT}$ 24 |
| 25 | $V_{PP}$ | 65 | $HV_{OUT}$ 25 |
| 26 | $D_{IOA}$ | 66 | $HV_{OUT}$ 26 |
| 27 | N/C | 67 | $HV_{OUT}$ 27 |
| 28 | N/C | 68 | $HV_{OUT}$ 28 |
| 29 | $\overline{BL}$ | 69 | $HV_{OUT}$ 29 |
| 30 | $\overline{POL}$ | 70 | $HV_{OUT}$ 30 |
| 31 | $V_{DD}$ | 71 | $HV_{OUT}$ 31 |
| 32 | DIR | 72 | $HV_{OUT}$ 32 |
| 33 | GND | 73 | $HV_{OUT}$ 33 |
| 34 | HVGND | 74 | $HV_{OUT}$ 34 |
| 35 | N/C | 75 | $HV_{OUT}$ 35 |
| 36 | N/C | 76 | $HV_{OUT}$ 36 |
| 37 | CLK | 77 | $HV_{OUT}$ 37 |
| 38 | $\overline{LE}$ | 78 | $HV_{OUT}$ 38 |
| 39 | $D_{IOB}$ | 79 | $HV_{OUT}$ 39 |
| 40 | $V_{PP}$ | 80 | $HV_{OUT}$ 40 |

## Package Outline




top view

80-pin Gullwing Package