

DESCRIPTION

The PT5619 is a high-speed 3-phase gate driver for power MOSFET and IGBT devices with three independent high and low side referenced output channels. Built-in dead time protection and shoot-through protection prevent damage to the half-bridge. The UVLO circuits prevent malfunction when VCC and VBS are lower than the specified threshold voltage. A novel high-voltage BCD process and common-mode noise canceling technique provide stable operation of high-side drivers under high dV/dt noise conditions while achieving excellent negative transient voltage tolerance. An enable pin (ENB) is included so that standby mode may be used to set the chip into a low quiescent current state to realize long battery lifetime.

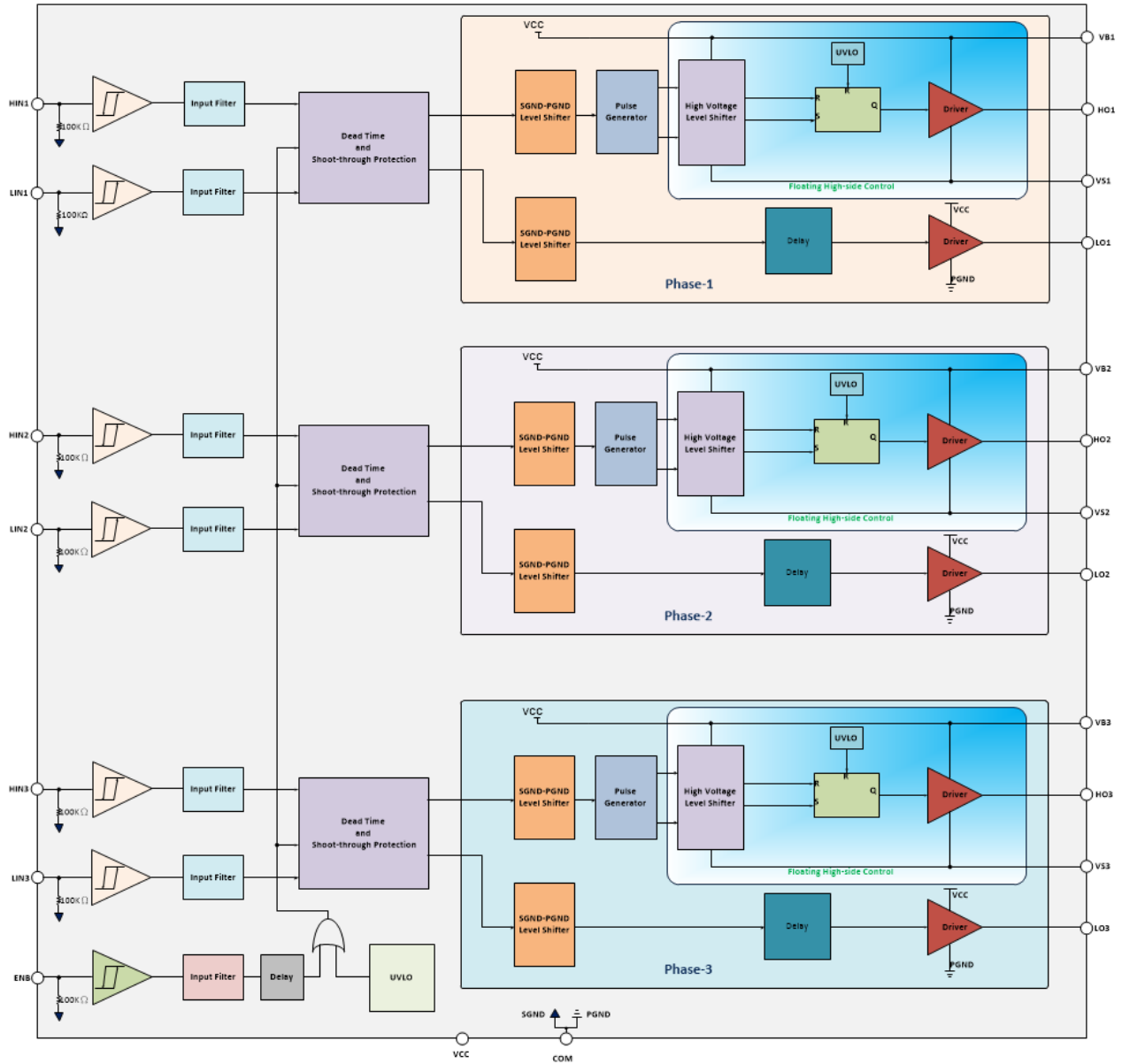
APPLICATION

- E-BIKE/electric power tool 3-phase motor driver
- Battery-powered mini/micro motor control
- General purpose inverter

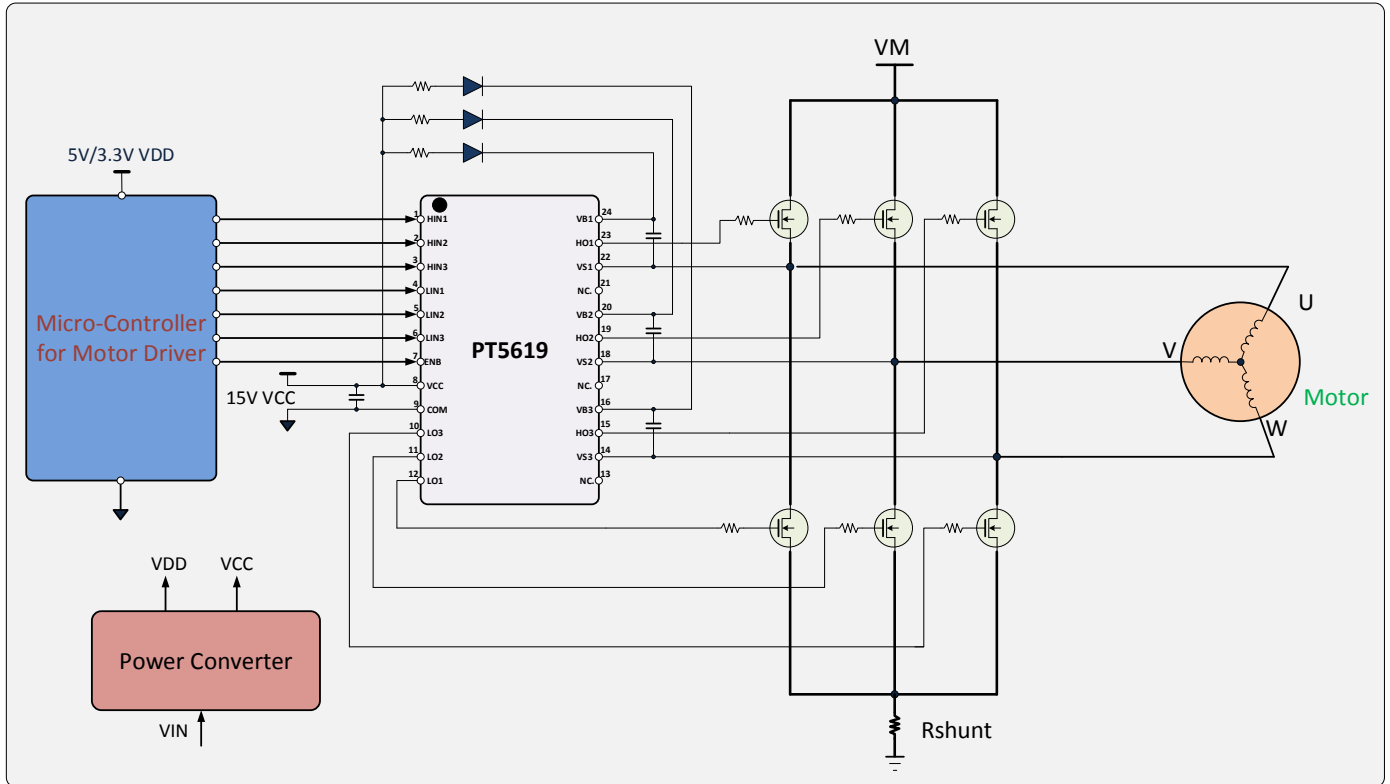
FEATURE

- Integrated 90V half-bridge high side driver
- Ability to drive up to 3-phase half-bridge gates
- Built-in dead time protection
- Shoot-through protection
- Under voltage lockout for VCC and VBS
- Low operation voltage 0–5.5V for VCC and VBS
- 3.3V and 5V input logic compatible
- Enable pin (ENB) for low standby current
- IO+/IO-: +1.2A/-2.0A at VCC=15V, VBS=15V
- Built-in dead time: 0.5 μ s (typ.)
- Common-mode dV/dt noise cancellation circuit
- Tolerant of negative transient voltage
- Low dI/dt gate drive for better noise immunity
- -40°C to 125°C operating range
- Small footprint package: TSSOP20L/24L, QFN24

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT

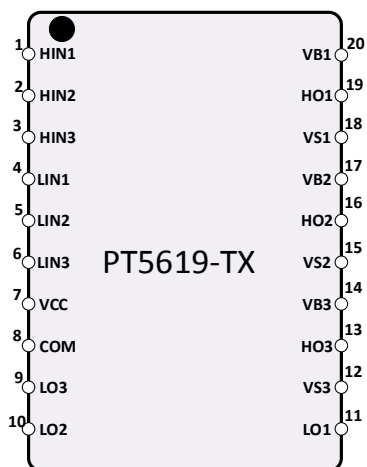


ORDER INFORMATION

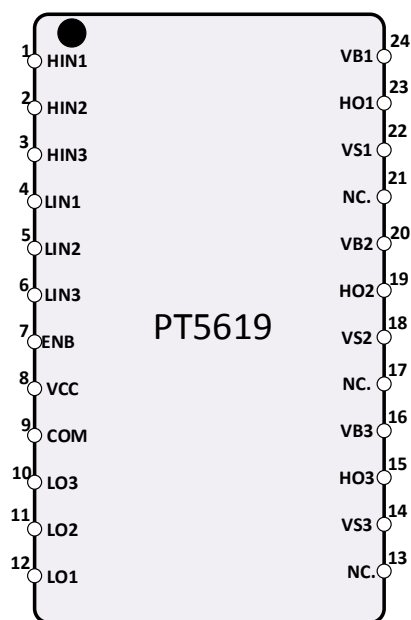
Valid Part Number	Package Type	Top Code
PT5619-TX	20 Pins, TSSOP	PT5619-TX
PT5619	24 Pins, TSSOP	PT5619
PT5619	24 Pins, QFN	PT5619

PIN CONFIGURATION

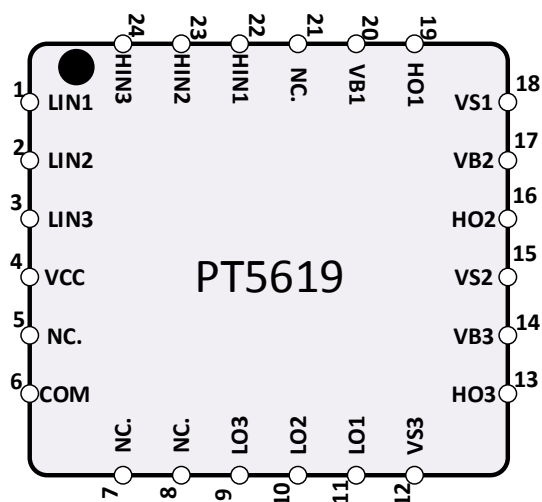
20-PIN TSSOP



24-PIN TSSOP



QFN



PIN DESCRIPTION

Pin Name	Description	Pin No.		
		20-Pin TSSOP	24-Pin TSSOP	QFN
HIN1	Logic input for phase-1 high-side gate driver	1	1	22
HIN2	Logic input for phase-2 high-side gate driver	2	2	23
HIN3	Logic input for phase-3 high-side gate driver	3	3	24
LIN1	Logic input for phase-1 low-side gate driver	4	4	1
LIN2	Logic input for phase-2 low-side gate driver	5	5	2
LIN3	Logic input for phase-3 low-side gate driver	6	6	3
ENB	Logic input for standby mode control	-	7	-
VCC	Logic and low-side gate drivers power supply voltage	7	8	4
NC	Not connected	-	-	5
COM	Logic ground and low-side gate drivers ground	8	9	6
NC	Not connected	-	-	7
NC	Not connected	-	-	8
LO3	Phase-3 low-side gate driver output	9	10	9
LO2	Phase-2 low-side gate driver output	10	11	10
LO1	Phase-1 low-side gate driver output	11	12	11
NC.	Not connected	-	13	-
VS3	Phase-3 high-side driver floating supply offset voltage	12	14	12
HO3	Phase-3 high-side driver output	13	15	13
VB3	Phase-3 high-side driver floating supply	14	16	14
NC.	Not connected	-	17	-
VS2	Phase-2 high-side driver floating supply offset voltage	15	18	15
HO2	Phase-2 high-side driver output	16	19	16
VB2	Phase-2 high-side driver floating supply	17	20	17
NC.	Not connected	-	21	-
VS1	Phase-1 high-side driver floating supply offset voltage	18	22	18
HO1	Phase-1 high-side driver output	19	23	19
VB1	Phase-1 high-side driver floating supply	20	24	20
NC	Not connected	-	-	21

FUNCTION DESCRIPTION

LOW SIDE POWER SUPPLY: VCC

VCC is the low side supply and it provides power to both input logic and low side output power stage. The built-in under-voltage lockout circuit enables the device to operate at sufficient power when a typical VCC supply voltage higher than $V_{CCUV+}=4.2V$ is present, shown as Figure. 1. The PT5619 shuts down all the gate driver outputs, when the VCC supply voltage is below $V_{CCUV-}=3.8V$, shown as Figure. 1. This prevents the external power devices against extremely low gate voltage levels during on-state which may result in excessive power dissipation.

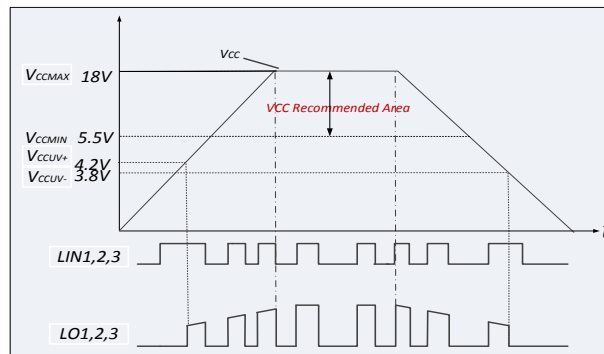


Figure. 1 VCC supply UVLO operating area

HIGH SIDE POWER SUPPLY: VBS (VB1-VS1, VB2-VS2, VB3-VS3)

VBS is the high side supply voltage. The total high side circuitry may float with respect to COM following the external high side power device emitter/source voltage. Due to the internal low power consumption, the entire high side circuitry may be supplied by bootstrap topology connected to VCC, and it may be powered with small bootstrap capacitors. The device operating area as a function of the supply voltage is given in Figure. 2.

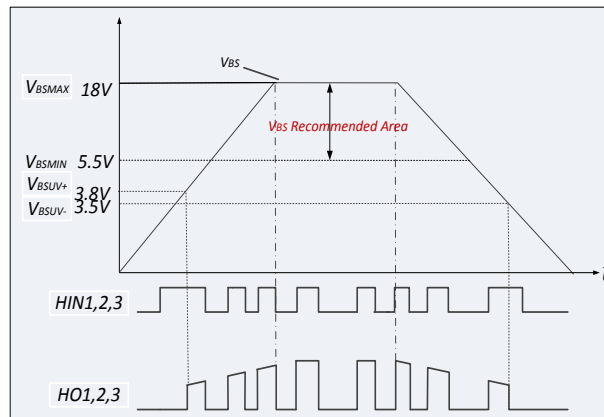


Figure. 2 VBS supply UVLO operating area

LOW SIDE AND HIGH CONTROL INPUT LOGIC: HIN&LIN (HIN1, 2, 3/LIN1, 2, 3)

The Schmitt trigger threshold of each input is designed low enough to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Input Schmitt trigger and advanced noise filtering provide noise rejection of short input pulses. An internal pull-down resistor of about 100k Ω (positive logic) pre-biases each input during VCC supply start-up state. The minimum recommended input pulse-width is 300ns for proper operation of the driver.

SHOOT-THROUGH PREVENTION

The PT5619 is equipped with shoot-through protection circuitry (also known as cross conduction prevention circuitry). Figure. 3 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. When the inputs controlling both high-side and low-side drivers are both logic HIGH, then both driver outputs are pulled down to logic LOW to shut down two power devices in the same bridge.

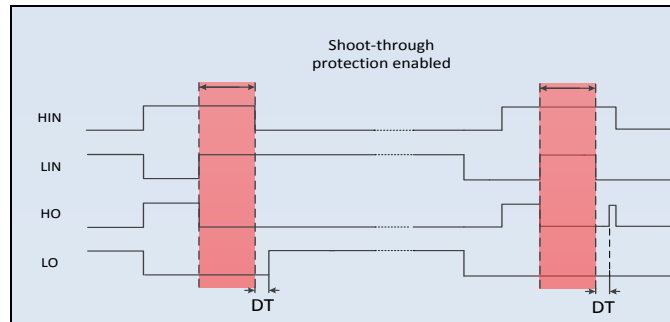


Figure. 3 Shoot-through prevention

DEAD TIME PROTECTION

The PT5619 features integrated fixed dead time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off. This is done to ensure that the power switch has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT. External dead times larger than DT are not modified by the gate driver. Figure. 4 illustrates the dead time period and the relationship between the output gate signals.

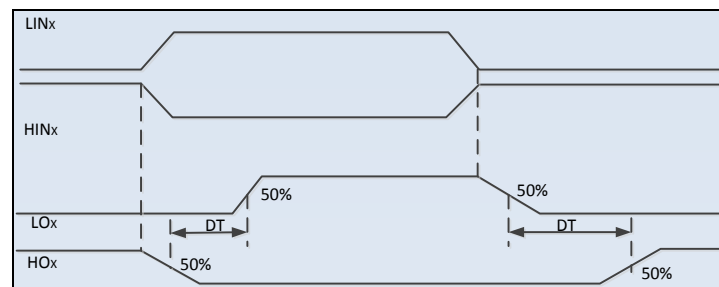


Figure. 4 Dead time protection

GATE DRIVER (HO1, 2, 3/ LO1, 2, 3)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive power devices such as IGBT and power MOSFET. Low side outputs (i.e. LO1, 2, 3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are only changed at the edge of the respective inputs. After releasing from an under-voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output. In contrast, after releasing from an under-voltage condition of the VCC supply, the low side outputs may directly switch to the state of their respective inputs without the additional constraints of the high side driver.

STANDBY MODE

The PT5619 packaged in TSSOP24L provides an enable pin (ENB) to allow the device to work in a low current dissipation state. Pin ENB is compatible with 3.3/5V logic level. If ENB is set to logic HIGH, the device is forced into standby mode and all gate driver outputs are locked into a logic LOW state and only 46 μ A (typ.) is dissipated. If ENB goes from logic HIGH to logic LOW and incorporates a delay of 6 μ s (typ.), the device may be released from standby mode and all outputs are enabled. In order to lower the bias current, a sufficiently large resistor (100k Ω) is tied between ENB and COM.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or cause abnormal function. All the voltage parameters are absolute voltages referenced to IC COM unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	$V_{B1,2,3}$	-0.3	90	V
High-side offset voltage	$V_{S1,2,3}$	$V_{B1,2,3}-20$	$V_{B1,2,3}+0.3$	
High-side gate driver output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}-0.3$	$V_{B1,2,3}+0.3$	
Low-side gate driver output voltage	$V_{LO1,2,3}$	COM-0.3	$V_{CC}+0.3$	
Logic input voltage	$V_{HIN1,2,3}$ $V_{LIN1,2,3}$ ENB	-0.3	20	
Low-side supply voltage	V_{CC}	-0.3	20	
Package power dissipation @ $T_A \leq 25^\circ\text{C}$ ①	P_D	-	TSSOP20:1.2 TSSOP24:1.3	W
Thermal resistance, junction to ambient ①	R_{thJA}	-	TSSOP20:100 TSSOP24:94	$^\circ\text{C}/\text{W}$
Allowable offset voltage slew rate	dV/dt	-	50	V/ns
Junction temperature	T_J	-40	+150	$^\circ\text{C}$
Storage temperature	T_S	-40	+150	
Soldering lead temperature (duration 10s)	TL	-	260	$^\circ\text{C}$

Note:

①: P_D and R_{thJA} are only guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Low-side supply voltage	V_{CC}	5.5	-	18	V
High-side floating supply offset voltage②	$V_{S1,2,3}$	COM-6	-	60	
High-side floating supply voltage	$V_{B1,2,3}$	$V_{S1,2,3}+5.5$	-	$V_{B1,2,3}+18$	
High-side gate driver output voltage	$V_{HO1,2,3}$	V_S	-	V_B	
Low-side gate driver output voltage	$V_{LO1,2,3}$	COM	-	V_{CC}	
Logic input voltage	$V_{HIN1,2,3}$ $V_{LIN1,2,3}$ ENB	0	-	5	
IC operating junction temperature	T_J	-40	-	+125	$^\circ\text{C}$

②: For $V_{BS}=15\text{V}$, normal logic operation for V_S is between COM-6V to 90V. High-side circuitry will sustain current state if V_S is between COM-6V to COM- V_{BS} . The parameter is only guaranteed by design.

STATIC ELECTRICAL CHARACTERISTICS

($V_{CC}-COM$)=(V_B-V_S)=15V. Ambient temperature $T_A=25^{\circ}C$ unless otherwise specified. The $V_{IN,TH}$, V_I , and I_{IN} parameters are referenced to COM and are applicable to all channels. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads. The V_{CCUV} parameters are referenced to, COM. The V_{BSUV} parameters are referenced to V_S .

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
Quiescent VCC supply current	I_{QVCC1}	$V_{HIN1,2,3} = V_{LIN1,2,3} = 0$ or 5V, $V_{ENB} = 0$	210	330	450	μA
Quiescent VCC supply current in standby mode	I_{QVCC2}	$V_{HIN1,2,3} = V_{LIN1,2,3} = 0$ or 5V, $V_{ENB} = 5$	-	46	80	
operating VCC supply current	I_{VCCOP}	$f_{LIN1,2,3} = 20KHz$, $f_{HIN1,2,3} = 20KHz$,	-	1500	-	
VCC supply under-voltage positive going threshold	V_{CCUV+}	-	2.9	4.2	5.5	V
VCC supply under-voltage negative going threshold	V_{CCUV-}	-	2.5	3.8	5.1	
VCC supply under-voltage lockout hysteresis	V_{CCCHYS}	-	-	0.4	-	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V_{BSUV+}	-	2.5	3.8	5.5	V
High side VBS supply under-voltage negative going threshold	V_{BSUV-}	-	2.2	3.5	4.8	
High side VBS supply under-voltage lockout hysteresis	$V_{BSUVHYS}$	-	-	0.3	-	
High side quiescent VBS supply current	I_{QBS}	$V_{BS} = 15V$	25	45	65	μA
Offset supply leakage current	I_{LK}	$V_B = V_S = 100V$ $V_{CC} = 0V$	-	-	10	
Logic Input Section						
Logic HIGH input voltage $HIN1,2,3$, $LIN1,2,3$ and ENB	V_{IH}	-	2.5	-	-	V
Logic LOW input voltage $HIN1,2,3$, $LIN1,2,3$ and ENB	V_{IL}	-	-	-	0.8	
Input positive going threshold	$V_{IN,TH+}$	-	-	1.9	-	
Input negative going threshold	$V_{IN,TH-}$	-	-	1.4	-	
Logic HIGH input bias current	I_{IN+}	$V_{IN} = 5V$	-	50	-	μA
Logic LOW input bias current	I_{IN-}	$V_{IN} = 0$	-	0	-	
Gate Driver Output Section						
High side output HIGH short-circuit pulse current	I_{HO+}	$V_{HO} = V_S = 0$	-	1.2	-	A
High side output LOW short-circuit pulse current	I_{HO-}	$V_{HO} = V_B = 15V$	-	2.0	-	
Low side output HIGH short-circuit pulse current	I_{LO+}	$V_{LO} = 0$	-	1.2	-	
Low side output LOW short-circuit pulse current	I_{LO-}	$V_{LO} = V_{CC} = 15V$	-	2.0	-	
Allowable negative VS voltage for $HIN1,2,3$ signal propagation to $HO1,2,3$	V_{SN}	$V_{BS} = 15V$	-	-8	-	V

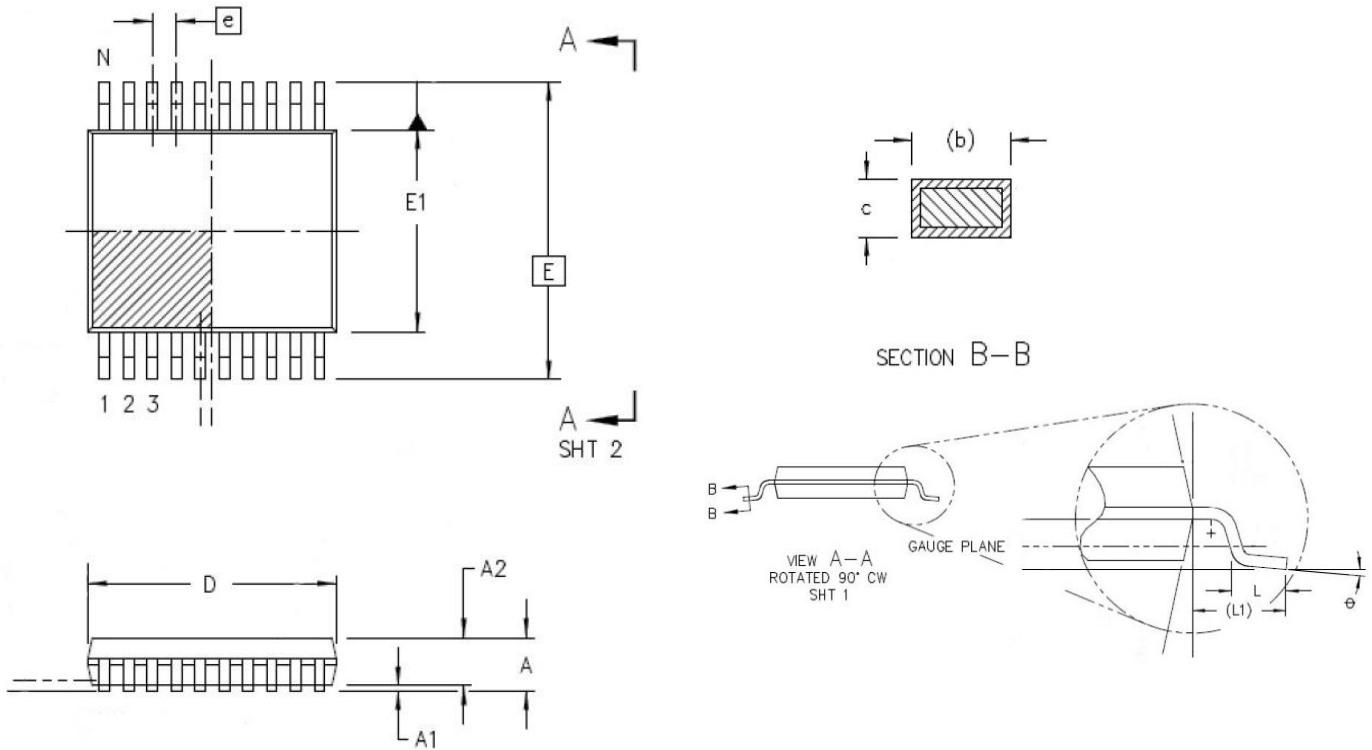
DYNAMIC ELECTRICAL CHARACTERISTICS

($V_{CC}-COM$)=(V_B-V_S)=15V, $V_{S1,2,3}=COM$, and $C_{load}=1nF$ unless otherwise specified, ambient temperature $T_A=25^{\circ}C$.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	t_{on}	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=5V$, $V_{S1,2,3}=0$	-	120	200	ns
Turn-off propagation delay	t_{off}	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=0$, $V_{S1,2,3}=0$	-	120	200	
Turn-on rise time	t_r	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=5V$, $V_{S1,2,3}=0$	-	37	-	
Turn-off fall time	t_f	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=0$, $V_{S1,2,3}=0$	-	30	-	
Dead time	DT	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=0$ and 5V, without external dead time	300	500	700	
Dead time matching (all six channels)	MDT	without external dead time	-	-	50	
Delay matching (all six channels)	MT	external dead time > 1000ns	-	-	50	
Output pulse-width matching	PM	external dead time > 1000ns, $PW_{IN}=10\mu s$, $PM=PW_{OUT}-PW_{IN}$	-	-	50	
ENB input filter time	$t_{FLT,ENB}$	$V_{ENB}=0$ and 5V	-	450	-	μs
ENB input logic HIGH to HO/LO turn-off delay time	$t_{off,ENB}$	$V_{ENB}=5V$	-	0.55	-	
ENB input logic LOW to HO/LO turn-on delay time	$t_{on,ENB}$	$V_{ENB}=0V$	-	6	-	

PACKAGE INFORMATION

20 PINS, TSSOP, 173MIL

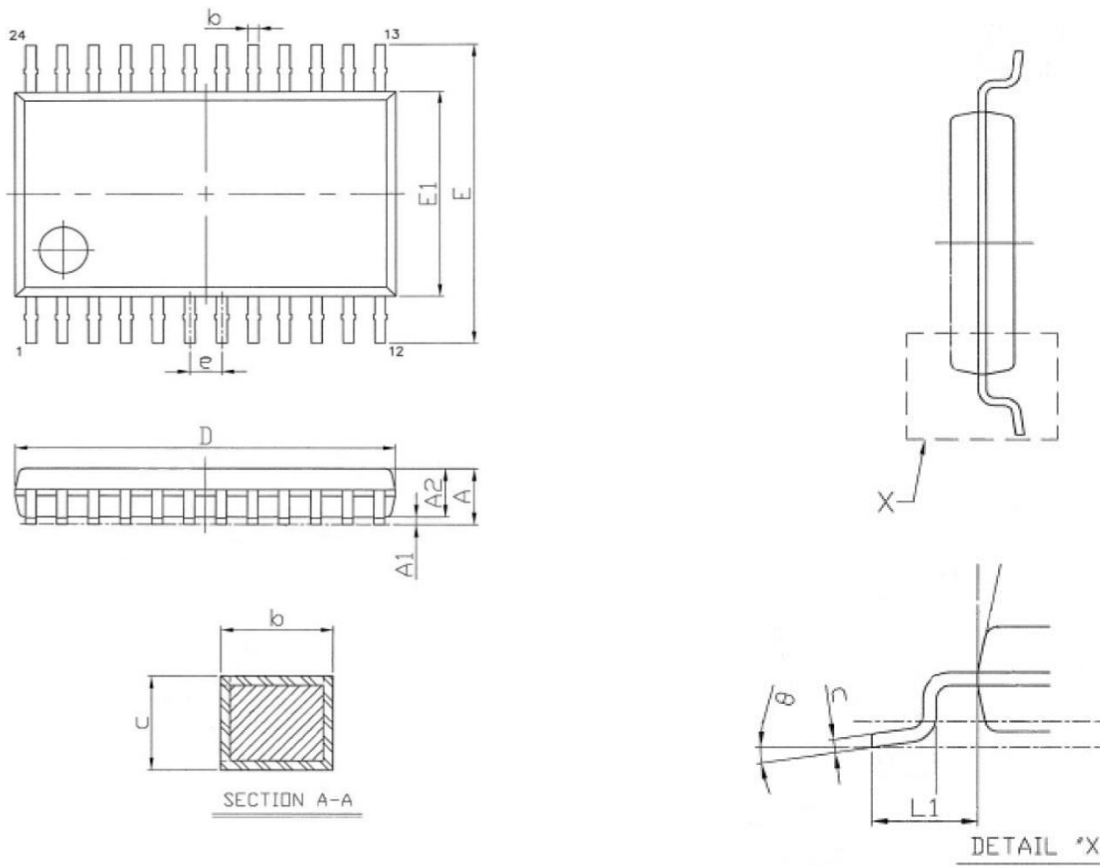


Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
e	0.65BSC		
D	6.40	6.50	6.60
E	6.4 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	-	8°

Notes:

1. All dimensions refer to JEDEC MO-153 AC
2. All dimensions are in mm

24 PINS, TSSOP, 173MIL

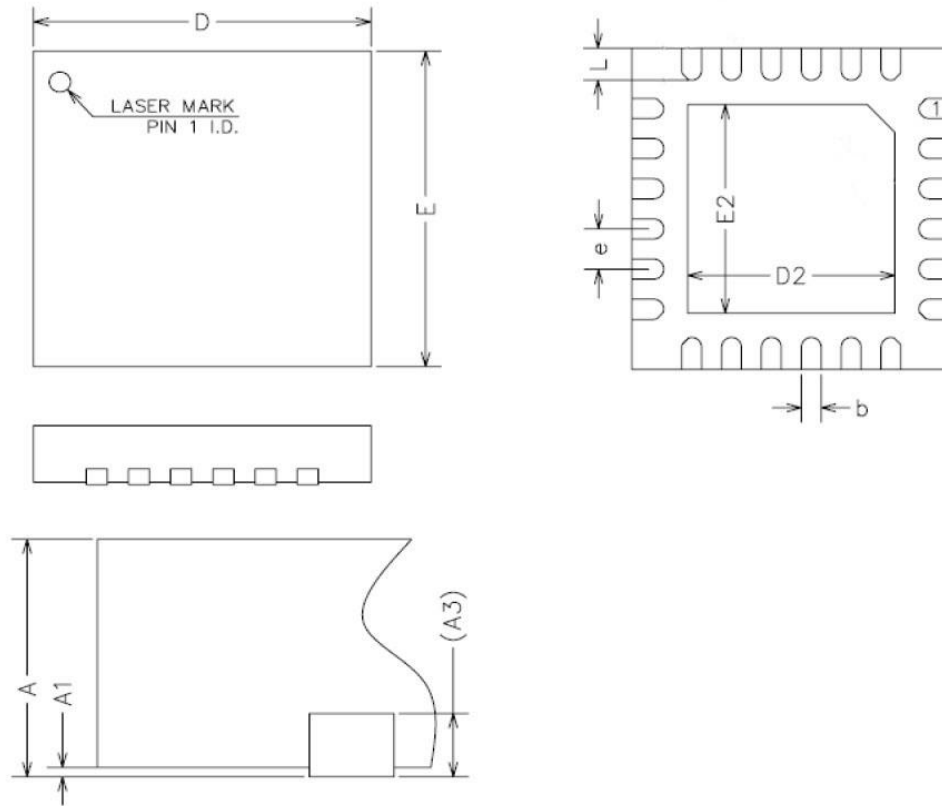


Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	0.20	0.30
c	0.09	-	0.20
e	0.65 BSC		
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
L1	1.00 REF		
θ	0°	-	8°

Notes:

1. All dimensions refer to JEDEC MO-153 ADT
2. All dimensions are in mm

24 PINS, QFN



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.50	2.65	2.80
E	4.00 BSC		
E2	2.50	2.65	2.80
e	0.50 BSC		
L	0.35	0.40	0.45

Notes:

1. All dimensions refer to JEDEC MO-220 WGGD-6
2. All dimensions are in mm

IMPORTANT NOTICE

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