

# Delay Lines

## Active Delay Lines Lead

# ADL Series

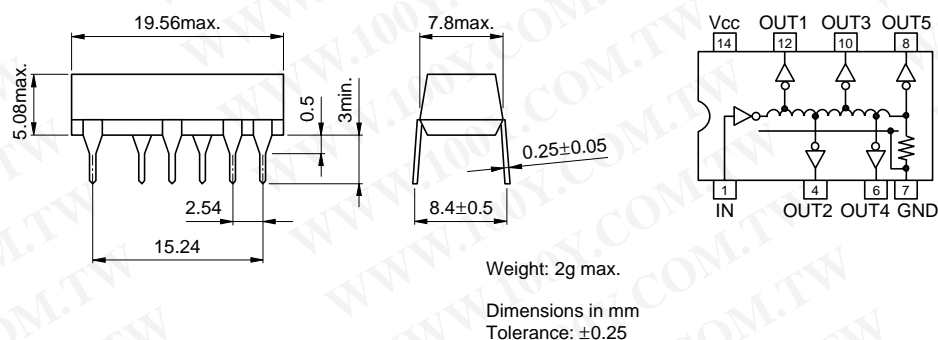
### FEATURES

- Waveform shaping circuits are not required for the built-in TTL IC.
- Integration into a dual-inline package achieves a compact size only 5.08mm in height.
- These delay lines are transfer molded using high-performance resins.
- They can be used with automated inserters.

### MAXIMUM RATINGS

Power supply voltage	Vcc	7V
Input voltage	Vin	-0.5 to +5.5V
Temperature range	Operating	0 to +70°C
	Storage	-55 to +125°C

### SHAPES AND DIMENSIONS/CIRCUIT DIAGRAM



Weight: 2g max.

Dimensions in mm  
Tolerance: ±0.25

### ELECTRICAL CHARACTERISTICS

Part No.	Total delay time Td(ns)	Delay time between each tap td(ns)	Rise time (ns)max.	Minimum input pulse width* (ns)min.
ADL-020SH	20±2	4±2	4	8
ADL-025SH	25±3	5±2	4	10
ADL-050SH	50±3	10±2	4	20
ADL-060SH	60±3	12±3	4	24
ADL-075SH	75±5%	15±3	4	30
ADL-100SH	100±5%	20±3	4	40
ADL-125SH	125±5%	25±3	4	50
ADL-150SH	150±5%	30±3	4	60
ADL-200SH	200±5%	40±3	4	80
ADL-250SH	250±5%	50±3	4	100

\* Repeat cycle T=Td×30

• Measuring conditions

Power supply voltage Vcc: 5±0.1V/Ambient temperature: 25±1°C/No load between each tap

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-34970699  
勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

# Delay Lines

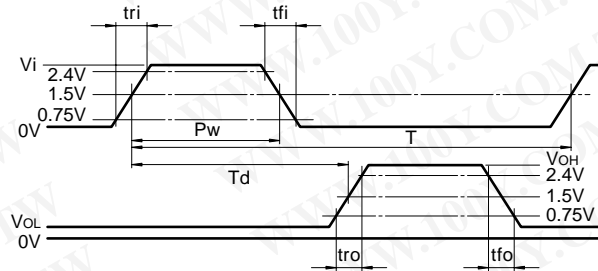
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### MEASURING CONDITIONS

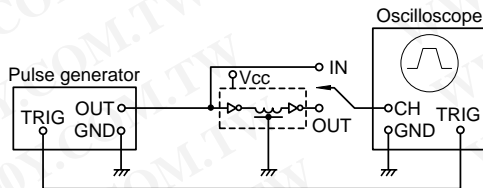
Input voltage $V_i$	3.2V
Pulse width conversion $P_w$	$T_d(\text{Total delay time}) \times 3$
Repeat cycle $T$	$P_w \times 10$ [Duty: 10%]
Input rise time $T_{ri}$	5ns max.
Power supply voltage $V_{cc}$	$5 \pm 0.1V$
Ambient temperature $T_a$	$25 \pm 1^\circ C$

### WAVEFORMS



$V_i$  : Input voltage  
 $T_d$  : Total delay time  
 $P_w$  : Pulse width conversion  
 $t_{ri}$  : Input rise time  
 $t_{fi}$  : Input fall time  
 $t_{ro}$  : Output rise time  
 $t_{fo}$  : Output fall time  
 $V_{OL}$  : Output voltage(L level)  
 $V_{OH}$  : Output voltage(H level)

### MEASURING CIRCUITS



### INPUT/OUTPUT CHARACTERISTICS

Item	Measuring conditions	Standard value		
		Minimum	Nominal	Maximum
Power supply voltage $V_{cc}$		4.75V	5V	5.25V
Input voltage (H level) $V_{IH}$		2V	—	—
Input voltage (L level) $V_{IL}$		—	—	0.8V
Output voltage (H level) $V_{OH}$	$V_{cc}=4.75V$ $V_{IH}=2V$ $I_{OH}=-1mA$	2.7V	3.4V	—
Output voltage (L level) $V_{OL}$	$V_{cc}=4.75V$ $V_{IL}=0.8V$ $I_{OL}=20mA$	—	—	0.5V
Input current (H level) $I_{IH}$	$V_{cc}=5.25V$ $V_i=2.7V$	—	—	50 $\mu A$
Input current (L level) $I_{IL}$	$V_{cc}=5.25V$ $V_i=0.5V$	—	—	-2mA
Power supply current $I_{ccL}$	$V_{cc}=5.25V$ $V_{IL}=0V$	—	47mA	65mA

### OUTPUT LOAD CONDITIONS

Logic 1 output	20TTL load/tap [ $I_{OH}/I_{IH}=1mA/50\mu A=20$ ]
Logic 0 output	10TTL load/tap [ $I_{OL}/I_{IL}=20mA/2mA=10$ ]