8031AH/8051AH
8032AH/8052AH
MCS® 51
NMOS SINGLE-CHIP 8-BIT MICROCONTROLLERS

Automotive

- **High Performance HMOS Process**
- **Internal Timers/Event Counters**
- **2-Level Interrupt Priority Structure**
- **32 I/O Lines (Four 8-Bit Ports)**
- **64K Program Memory Space**
- **Security Feature Protects EPROM Parts Against Software Piracy**
- **Boolean Processor**
- **Bit-Addressable RAM**
- **Programmable Full Duplex Serial Channel**
- **111 Instructions (64 Single-Cycle)**
- **64K Data Memory Space**
- **Available in PLCC and DIP Packages**

The MCS® 51 microcontroller products are optimized for control applications. Byte-processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for one-bit variables as a separate data type, allowing direct bit manipulation and testing in control and logic systems that require Boolean processing.

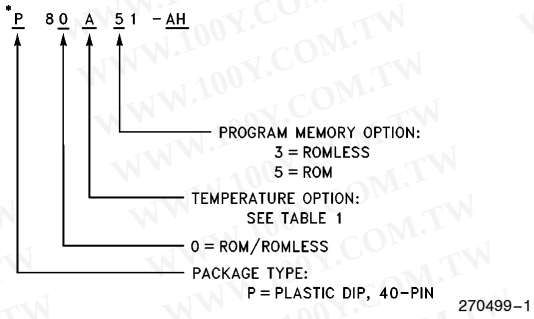
Device	Internal Memory		Timers/ Event Counters	Interrupts
	Program	Data		
8052AH	8K x 8 ROM	256 x 8 RAM	3 x 16-Bit	6
8051AH	4K x 8 ROM	128 x 8 RAM	2 x 16-Bit	5
8032AH	none	256 x 8 RAM	3 x 16-Bit	6
8031AH	none	128 x 8 RAM	2 x 16-Bit	5

PRODUCT OPTIONS

Intel's extended and automotive temperature range products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C ambient. For the automotive temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +110°C ambient.

The automotive, extended, and commercial temperature versions of the MCS 51 microcontroller product families are available with or without burn-in options.



*Example:
P, 80A51AH indicates an automotive temperature range version of the 8051AH in a PDIP package with 4 Kbyte ROM program memory.

Figure 1. MCS® 51 Microcontroller Product Family Nomenclature

Table 1. Temperature Options

Temperature Classification	Temperature Designation	Operating Temperature °C Ambient	Burn-In Option
Extended	T	−40 to +85	Standard
	L	−40 to +85	Extended
Automotive	A	−40 to +110	Standard

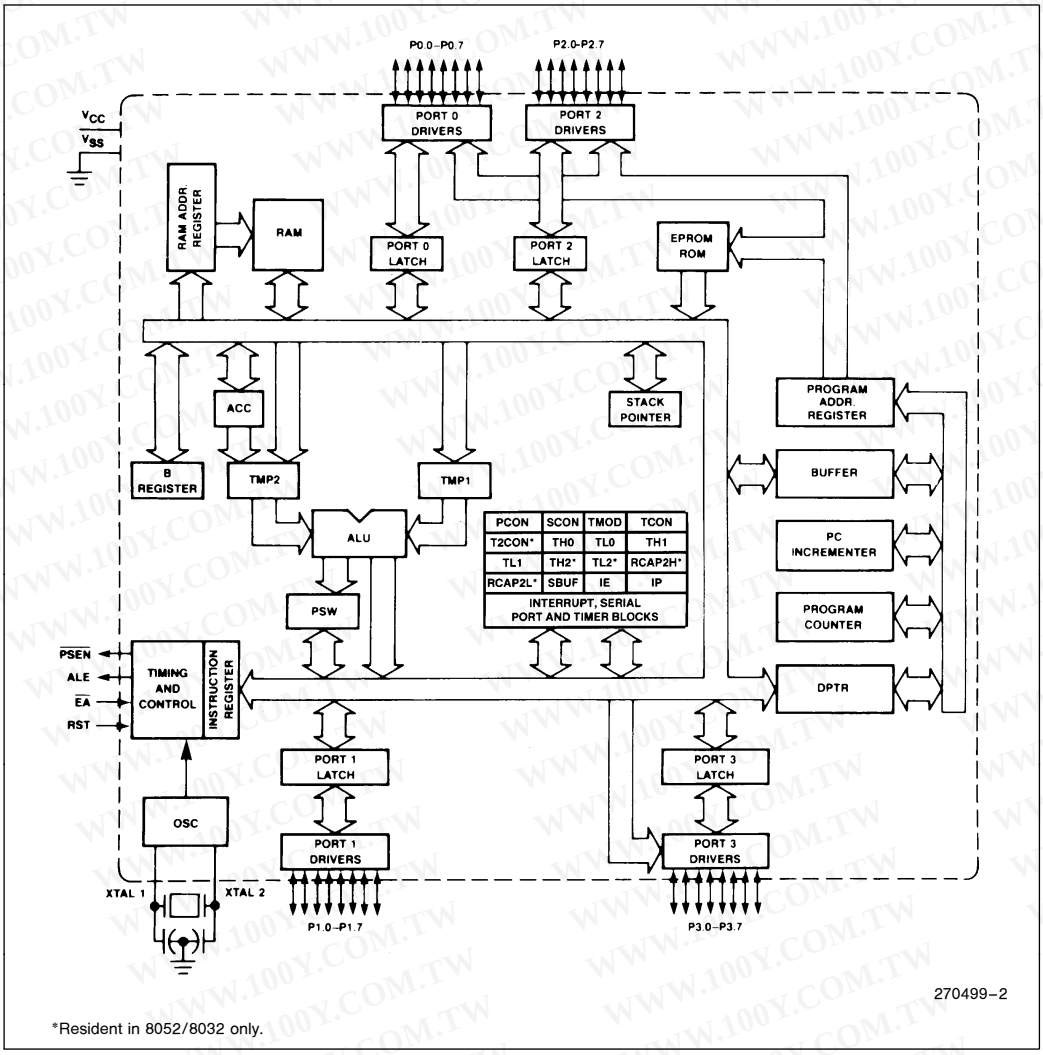


Figure 2. MCS® 51 Microcontroller Block Diagram

PIN DESCRIPTIONS

V_{CC}

Supply voltage.

V_{SS}

Circuit ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s and can source and sink 8 LS TTL inputs.

Port 0 also outputs the code bytes during program verification of the ROM. External pullups are required.

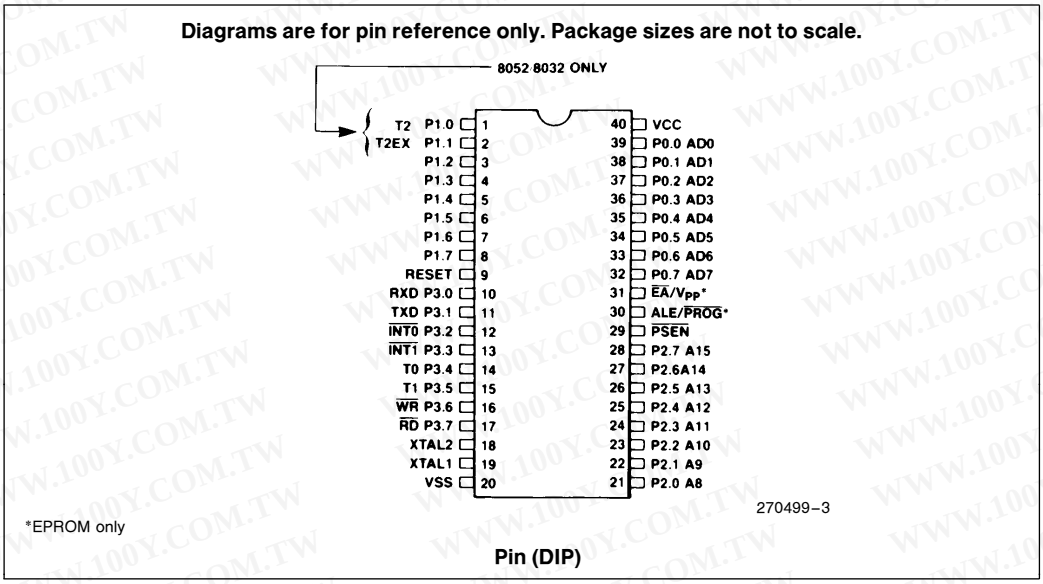


Figure 3. MCS® 51 Microcontroller Connections

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL} on the datasheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during program verification of the ROM.

In the 8032AH and 8052AH, Port 1 pins P1.0 and P1.1 also serve the T2 and T2EX functions, respectively.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL} on the datasheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during program verification of the ROM.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL} on the datasheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS 51 microcontroller family, as listed below:

Port Pin	Alternative Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

RESET

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

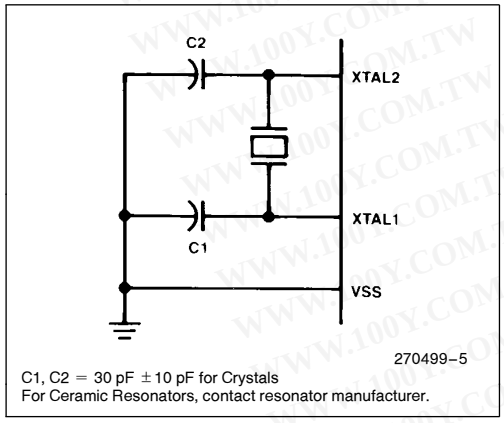
$\overline{PSEN}$

Program Store Enable is the read strobe to external Program Memory.

When the device is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}/V_{PP}$

External Access enable $\overline{EA}$ must be strapped to V_{SS} in order to enable any MCS 51 microcontroller device to fetch code from external Program memory locations 0 to 0FFFH (0 to 1FFFH, in the 8032AH and 8052AH).



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 4. Oscillator Connections

XTAL1

Input to the inverting oscillator amplifier.

XTAL2

Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the datasheet must be observed.

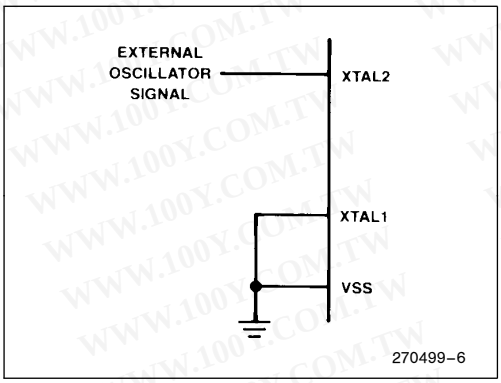


Figure 5. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias . . . . . −40°C to +110°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on $\overline{EA}$/VPP Pin to V_{SS} . . . −0.5V to +21.5V
Voltage on Any Other Pin to V_{SS} . . . . −0.5V to +7V
Power Dissipation 1.5W
Based on package heat transfer limitations not device power consumption.
Maximum Case Temperature
Under Bias . . . . . +125°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Typical Thermal Resistance Junction to Ambient (θ_{JA})

Package	θ_{JA}
Plastic DIP	75°C/W

DC CHARACTERISTICS $T_A = -40°C$ to $+110°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST)	2.1	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage to XTAL2, RST	2.6	V_{CC} + 0.5	V	XTAL1 = V_{SS}
V_{OL}	Output Low Voltage (Ports 1, 2, 3)*		0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)*		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4		V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −400 μA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, RST) 8032AH, 8052AH All Others		−800 −500	μA μA	V_{IN} = 0.45V V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current (XTAL2)		−4.0	mA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)		±10	μA	$0.45 \le V_{IN} \le V_{CC}$
I_{IH1}	Input Current to RST to Activate Reset		500	μA	$V_{IN} < (V_{CC} - 1.5V)$
I_{CC}	Power Supply Current: 8031/8051 8031AH/8051AH 8032AH/8052AH		 175 135 175	 mA mA mA	 All Outputs Disconnected;
C_{IO}	Pin Capacitance		10	pF	Test freq = 1 MHz

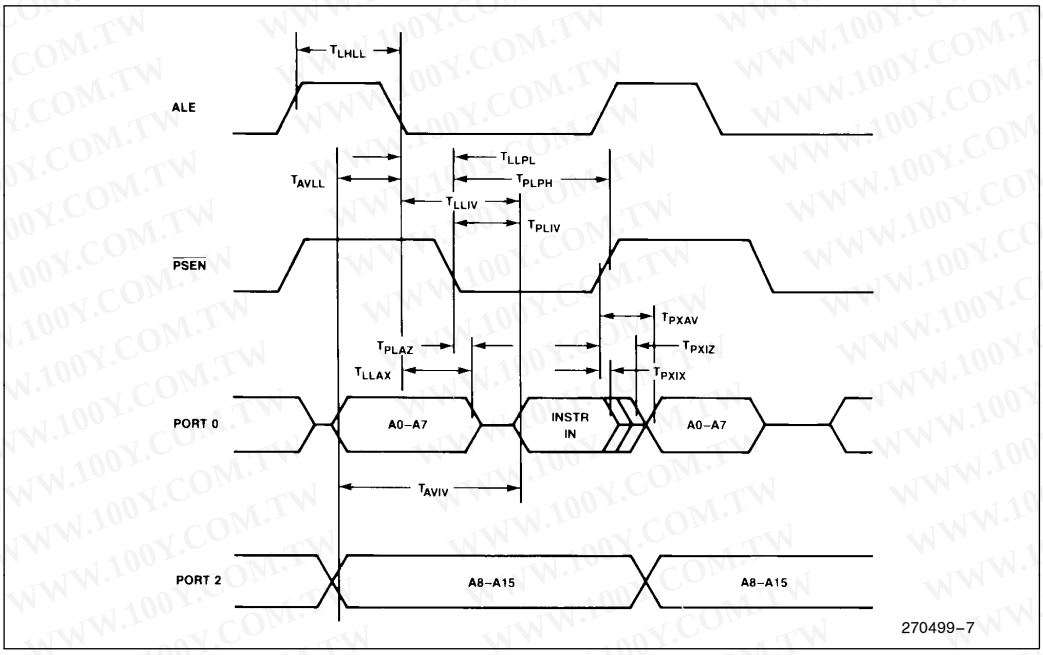
***NOTE:**
Capacitive loading on Ports 0 and 2 may cause noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

AC CHARACTERISTICS

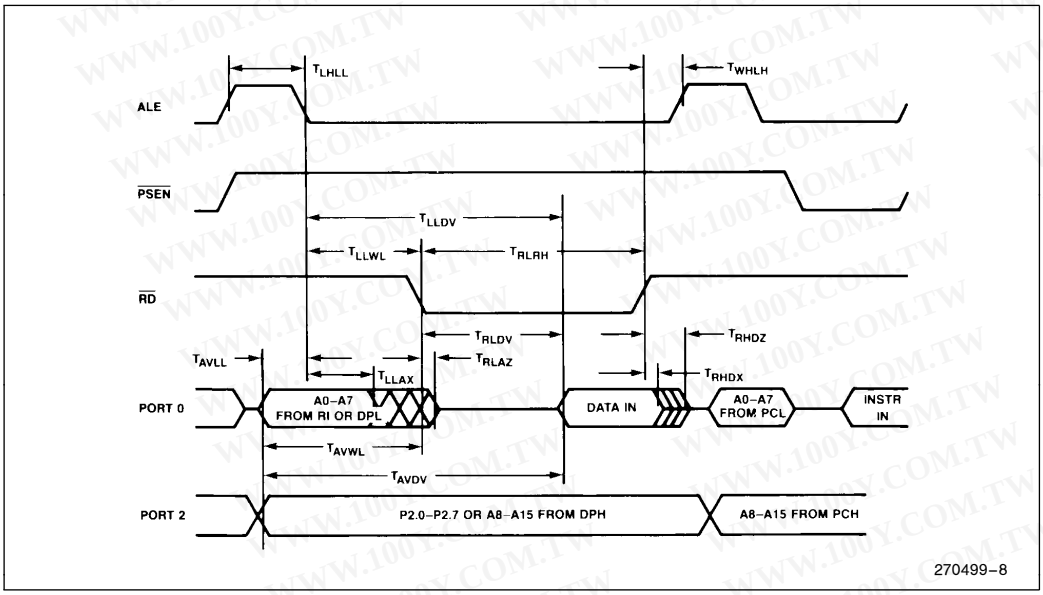
$T_A = -40°C$ to $+110°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$;
Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency			3.5	12.0	MHz
T_{LHLL}	ALE Pulse Width	127		$2T_{CLCL}-40$		ns
T_{AVLL}	Address Valid to ALE Low	43		$T_{CLCL}-40$		ns
T_{LLAX}	Address Hold after ALE Low	48		$T_{CLCL}-35$		ns
T_{LLIV}	ALE Low to Valid Instr In		233		$4T_{CLCL}-100$	ns
T_{LLPL}	ALE Low to $\overline{PSEN}$ Low	58		$T_{CLCL}-25$		ns
T_{PLPH}	$\overline{PSEN}$ Pulse Width	215		$3T_{CLCL}-35$		ns
T_{PLIV}	$\overline{PSEN}$ Low to Valid Instr In		125		$3T_{CLCL}-125$	ns
T_{PXIX}	Input Instr Hold after $\overline{PSEN}$	0		0		ns
T_{PXIZ}	Input Instr Float after $\overline{PSEN}$		63		$T_{CLCL}-20$	ns
T_{PXAV}	$\overline{PSEN}$ to Address Valid	75		$T_{CLCL}-8$		ns
T_{AVIV}	Address to Valid Instr In		302		$5T_{CLCL}-115$	ns
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float		20		20	ns
T_{RLRH}	$\overline{RD}$ Pulse Width	400		$6T_{CLCL}-100$		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	400		$6T_{CLCL}-100$		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5T_{CLCL}-165$	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Data Float after $\overline{RD}$ High		97		$2T_{CLCL}-70$	ns
T_{LLDV}	ALE Low to Valid Data In		517		$8T_{CLCL}-150$	ns
T_{AVDV}	Address to Valid Data In		585		$9T_{CLCL}-165$	ns
T_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3T_{CLCL}-50$	$3T_{CLCL}+50$	ns
T_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4T_{CLCL}-130$		ns
T_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		$T_{CLCL}-60$		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7T_{CLCL}-150$		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	33		$T_{CLCL}-50$		ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		20		20	ns
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	$T_{CLCL}-40$	$T_{CLCL}+40$	ns

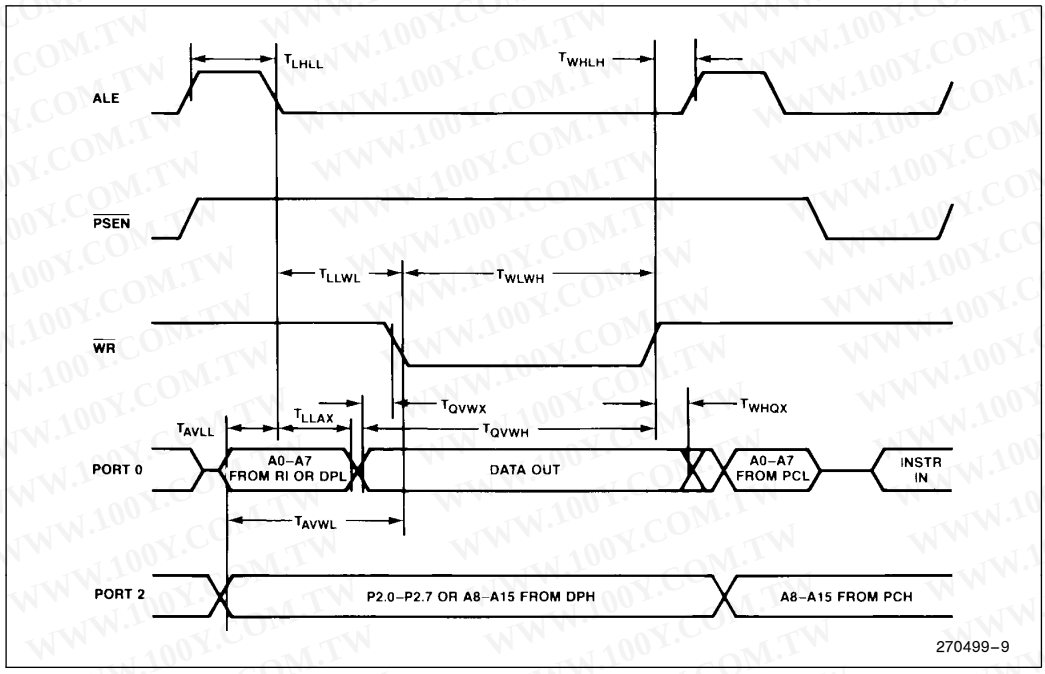
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

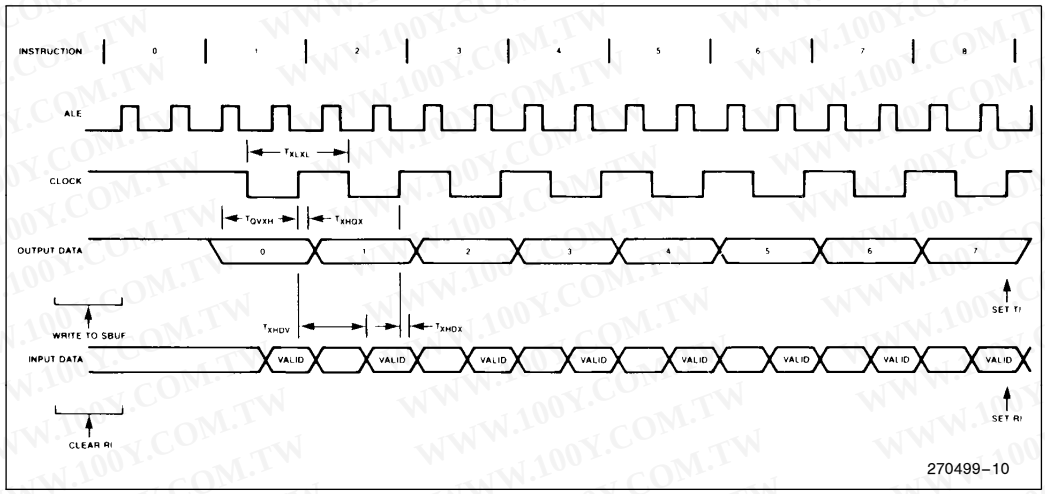


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_A = -40°C$ to $+110°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		$12T_{CLCL}$		μs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10T_{CLCL}-133$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	50		$2T_{CLCL}-117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10T_{CLCL}-133$	ns

SHIFT REGISTER TIMING WAVEFORMS

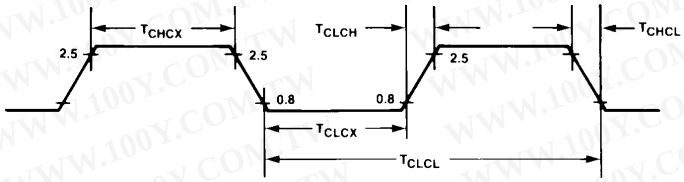


270499–10

EXTERNAL CLOCK DRIVE

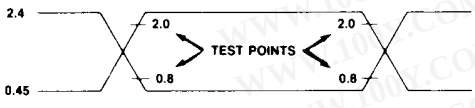
Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency	3.5	12	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		20	ns
T_{CHCL}	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270499–11

AC TESTING INPUT, OUTPUT WAVEFORMS



270499–12

AC Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

DATASHEET REVISION HISTORY

The following are key differences between this datasheet and the -005 version:

1. The "preliminary" status was dropped and replaced with production status (no label).
2. Trademarks were updated.

The following are key differences between the -005 and the -004 version of the datasheet:

1. Preliminary notice was placed on the title page.
2. Figure 2. MCS 51 Block Diagram was modified to include the note found at the bottom of the figure.
3. RST pin in Figure 3 was changed to RESET.
4. RST pin description was changed to RESET pin description.
5. Power dissipation note added below Power dissipation listing in Absolute Maximum Ratings.
6. V_{IH} and V_{IH1} were changed by 0.1V to reflect test conditions.
7. T_{PLPH} was corrected to show test program timing.

The following are key differences between the -004 datasheet and the -003 version of the datasheet:

1. The title was changed to 8031AH/8051AH, 8032AH/8052AH MCS 51 NMOS Single-Chip 8-Bit Microcontrollers.
2. "NC" pin labels changed to "Reserved" in Figure 3.
3. Capacitor value for ceramic resonators deleted in Figure 4.

The following are key differences between the -001 and the -002 version of the datasheet:

1. The title was changed to 8031/8051, 8031AH/8051AH, 8032AH/8052AH, 8751H MCS 51 NMOS Single-Chip 8-Bit Microcontrollers.
2. Removed 8751H-8 from the datasheet.
3. Removed reference to LCC package version.
4. Removed burn-in options from Table 1.
5. Added pin count to Figure 1.
6. Test conditions for I_{IL1} and I_{IH} specifications added to the DC Characteristics.
7. Datasheet revision history added.