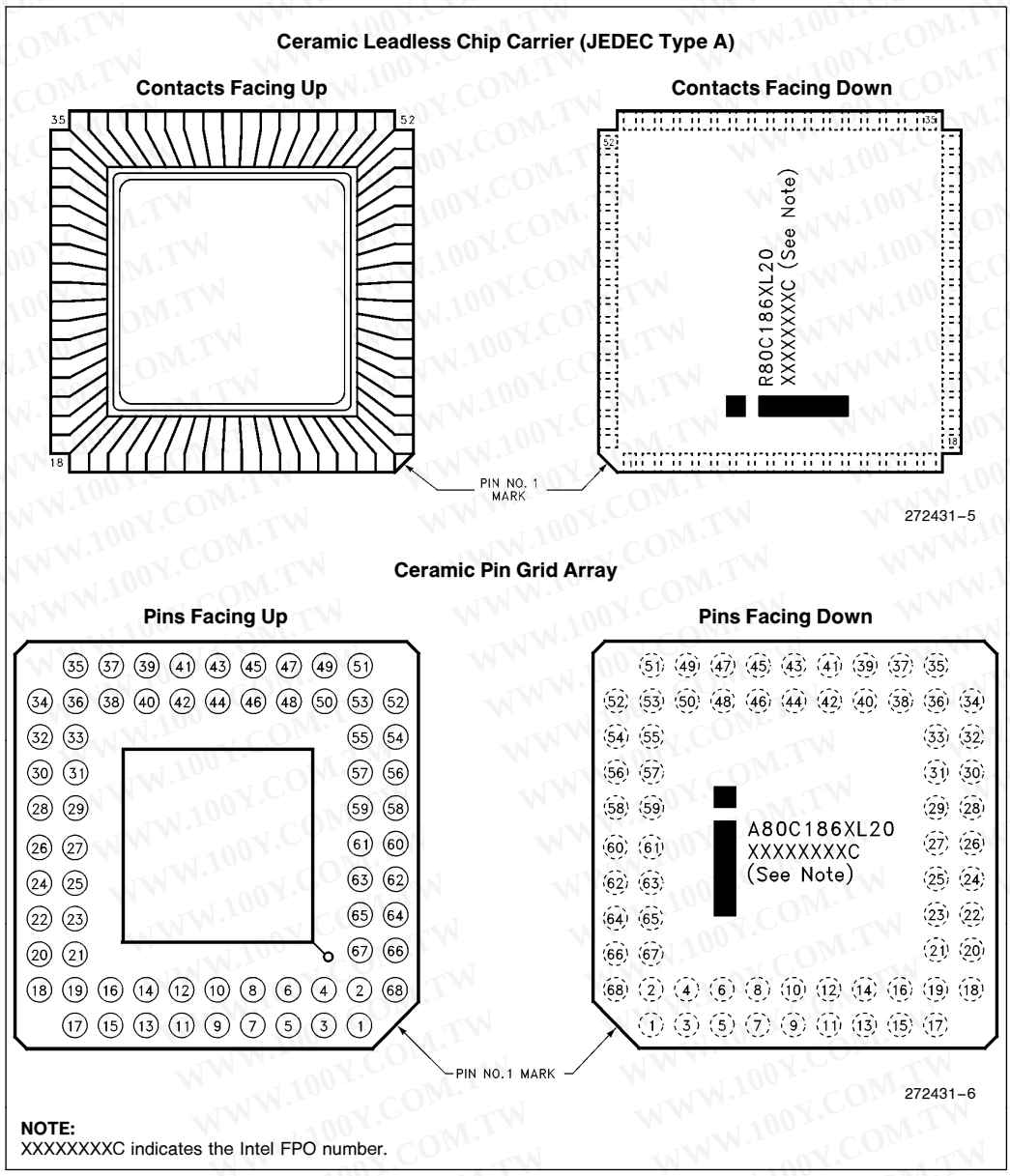
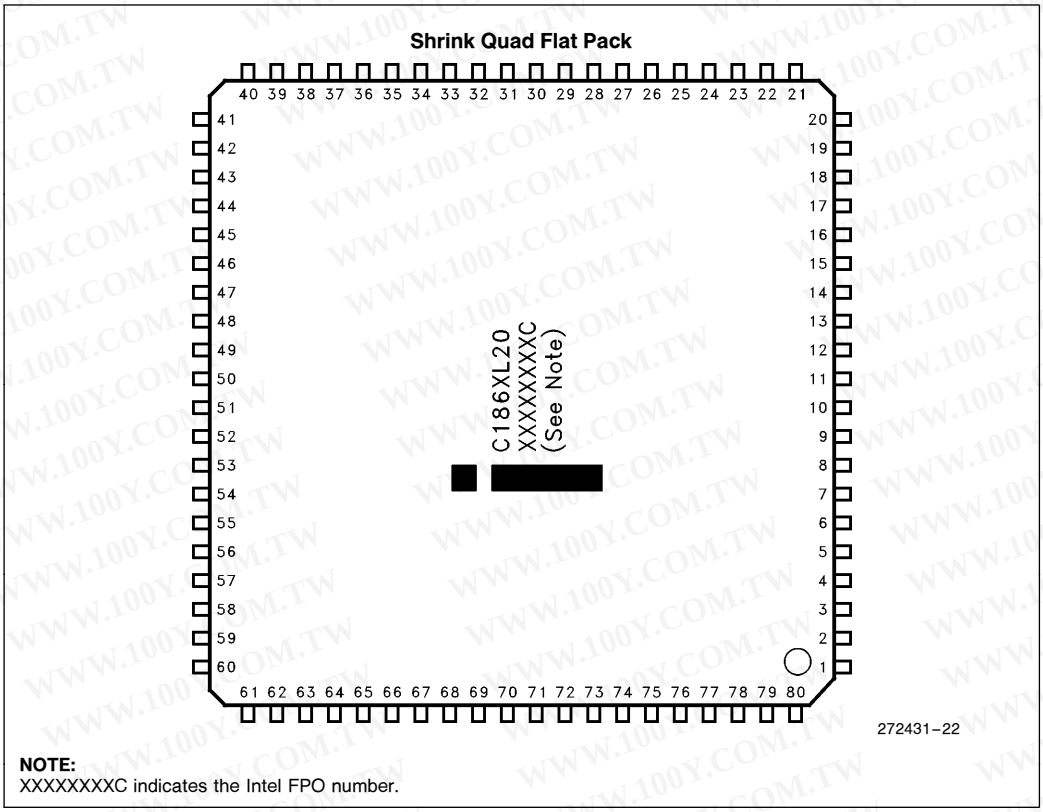


NOTE:
XXXXXXXXC indicates the Intel FPO number.

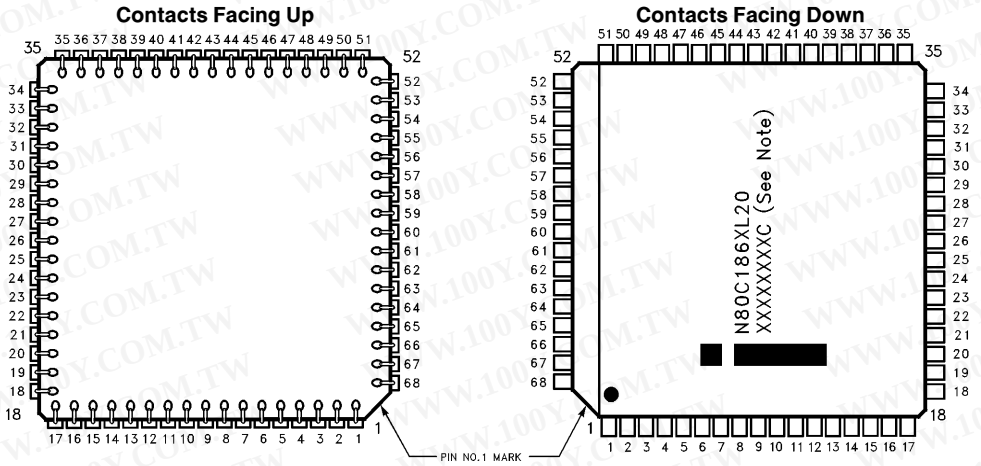
Figure 4. 80C186XL/80C188XL Pinout Diagrams



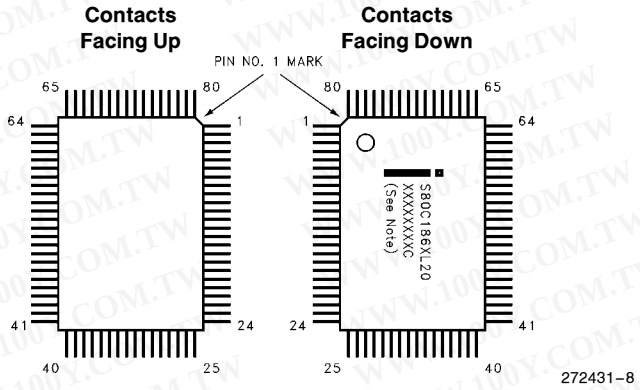
NOTE:
XXXXXXXXC indicates the Intel FPO number.

Figure 4. 80C186XL/80C188XL Pinout Diagrams (Continued)

Plastic Leaded Chip Carrier



80-Pin Quad Flat Pack (EIAJ)



NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 4. 80C186XL/80C288XL Pinout Diagrams (Continued)

Table 4. LCC/PLCC Pin Functions with Location

AD Bus	
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
AD8 (A8)	16
AD9 (A9)	14
AD10 (A10)	12
AD11 (A11)	10
AD12 (A12)	7
AD13 (A13)	5
AD14 (A14)	3
AD15 (A15)	1
A16/S3	68
A17/S4	67
A18/S5	66
A19/S6	65

Bus Control	
ALE/QS0	61
$\overline{BHE}$ ($\overline{RFSH}$)	64
$\overline{S0}$	52
$\overline{S1}$	53
$\overline{S2}$	54
$\overline{RD}$/$\overline{QSMD}$	62
$\overline{WR}$/QS1	63
ARDY	55
SRDY	49
$\overline{DEN}$	39
DT/$\overline{R}$	40
$\overline{LOCK}$	48
HOLD	50
HLDA	51

Processor Control	
$\overline{RES}$	24
RESET	57
X1	59
X2	58
CLKOUT	56
$\overline{TEST}$/BUSY	47
NMI	46
INT0	45
INT1/$\overline{SELECT}$	44
INT2/$\overline{INTA0}$	42
INT3/$\overline{INTA1}$	41

Power and Ground	
V_{CC}	9
V_{CC}	43
V_{SS}	26
V_{SS}	60

I/O	
$\overline{UCS}$	34
$\overline{LCS}$	33
$\overline{MCS0}$/PEREQ	38
$\overline{MCS1}$/$\overline{ERROR}$	37
$\overline{MCS2}$	36
$\overline{MCS3}$/$\overline{NPS}$	35
$\overline{PCS0}$	25
$\overline{PCS1}$	27
$\overline{PCS2}$	28
$\overline{PCS3}$	29
$\overline{PCS4}$	30
$\overline{PCS5}$/A1	31
$\overline{PCS6}$/A2	32
TMR IN 0	20
TMR IN 1	21
TMR OUT 0	22
TMR OUT 1	23
DRQ0	18
DRQ1	19

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 5. LCC/PGA/PLCC Pin Locations with Pin Names

1	AD15 (A15)
2	AD7
3	AD14 (A14)
4	AD6
5	AD13 (A13)
6	AD5
7	AD12 (A12)
8	AD4
9	V_{CC}
10	AD11 (A11)
11	AD3
12	AD10 (A10)
13	AD2
14	AD9 (A9)
15	AD1
16	AD8 (A8)
17	AD0

18	DRQ0
19	DRQ1
20	TMR IN 0
21	TMR IN 1
22	TMR OUT 0
23	TMR OUT 1
24	$\overline{RES}$
25	$\overline{PCS0}$
26	V_{SS}
27	$\overline{PCS1}$
28	$\overline{PCS2}$
29	$\overline{PCS3}$
30	$\overline{PCS4}$
31	$\overline{PCS5}$/A1
32	$\overline{PCS6}$/A2
33	$\overline{LCS}$
34	$\overline{UCS}$

35	$\overline{MCS3}$/$\overline{NPS}$
36	$\overline{MCS2}$
37	$\overline{MCS1}$/$\overline{ERROR}$
38	$\overline{MCS0}$/PEREQ
39	$\overline{DEN}$
40	DT/$\overline{R}$
41	INT3/$\overline{INTA1}$
42	INT2/$\overline{INTA0}$
43	V_{CC}
44	INT1/$\overline{SELECT}$
45	INT0
46	NMI
47	$\overline{TEST}$/BUSY
48	$\overline{LOCK}$
49	SRDY
50	HOLD
51	HLDA

52	$\overline{S0}$
53	$\overline{S1}$
54	$\overline{S2}$
55	ARDY
56	CLKOUT
57	RESET
58	X2
59	X1
60	V_{SS}
61	ALE/QS0
62	$\overline{RD}$/$\overline{QSMD}$
63	$\overline{WR}$/QS1
64	$\overline{BHE}$ ($\overline{RFSH}$)
65	A19/S2
66	A18/S3
67	A17/S4
68	A16/S3

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 6. QFP Pin Functions with Location

AD Bus	
AD0	64
AD1	66
AD2	68
AD3	70
AD4	74
AD5	76
AD6	78
AD7	80
AD8 (A8)	65
AD9 (A9)	67
AD10 (A10)	69
AD11 (A11)	71
AD12 (A12)	75
AD13 (A13)	77
AD14 (A14)	79
AD15 (A15)	1
A16/S3	3
A17/S4	4
A18/S5	5
A19/S6	6

Bus Control	
ALE/QS0	10
$\overline{BHE}$ ($\overline{RFSH}$)	7
$\overline{S0}$	23
$\overline{S1}$	22
$\overline{S2}$	21
$\overline{RD}$/$\overline{QSMD}$	9
$\overline{WR}$/QS1	8
ARDY	20
SRDY	27
$\overline{DEN}$	38
DT/$\overline{R}$	37
$\overline{LOCK}$	28
HOLD	26
HLDA	25

No Connection	
N.C.	2
N.C.	11
N.C.	14
N.C.	15
N.C.	24
N.C.	43
N.C.	44
N.C.	62
N.C.	63

Processor Control	
$\overline{RES}$	55
RESET	18
X1	16
X2	17
CLKOUT	19
$\overline{TEST}$/BUSY	29
NMI	30
INT0	31
INT1/$\overline{SELECT}$	32
INT2/$\overline{INTA0}$	35
INT3/$\overline{INTA1}$	36

Power and Ground	
V_{CC}	33
V_{CC}	34
V_{CC}	72
V_{CC}	73
V_{SS}	12
V_{SS}	13
V_{SS}	53

I/O	
$\overline{UCS}$	45
$\overline{LCS}$	46
$\overline{MCS0}$/PEREQ	39
$\overline{MCS1}$/$\overline{ERROR}$	40
$\overline{MCS2}$	41
$\overline{MCS3}$/$\overline{NPS}$	42
$\overline{PCS0}$	54
$\overline{PCS1}$	52
$\overline{PCS2}$	51
$\overline{PCS3}$	50
$\overline{PCS4}$	49
$\overline{PCS5}$/A1	48
$\overline{PCS6}$/A2	47
TMR IN 0	59
TMR IN 1	58
TMR OUT 0	57
TMR OUT 1	56
DRQ0	61
DRQ1	60

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 7. QFP Pin Locations with Pin Names

1	AD15 (A15)
2	N.C.
3	A16/S3
4	A17/S4
5	A18/S5
6	A19/S6
7	$\overline{BHE}$/($\overline{RFSH}$)
8	$\overline{WR}$/QS1
9	$\overline{RD}$/$\overline{QSMD}$
10	ALE/QS0
11	N.C.
12	V_{SS}
13	V_{SS}
14	N.C.
15	N.C.
16	X1
17	X2
18	RESET
19	CLKOUT
20	ARDY

21	$\overline{S2}$
22	$\overline{S1}$
23	$\overline{S0}$
24	N.C.
25	HLDA
26	HOLD
27	SRDY
28	$\overline{LOCK}$
29	$\overline{TEST}$/BUSY
30	NMI
31	INT0
32	INT1/$\overline{SELECT}$
33	V_{CC}
34	V_{CC}
35	INT2/$\overline{INTA0}$
36	INT3/$\overline{INTA1}$
37	DT/$\overline{R}$
38	$\overline{DEN}$
39	$\overline{MCS0}$/PEREQ
40	$\overline{MCS1}$/$\overline{ERROR}$

41	$\overline{MCS2}$
42	$\overline{MCS3}$/$\overline{NPS}$
43	N.C.
44	N.C.
45	$\overline{UCS}$
46	$\overline{LCS}$
47	$\overline{PCS6}$/A2
48	$\overline{PCS5}$/A1
49	$\overline{PCS4}$
50	$\overline{PCS3}$
51	$\overline{PCS2}$
52	$\overline{PCS1}$
53	V_{SS}
54	$\overline{PCS0}$
55	$\overline{RES}$
56	TMR OUT 1
57	TMR OUT 0
58	TMR IN 1
59	TMR IN 0
60	DRQ1

61	DRQ0
62	N.C.
63	N.C.
64	AD0
65	AD8 (A8)
66	AD1
67	AD9 (A9)
68	AD2
69	AD10 (A10)
70	AD3
71	AD11 (A11)
72	V_{CC}
73	V_{CC}
74	AD4
75	AD12 (A12)
76	AD5
77	AD13 (A13)
78	AD6
79	AD14 (A14)
80	AD7

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 8. SQFP Pin Functions with Location

AD Bus	
AD0	1
AD1	3
AD2	6
AD3	8
AD4	12
AD5	14
AD6	16
AD7	18
AD8 (A8)	2
AD9 (A9)	5
AD10 (A10)	7
AD11 (A11)	9
AD12 (A12)	13
AD13 (A13)	15
AD14 (A14)	17
AD15 (A15)	19
A16/S3	21
A17/S4	22
A18/S5	23
A19/S6	24

Bus Control	
ALE/QS0	29
$\overline{BHE}$ ($\overline{RFSH}$)	26
$\overline{S0}$	40
$\overline{S1}$	39
$\overline{S2}$	38
$\overline{RD}$/$\overline{QSMD}$	28
$\overline{WR}$/QS1	27
ARDY	37
SRDY	44
$\overline{DEN}$	56
DT/$\overline{R}$	54
$\overline{LOCK}$	45
HOLD	43
HLDA	42

No Connection	
N.C.	4
N.C.	25
N.C.	35
N.C.	55
N.C.	72

Processor Control	
$\overline{RES}$	73
RESET	34
X1	32
X2	33
CLKOUT	36
$\overline{TEST}$/BUSY	46
NMI	47
INT0	48
INT1/$\overline{SELECT}$	49
INT2/$\overline{INTA0}$	52
INT3/$\overline{INTA1}$	53

Power and Ground	
V_{CC}	10
V_{CC}	11
V_{CC}	20
V_{CC}	50
V_{CC}	51
V_{CC}	61
V_{SS}	30
V_{SS}	31
V_{SS}	41
V_{SS}	70
V_{SS}	80

I/O	
$\overline{UCS}$	62
$\overline{LCS}$	63
$\overline{MCS0}$/PEREQ	57
$\overline{MCS1}$/$\overline{ERROR}$	58
$\overline{MCS2}$	59
$\overline{MCS3}$/$\overline{NPS}$	60
$\overline{PCS0}$	71
$\overline{PCS1}$	69
$\overline{PCS2}$	68
$\overline{PCS3}$	67
$\overline{PCS4}$	66
$\overline{PCS5}$/A1	65
$\overline{PCS6}$/A2	64
TMR IN 0	77
TMR IN 1	76
TMR OUT 0	75
TMR OUT 1	74
DRQ0	79
DRQ1	78

NOTE:
Pin names in parentheses apply to the 80C188XL.

Table 9. SQFP Pin Locations with Pin Names

1	AD0
2	AD8 (A8)
3	AD1
4	N.C.
5	AD9 (A9)
6	AD2
7	AD10 (A10)
8	AD3
9	AD11 (A11)
10	V_{CC}
11	V_{CC}
12	AD4
13	AD12 (A12)
14	AD5
15	AD13 (A13)
16	AD6
17	AD14 (A14)
18	AD7
19	AD15 (A15)
20	V_{CC}

21	A16/S3
22	A17/S4
23	A18/S5
24	A19/S6
25	N.C.
26	$\overline{BHE}$ ($\overline{RFSH}$)
27	$\overline{WR}$/QS1
28	$\overline{RD}$/$\overline{QSMD}$
29	ALE/QS0
30	V_{SS}
31	V_{SS}
32	X1
33	X2
34	RESET
35	N.C.
36	CLKOUT
37	ARDY
38	$\overline{S2}$
39	$\overline{S1}$
40	$\overline{S0}$

41	V_{SS}
42	HLDA
43	HOLD
44	SRDY
45	$\overline{LOCK}$
46	$\overline{TEST}$/BUSY
47	NMI
48	INT0
49	INT1/$\overline{SELECT}$
50	V_{CC}
51	V_{CC}
52	INT2/$\overline{INTA0}$
53	INT3/$\overline{INTA1}$
54	DT/$\overline{R}$
55	N.C.
56	$\overline{DEN}$
57	$\overline{MCS0}$/PEREQ
58	$\overline{MCS1}$/$\overline{ERROR}$
59	$\overline{MCS2}$
60	$\overline{MCS3}$/$\overline{NPS}$

61	V_{CC}
62	$\overline{UCS}$
63	$\overline{LCS}$
64	$\overline{PCS6}$/A2
65	$\overline{PCS5}$/A1
66	$\overline{PCS4}$
67	$\overline{PCS3}$
68	$\overline{PCS2}$
69	$\overline{PCS1}$
70	V_{SS}
71	$\overline{PCS0}$
72	N.C.
73	$\overline{RES}$
74	TMR OUT 1
75	TMR OUT 0
76	TMR IN 1
77	TMR IN 0
78	DRQ1
79	DRQ0
80	V_{SS}

NOTE:
Pin names in parentheses apply to the 80C188XL.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Ambient Temperature under Bias . . . . 0°C to +70°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . . −1.0V to +7.0V

Package Power Dissipation 1W

Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTICE: The specifications are subject to change without notice.

DC SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL1}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V (4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 µA @ V_{CC} −0.5(4)
I_{CC}	Power Supply Current		100	mA	@ 25 MHz, 0°C V_{CC} = 5.5V(3)
			90	mA	@ 20 MHz, 0°C V_{CC} = 5.5V(3)
			62.5	mA	@ 12 MHz, 0°C V_{CC} = 5.5V (3)
			100	µA	@ DC 0°C V_{CC} = 5.5V
I_{LI}	Input Leakage Current		±10	µA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	µA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA

DC SPECIFICATIONS (Continued) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CHO}	Clock Output High	$V_{CC} - 0.5$		V	$I_{CHO} = -500\ \mu A$
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:
1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$ and $\overline{TEST}$/BUSY pins have internal pullup devices. Loading some of these pins above $I_{OH} = -200\ \mu A$ can cause the processor to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

Power Supply Current

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by $I_{CC} = 5\ mA \times$ freq. (MHz) + I_{QL}.

I_{QL} is the quiescent leakage current when the clock is static. I_{QL} is typically less than 100 μA.

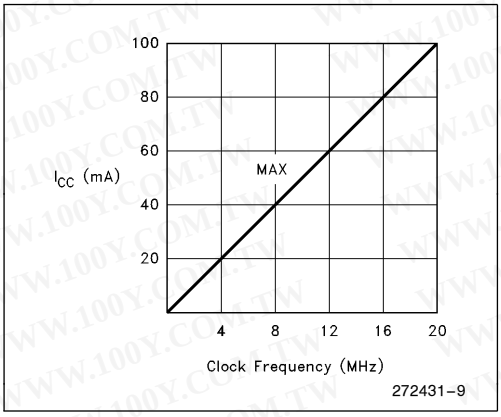


Figure 5. I_{CC} vs Frequency

AC SPECIFICATIONS

MAJOR CYCLE TIMINGS (READ CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	8		10		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	3	20	3	27	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 8		T_{CHCL} − 10		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	T_{CLAX}	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	3	25	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	3	20	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	17	3	22	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	17	3	22	3	37	ns	
T_{CHCTV}	Control Active Delay 2	3	20	3	22	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	17	3	22	3	37	ns	

AC SPECIFICATIONS (Continued)

MAJOR CYCLE TIMINGS (READ CYCLE) (Continued)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL TIMING RESPONSES (Read Cycle)									
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	20	3	27	3	37	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL}$ − 15		$2T_{CLCL}$ − 20		$2T_{CLCL}$ − 25		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	20	3	27	3	37	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	Equal Loading

AC SPECIFICATIONS (Continued)

MAJOR CYCLE TIMINGS (WRITE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	3	20	3	27	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 10		T_{CHCL} − 10		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	20	3	25	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	17	3	25	3	37	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	3	25	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	3	20	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	17	3	22	3	37	ns	
80C186XL TIMING RESPONSES (Write Cycle)									
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ − 15		$2T_{CLCL}$ − 20		$2T_{CLCL}$ − 25		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	T_{CLCL} − 10		T_{CLCL} − 15		T_{CLCL} − 20		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading

AC SPECIFICATIONS (Continued)

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	8		10		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	3	20	3	27	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 10		T_{CLCH} − 10		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} − 10		T_{CHCL} − 10		T_{CHCL} − 15		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	T_{CLAX}	25	ns	
T_{CVCTV}	Control Active Delay 1	3	17	3	25	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	17	3	25	3	37	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	3	22	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	17	3	22	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	17	3	22	3	37	ns	

AC SPECIFICATIONS (Continued)

SOFTWARE HALT CYCLE TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{CHSV}	Status Active Delay	3	20	3	25	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	20	3	25	3	35	ns	
T_{CLAV}	Address Valid Delay	3	20	3	27	3	36	ns	
T_{CHLH}	ALE Active Delay		20		20		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20		25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	3	22	3	37	ns	

AC SPECIFICATIONS (Continued)

CLOCK TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL CLKIN REQUIREMENTS(1)									
T_{CKIN}	CLKIN Period	20	∞	25	∞	40	∞	ns	
T_{CLCK}	CLKIN Low Time	8	∞	10	∞	16	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	8	∞	10	∞	16	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5		5	ns	1.0 to 3.5V
80C186XL CLKOUT TIMING									
T_{CICO}	CLKIN to CLKOUT Skew		17		17		21	ns	
T_{CLCL}	CLKOUT Period	40	∞	50		80	∞	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		6		8		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		6		8		10	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V. T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V. T_A = 0°C.

AC SPECIFICATIONS (Continued)

READY, PERIPHERAL AND QUEUE STATUS TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL READY AND PERIPHERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	8		10		15		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	8		10		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	8		10		15		ns	
T_{CLARX}	ARDY Active Hold Time(1)	8		10		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	8		10		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	10		15		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	8		10		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	8		10		15		ns	
80C186XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES									
T_{CLTMV}	Timer Output Delay		17		22		33	ns	
T_{CHQSV}	Queue Status Delay		22		27		32	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

AC SPECIFICATIONS (Continued)

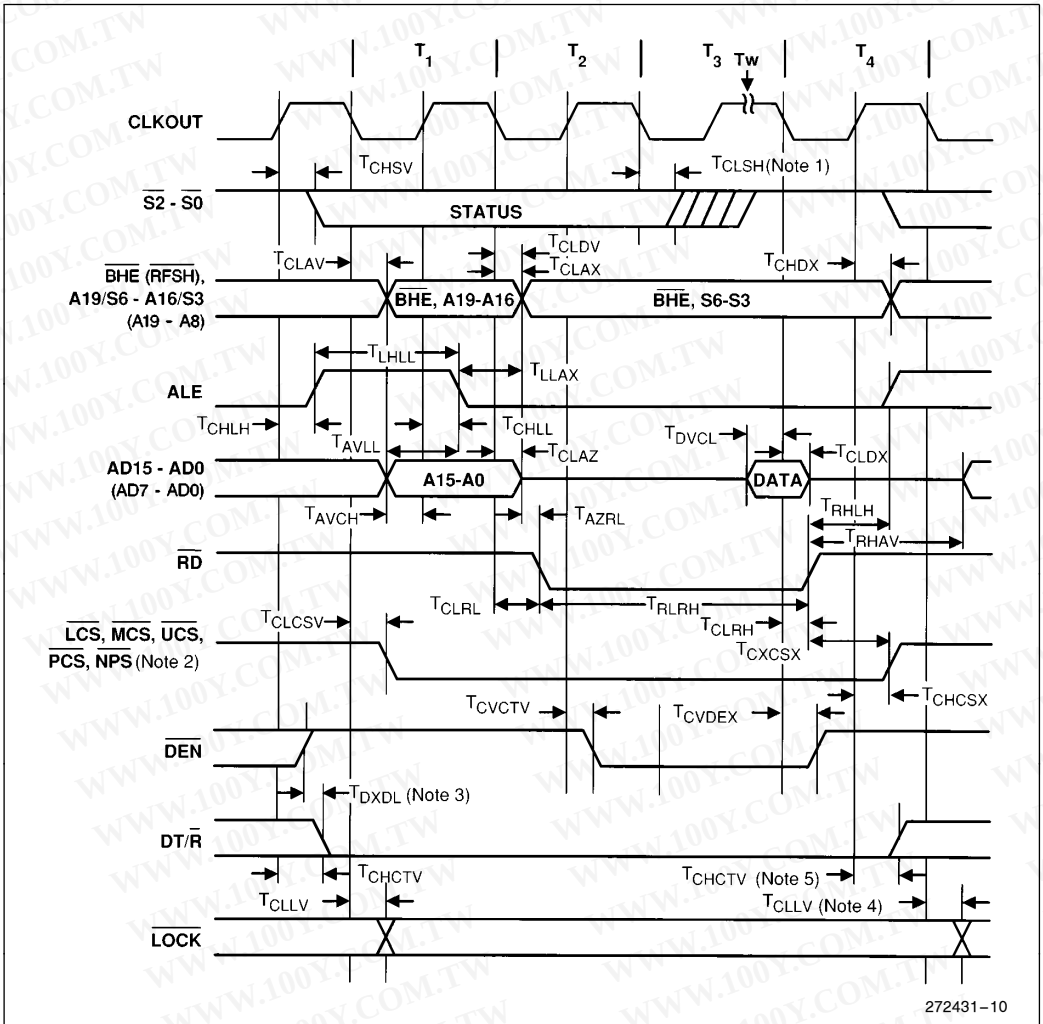
RESET AND HOLD/HLDA TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values						Unit	Test Conditions
		80C186XL25		80C186XL20		80C186XL12			
		Min	Max	Min	Max	Min	Max		
80C186XL RESET AND HOLD/HLDA TIMING REQUIREMENTS									
T_{RESIN}	$\overline{RES}$ Setup	15		15		15		ns	
T_{HVCL}	HOLD Setup(1)	8		10		15		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	T_{CLAX}	25	ns	
T_{CLAV}	Address Valid Delay	3	20	3	22	3	36	ns	
80C186XL RESET AND HOLD/HLDA TIMING RESPONSES									
T_{CLRO}	Reset Delay		17		22		33	ns	
T_{CLHAV}	HLDA Valid Delay	3	17	3	22	3	33	ns	
T_{CHCZ}	Command Lines Float Delay		22		25		33	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		20		26		36	ns	

NOTE:
1. To guarantee recognition at next clock.

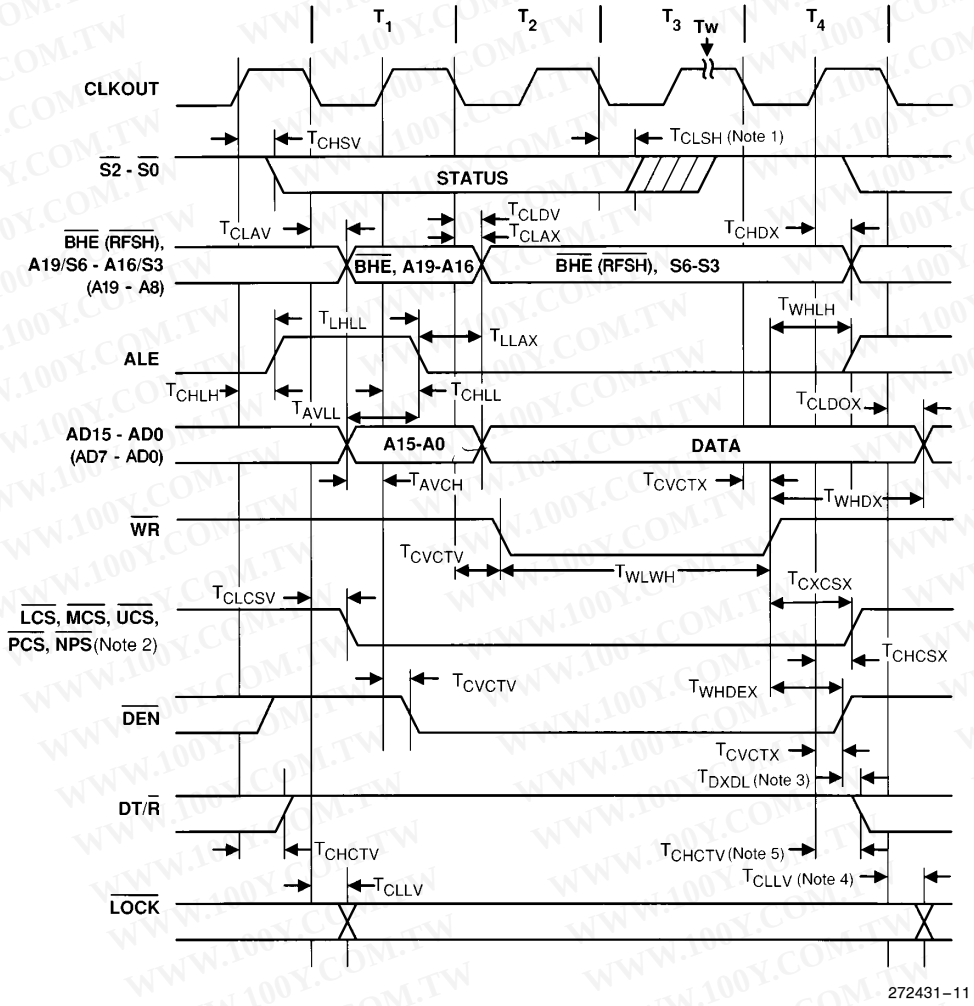
AC SPECIFICATIONS (Continued)



NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.
Pin names in parentheses apply to the 80C188XL.

Figure 6. Read Cycle Waveforms

AC SPECIFICATIONS (Continued)

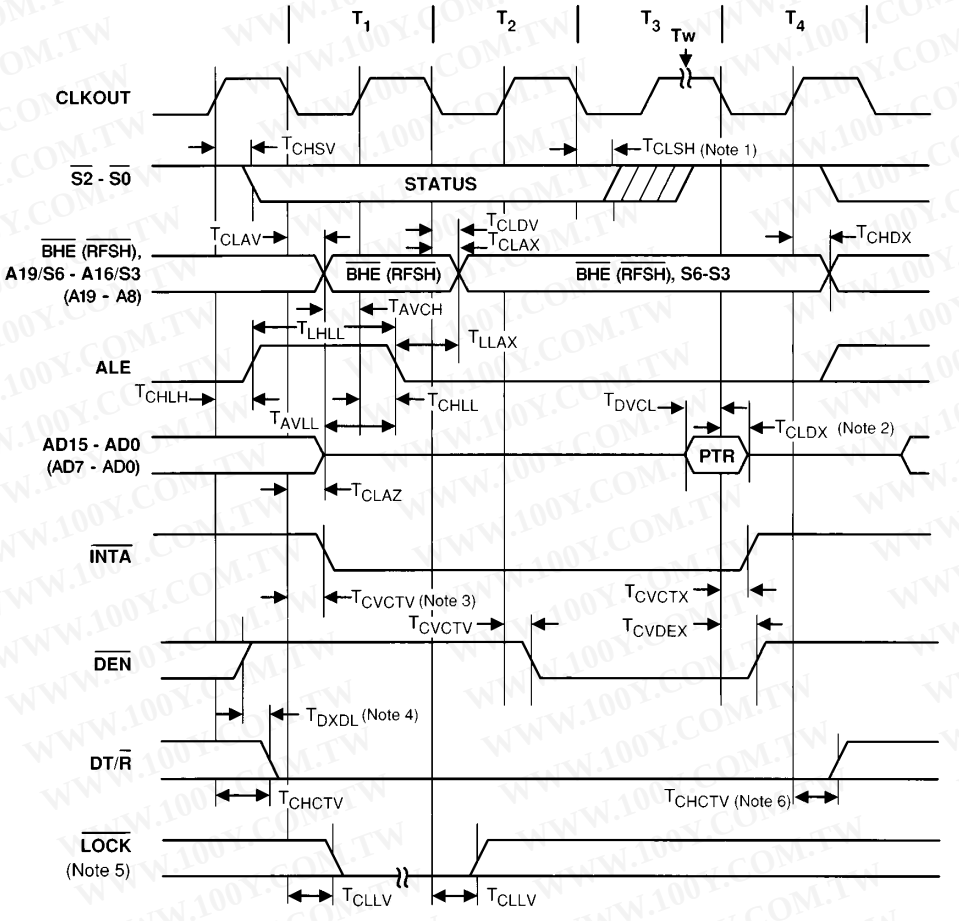


NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

Pin names in parentheses apply to the 80C188XL.

Figure 7. Write Cycle Waveforms

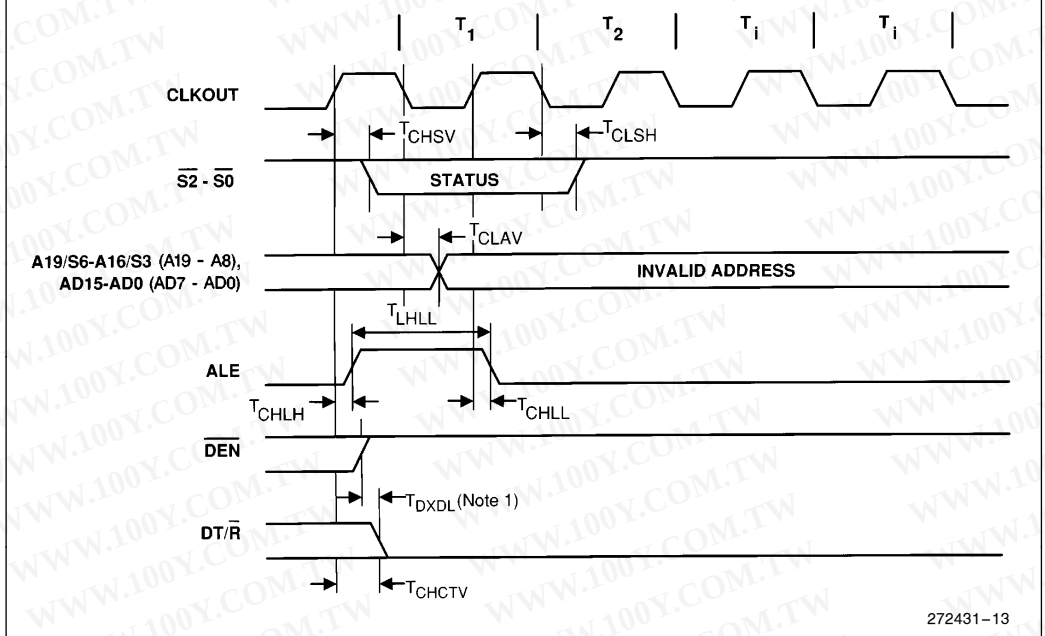
AC SPECIFICATIONS (Continued)



NOTES:
1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX} (min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.
6. Changes in T-state preceding next bus cycle if followed by write.
Pin names in parentheses apply to the 80C188XL.

Figure 8. Interrupt Acknowledge Cycle Waveforms

AC SPECIFICATIONS (Continued)



NOTE:
1. For write cycle followed by halt cycle.
Pin names in parentheses apply to the 80C188XL.

Figure 9. Software Halt Cycle Waveforms

WAVEFORMS

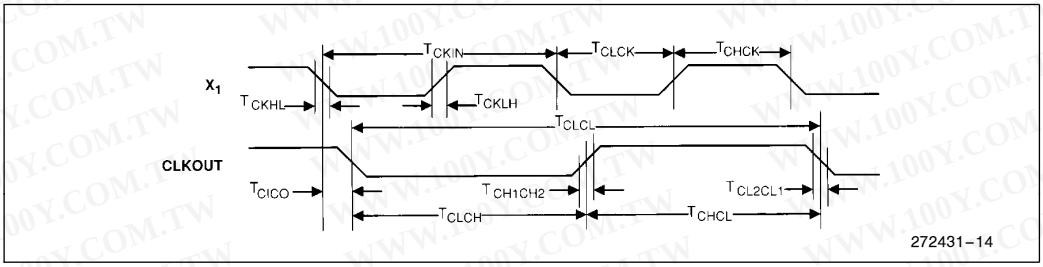


Figure 10. Clock Waveforms

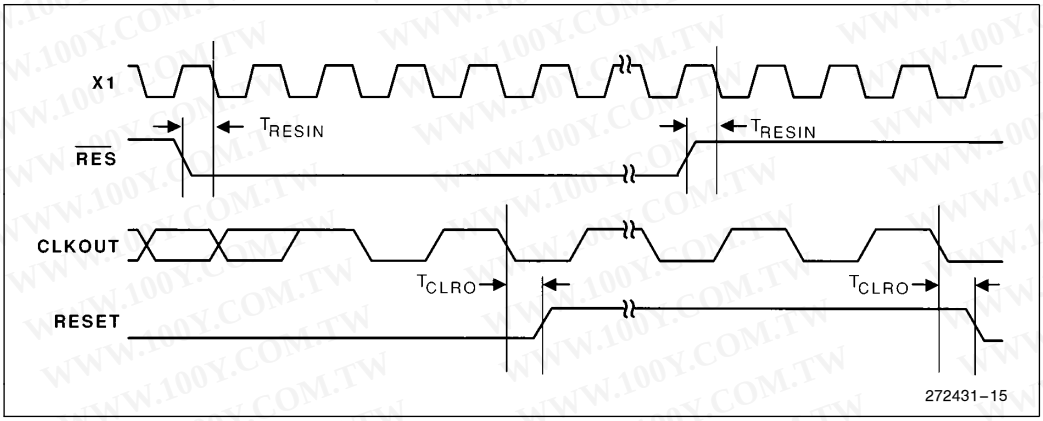


Figure 11. Reset Waveforms

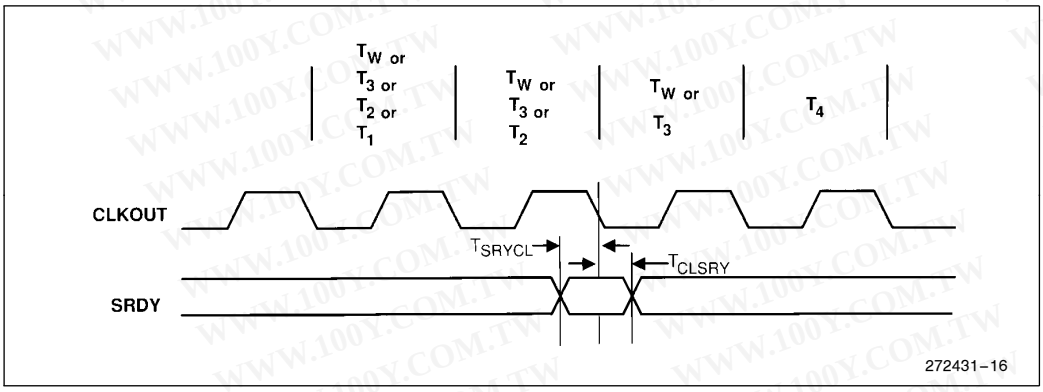


Figure 12. Synchronous Ready (SRDY) Waveforms

AC CHARACTERISTICS

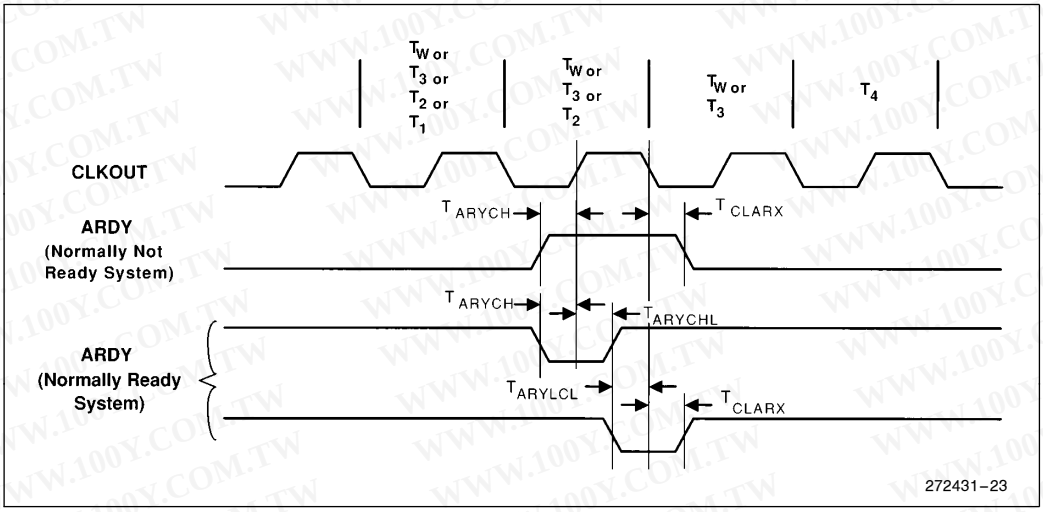


Figure 13. Asynchronous Ready (ARDY) Waveforms

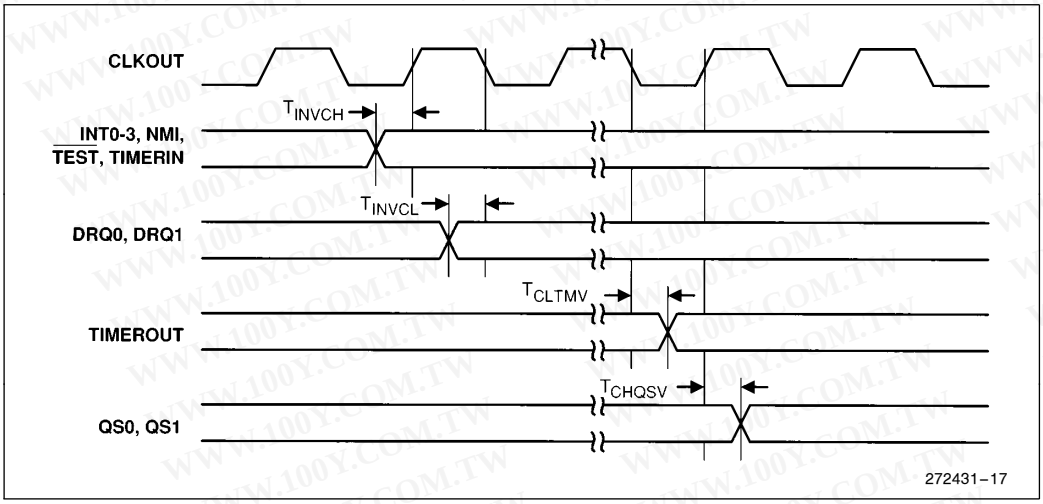


Figure 14. Peripheral and Queue Status Waveforms

AC CHARACTERISTICS (Continued)

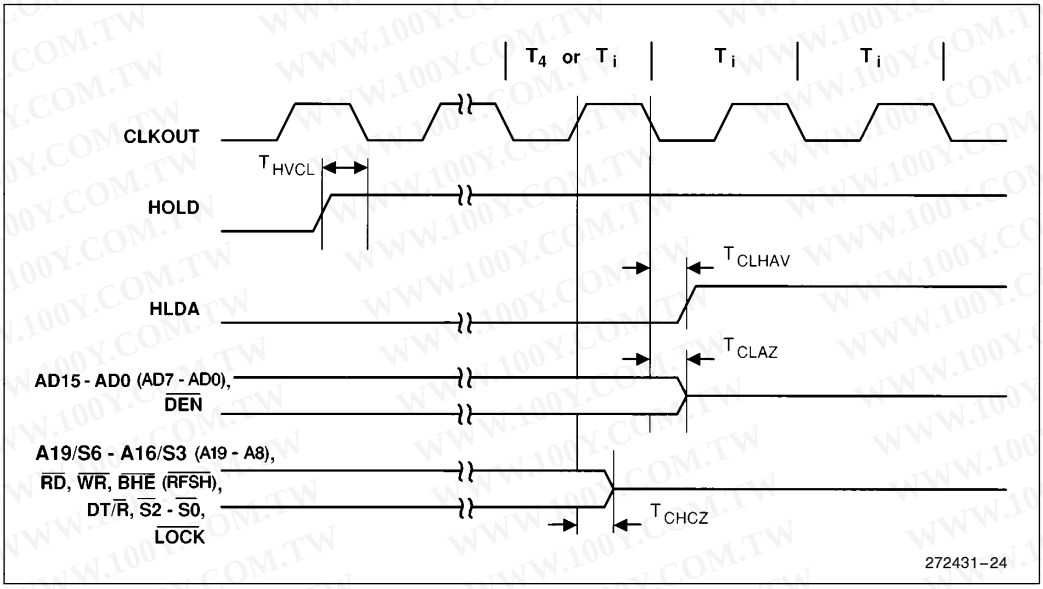


Figure 15. HOLDA/HLDA Waveforms (Entering Hold)

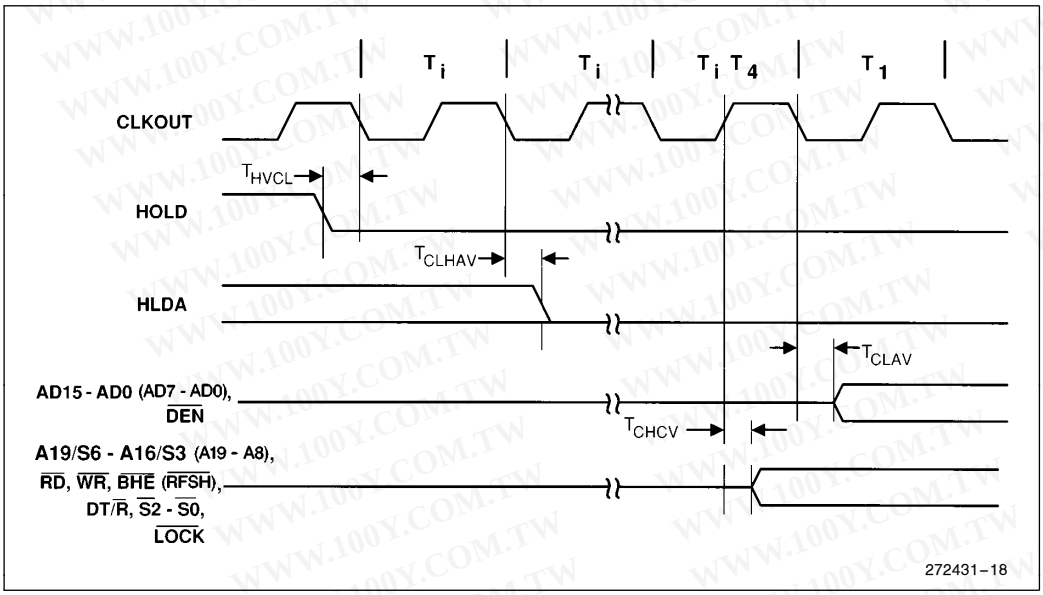


Figure 16. HOLD/HLDA Waveforms (Leaving Hold)

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
OUT: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV} — Time from Clock low to Address valid
T_{CHLH} — Time from Clock high to ALE high
T_{CLCSV} — Time from Clock low to Chip Select valid

DERATING CURVES

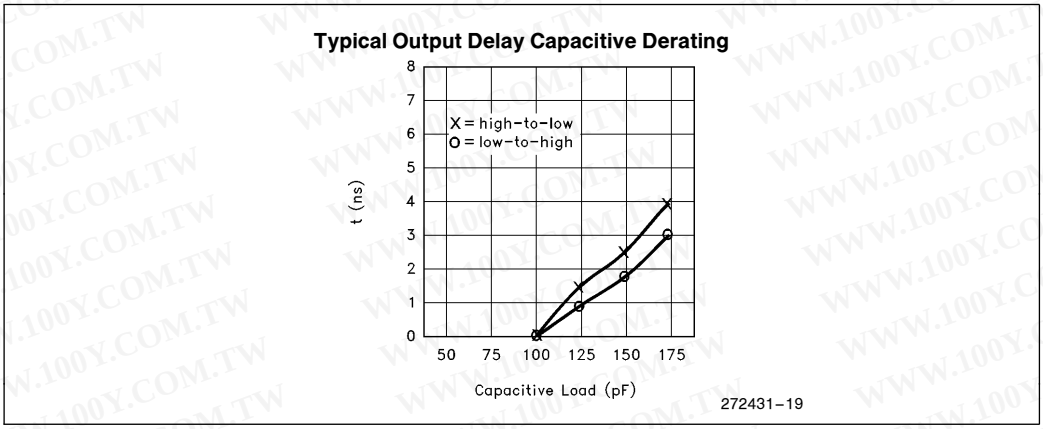


Figure 17. Capacitive Derating Curve

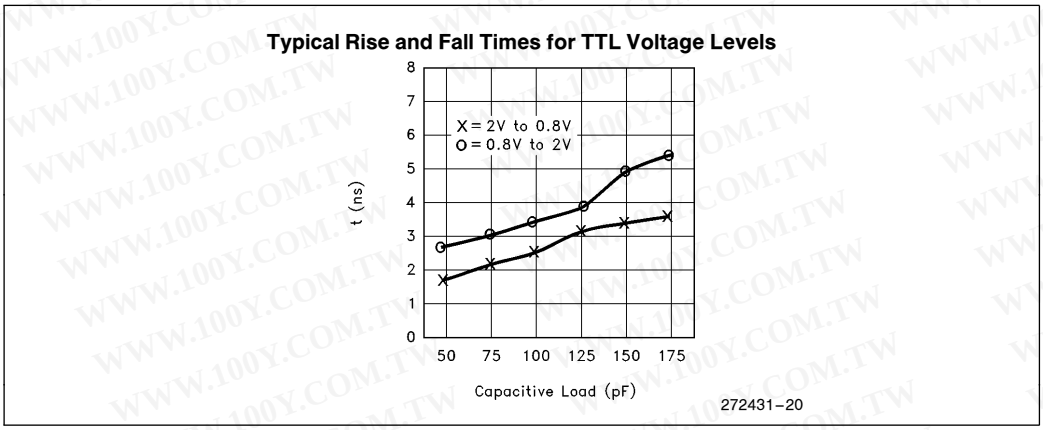


Figure 18. TTL Level Rise and Fall Times for Output Buffers

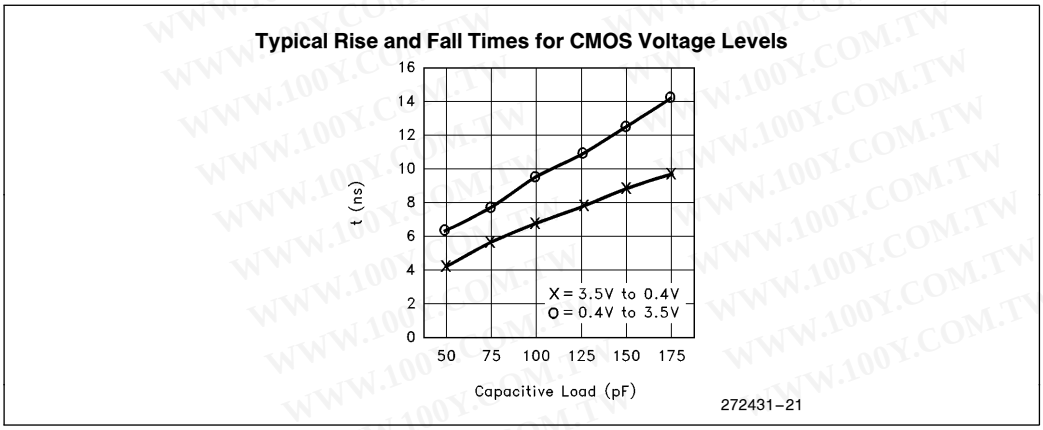


Figure 19. CMOS Level Rise and Fall Times for Output Buffers

80C186XL/80C188XL EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80C186XL microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The 80C186XL EXPRESS program includes an extended temperature range. With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 10. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 10. Prefix Identification

Prefix	Package Type	Temperature Range
A	PGA	Commercial
N	PLCC	Commercial
R	LCC	Commercial
S	QFP	Commercial
SB	SQFP	Commercial
TA	PGA	Extended
TN	PLCC	Extended
TR	LCC	Extended
TS	QFP	Extended

80C186XL/80C188XL EXECUTION TIMINGS

A determination of program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries (80C186XL only).

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186XL has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue (6 bytes) most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

The 80C188XL 8-bit BIU is limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue (4 bytes) much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.