87C196KC
16-BIT HIGH-PERFORMANCE CHMOS MICROCONTROLLER

Automotive

- −40°C to +125°C
- 16 Kbytes of On-Chip EPROM
- 232 Byte Register File
- 256 Bytes of Additional RAM
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- Peripheral Transaction Server
- 1.75 μs 16 x 16 Multiply (16 MHz)
- 3.0 μs 32/16 Divide (16 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High-Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- 3 Pulse-Width-Modulated Outputs
- Four 16-Bit Software Timers
- 8- or 10-Bit 8-Channel A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ Bus Protocol
- OTP One-Time Programmable and QROM Versions
- Available in 12 MHz and 16 MHz Versions
- 16 MHz Operation

The 87C196KC 16-bit microcontroller is a high-performance member of the MCS® 96 microcontroller family. The 87C196KC is an enhanced 8XC196KB device with 488 bytes RAM, 16 MHz operation and 16 Kbytes of on-chip EPROM. Intel's CHMOS process provides a high performance processor along with low power consumption.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

NOTICE:
This datasheet contains information on products in full production. Specifications within this datasheet are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

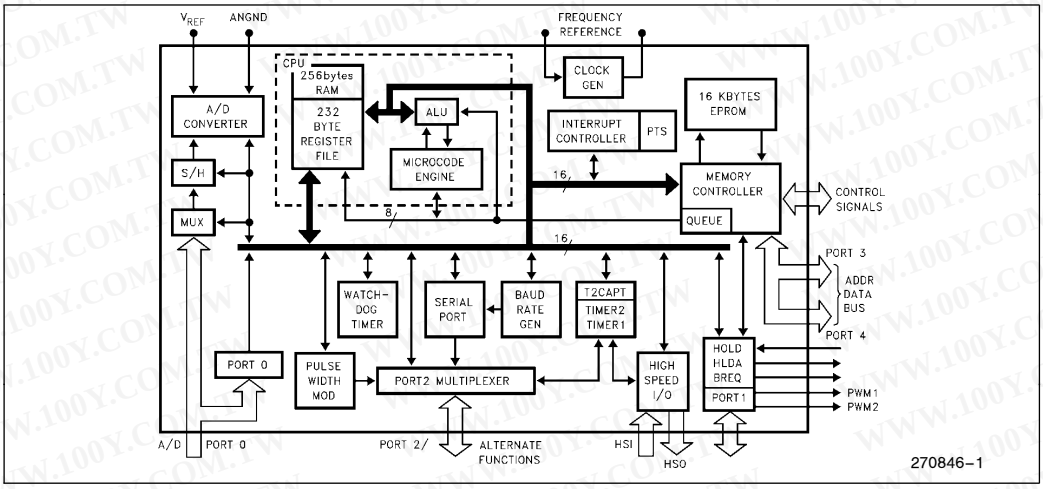


Figure 1. 87C196KC Block Diagram

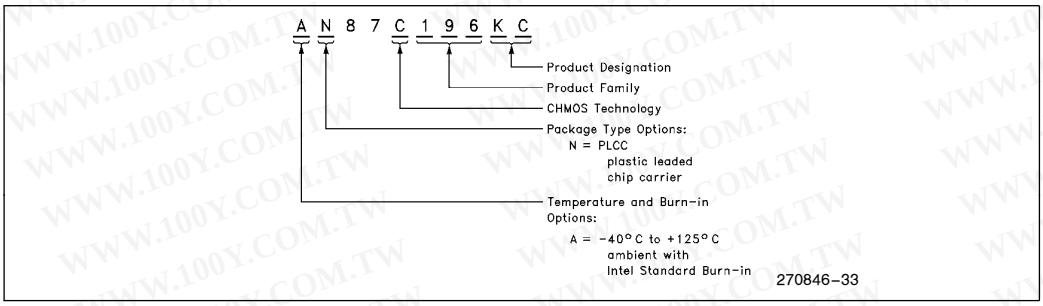


Figure 2. The 87C196KC Family Nomenclature

87C196KC Enhanced Feature Set over the 87C196KB

1. The 87C196KC has twice the RAM and twice the EPROM of the 87C196KB. Also, a Vertical Register Windowing Scheme allows the extra 256 bytes of RAM to be used as registers. This greatly reduces the context switching time.
2. Peripheral Transaction Server (PTS). The PTS is an alternative way to service an interrupt, reducing latency and overhead. Each interrupt can be mapped to its PTS channel, which acts like a DMA channel. Each interrupt can now do a single or block transfer, without executing an Interrupt service routine. Special PTS modes exist for the A/D converter, HSI, and HSO.
3. Two extra Pulse Width Modulated outputs. The 87C196KC has added 2 PWM outputs that are functionally compatible to the 87C196KB PWM.
4. Timer2 Internal Clocking. Timer2 can now be clocked with an internal source, every 1 or 8 state times.
5. The A/D can now perform an 8- as well as a 10-bit conversion. 8-bit conversion allows for a faster conversion time.
6. Additional On-chip Memory Security. Two UPROM (Uneraseable Programmable Read Only Memory) bits can be programmed to disable the bus controller for external code and data fetches. Once programmed, a UPROM bit cannot be erased. By shutting off the bus controller for external fetches, no one can try and gain access to your code by executing from external memory.
7. New Instructions. The 87C196KC has 5 new instructions. An exchange (XCHB/XCHW) instruction swaps two memory locations, an Interruptable Block Move Instruction (BMOVI), a Table Indirect Jump (TIJMP) instruction, and two instructions for enabling and disabling the PTS (EPTS/DPTS).

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PACKAGING

PLCC	Description	PLCC	Description	PLCC	Description
9	ACH7/P0.7	54	AD6/P3.6	31	P1.6/$\overline{\text{HLDA}}$
8	ACH6/P0.6	53	AD7/P3.7	30	P1.5/$\overline{\text{BREQ}}$
7	ACH2/P0.2	52	AD8/P4.0	29	HSO.1
6	ACH0/P0.0	51	AD9/P4.1	28	HSO.0
5	ACH1/P0.1	50	AD10/P4.2	27	HSO.5/HSI.3
4	ACH3/P0.3	49	AD11/P4.3	26	HSO.4/HSI.2
3	NMI	48	AD12/P4.4	25	HSI.1
2	$\overline{\text{EA}}$	47	AD13/P4.5	24	HSI.0
1	V_{CC}	46	AD14/P4.6	23	P1.4/PWM2
68	V_{SS}	45	AD15/P4.7	22	P1.3/PWM1
67	XTAL1	44	T2CLK/P2.3	21	P1.2
66	XTAL2	43	READY	20	P1.1
65	CLKOUT	42	T2RST/P2.4	19	P1.0
64	BUSWIDTH	41	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	18	TXD/P2.0
63	INST	40	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	17	RXD/P2.1
62	ALE/$\overline{\text{ADV}}$	39	PWM0/P2.5	16	$\overline{\text{RESET}}$
61	$\overline{\text{RD}}$	38	P2.7/T2CAPTURE	15	EXTINT/P2.2
60	AD0/P3.0	37	V_{PP}	14	V_{SS}
59	AD1/P3.1	36	V_{SS}	13	V_{REF}
58	AD2/P3.2	35	HSO.3	12	ANGND
57	AD3/P3.3	34	HSO.2	11	ACH4/P.04
56	AD4/P3.4	33	P2.6/T2UP-DN	10	ACH5/P.05
55	AD5/P3.5	32	P1.7/$\overline{\text{HOLD}}$		

Figure 3. 68-Pin PLCC Functional Pin-out

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

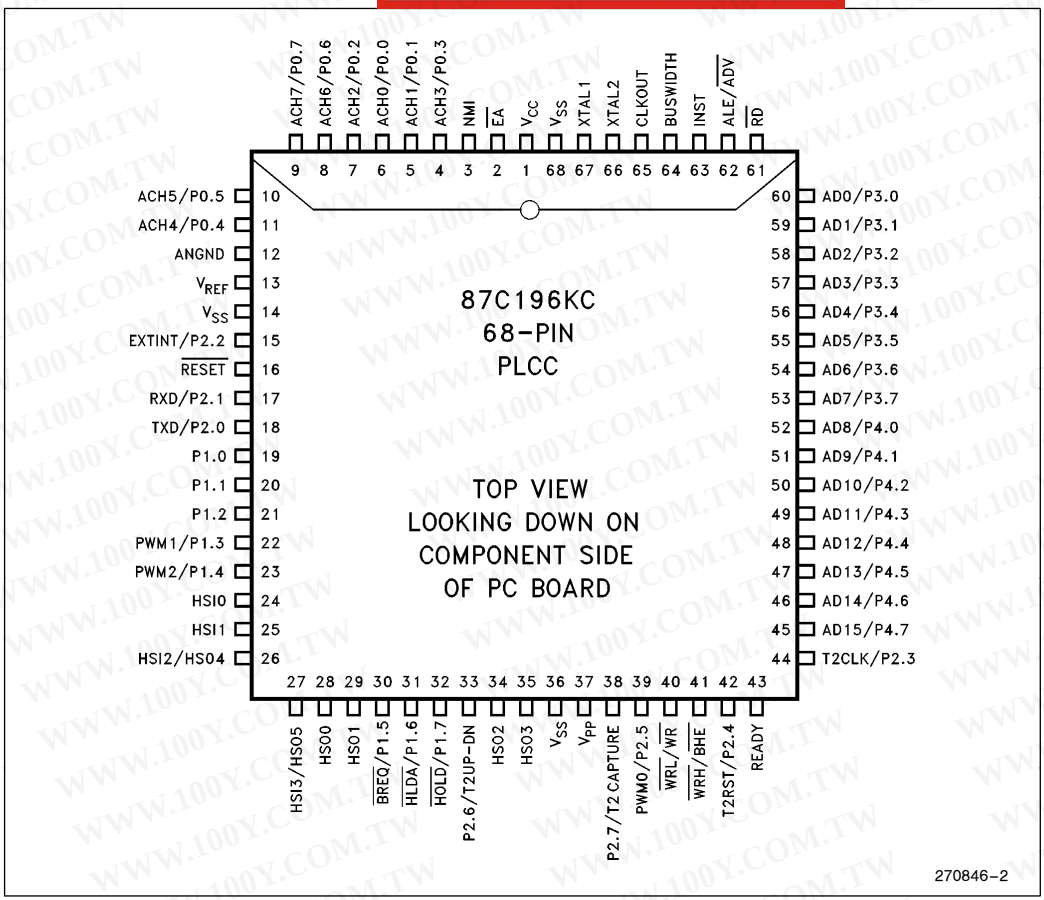


Figure 4. 68-Pin PLCC Package

Table 1. Prefix Identification

	PLCC
87C196KC	AN87C196KC*

*OTP Version

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used V_{PP} may be tied to V_{CC}. This pin is the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input to the chip.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to those locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KC.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.

ELECTRICAL CHARACTERISTICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias . . . . . −40°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin to V_{SS} . . . . . −0.5V to +7.0V
Power Dissipation 0.43W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1, EA	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.2 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA
V_{OH2}	Output High Voltage in RESET on P2.0 (Note 2)	2.0		V	I_{OH} = −0.6 mA

NOTES:
1. All pins except $\overline{\text{RESET}}$, XTAL1 and $\overline{\text{EA}}$.
2. Violating these specifications in Reset may cause the part to enter test modes.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

DC CHARACTERISTICS (Over Specified Operating Conditions)

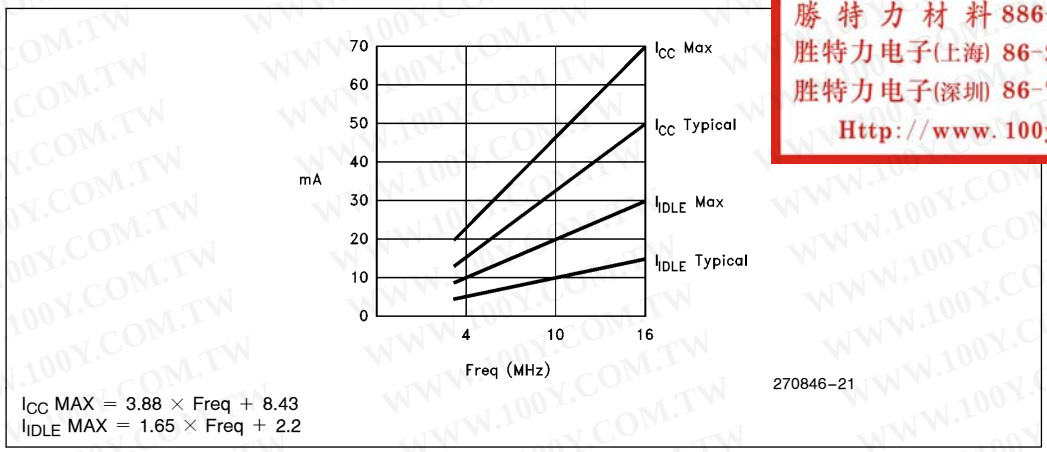
Symbol	Description	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	µA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	µA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	µA	$V_{IN} = 0.45V$
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	
I_{PD}	Powerdown Mode Current		50	T.B.D.	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	$V_{CC} = 5.0V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw



I_{CC} MAX = 3.88 × Freq + 8.43
I_{IDLE} MAX = 1.65 × Freq + 2.2

Figure 5. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 87C196KC:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 75	ns	
T_{LLYV}	ALE Low to READY Setup		T_{OSC} − 70	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 75	ns	
T_{LLGV}	ALE Low to Buswidth Setup		T_{OSC} − 60	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 30	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 50	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AC CHARACTERISTICS (Continued)

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

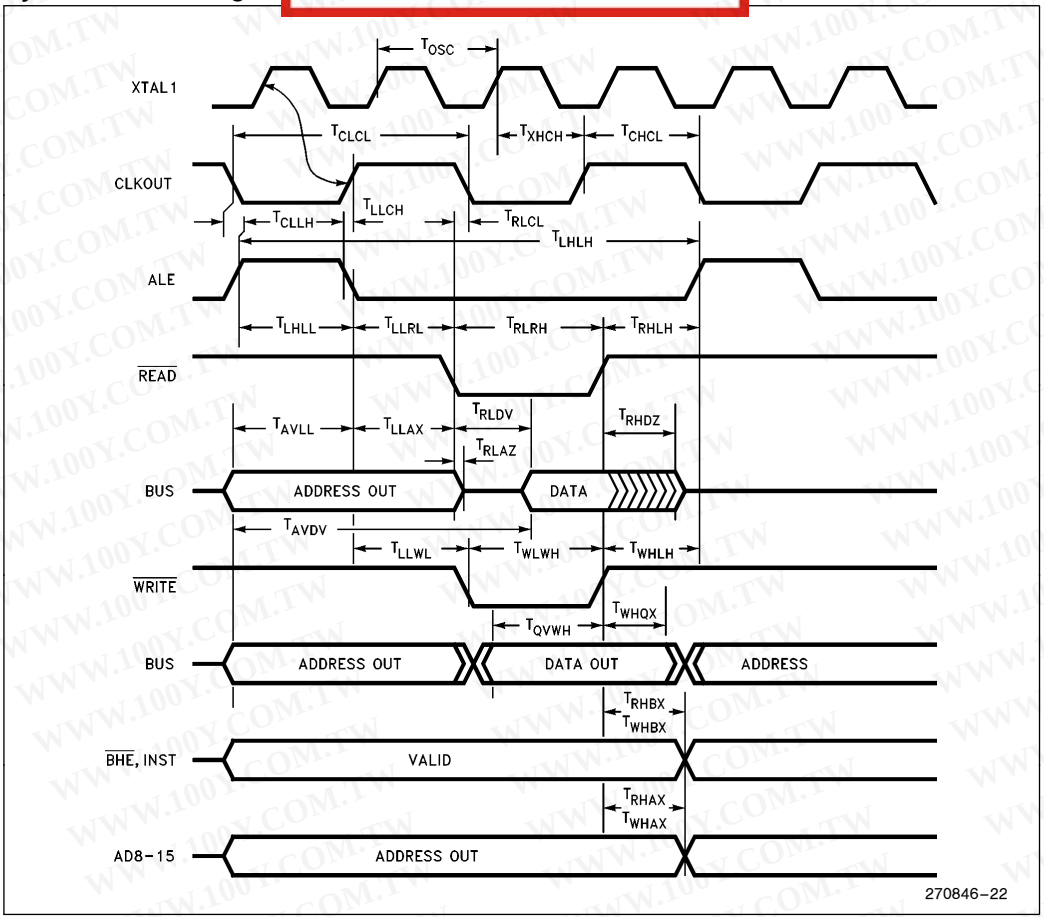
The 87C196KC will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on $XTAL_1$	4.0	16	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$	62.5	250	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns	
T_{CLCL}	CLKOUT Cycle Time	$2\,T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC} - 10$	$T_{OSC} + 15$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	$4\,T_{OSC}$		ns	(Note 4)
T_{LHLL}	ALE High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC} - 15$			
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC} - 30$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	0	35	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 30$			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 30$		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 25$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC} - 10$	$T_{OSC} + 15$	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	$T_{OSC} - 30$		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	$T_{OSC} - 30$		ns	(Note 3)

NOTES:
1. Testing performed at 4.0 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

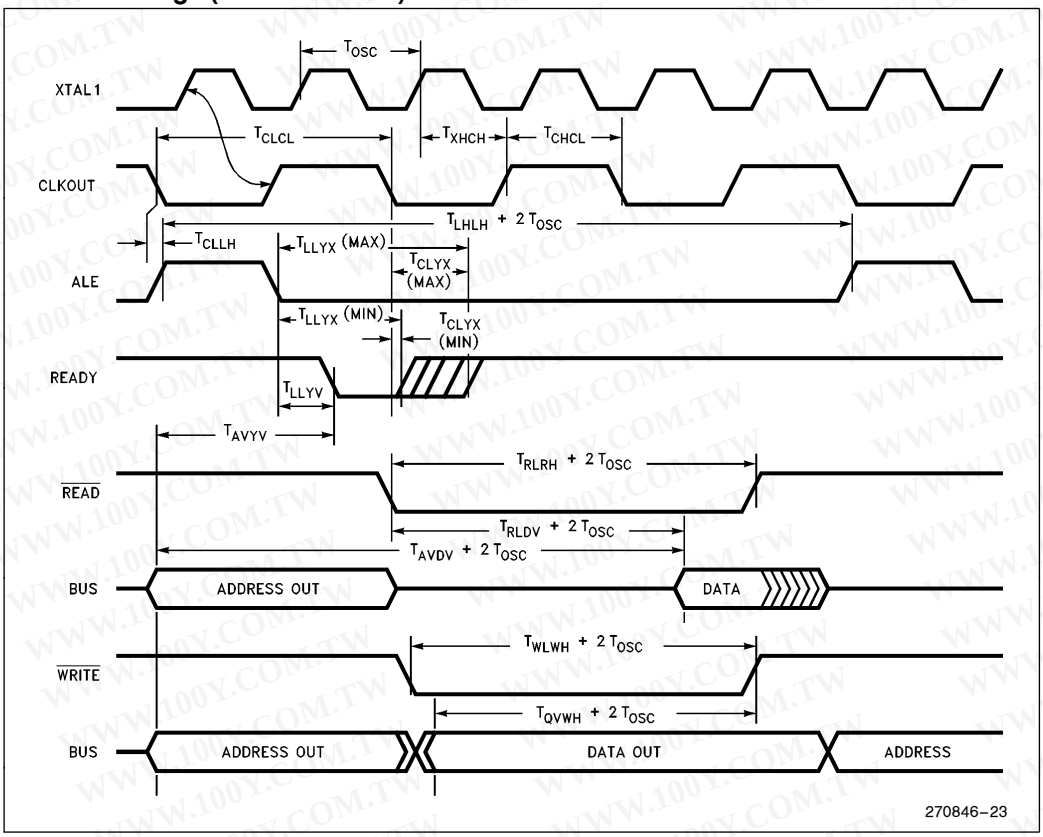
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

System Bus Timings

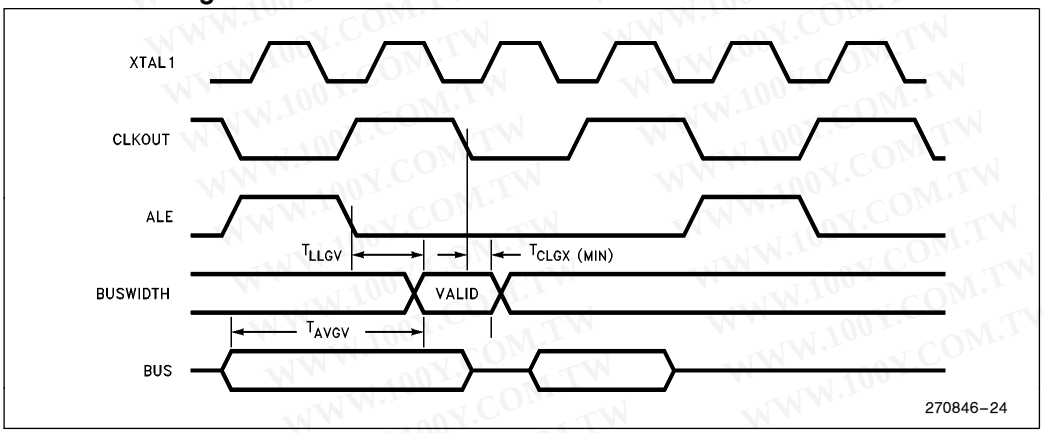


勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

READY Timings (One Waitstate)



Buswidth Timings



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

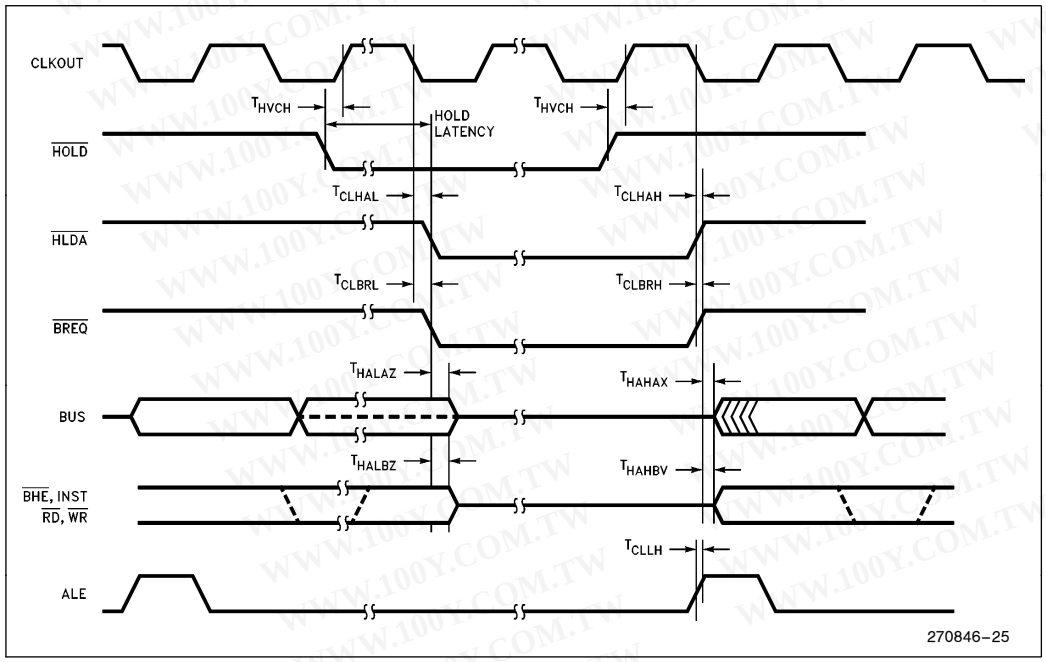
HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	15	ns	
T_{AZHAL}	HLDA Low to Address Float		15	ns	
T_{BZHAL}	HLDA Low to BHE, INST, RD, WR Weakly Driven		15	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−10		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

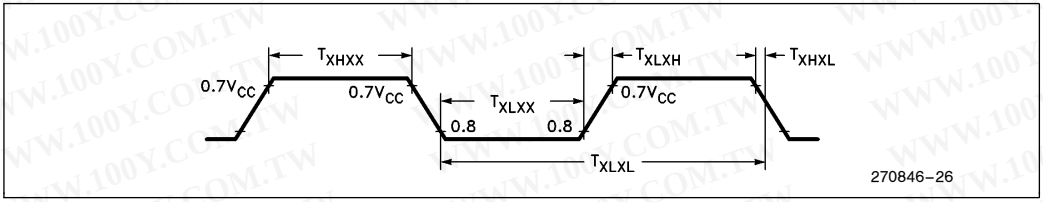
	Min	Max	Units
Weak Pullups on ADV, RD, WR, WRL, BHE	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4



EXTERNAL CLOCK DRIVE

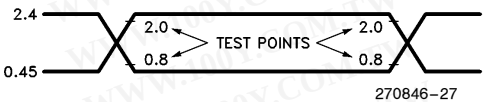
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4.0	16.0	MHz
T_{XLXL}	Oscillator Frequency	62.5	250	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications, the capacitance will not exceed 20 pF.

AC TESTING INPUT, OUTPUT WAVEFORMS



AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS

For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

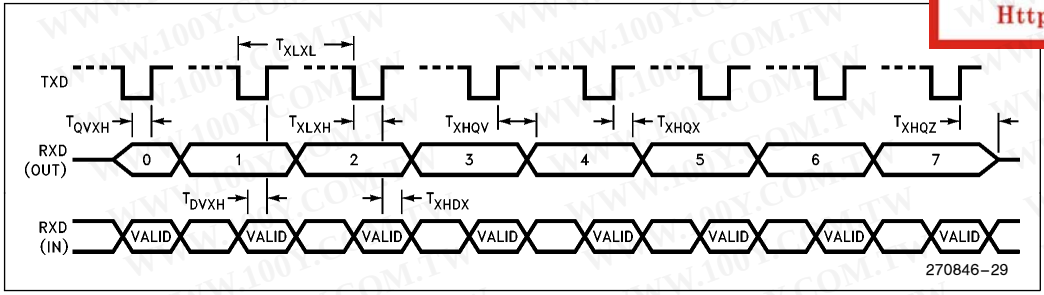
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

EPROM SPECIFICATIONS

AC EPROM Programming Characteristics

Operating Conditions: Load Capacitance = 150 pF, T_A = +25°C ±5°C, V_{CC}, V_{REF} = 5V, V_{SS}, ANGND = 0V, V_{PP} = 12.50V ±0.25V, EA = 12.50V ±0.25V

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(2)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run Time Programming is done with F_{OSC} = 6.0 MHz to 12.0 MHz, V_{REF} = 5V ±0.50V. T_A = +25°C to ±5°C and V_{PP} = 12.50V. For run-time programming over a full operating range, contact the factory.
2. This specification is for the Word Dump Mode. For programming pulses, use 300 T_{OSC} + 100 µs.

DC EPROM Programming Characteristics

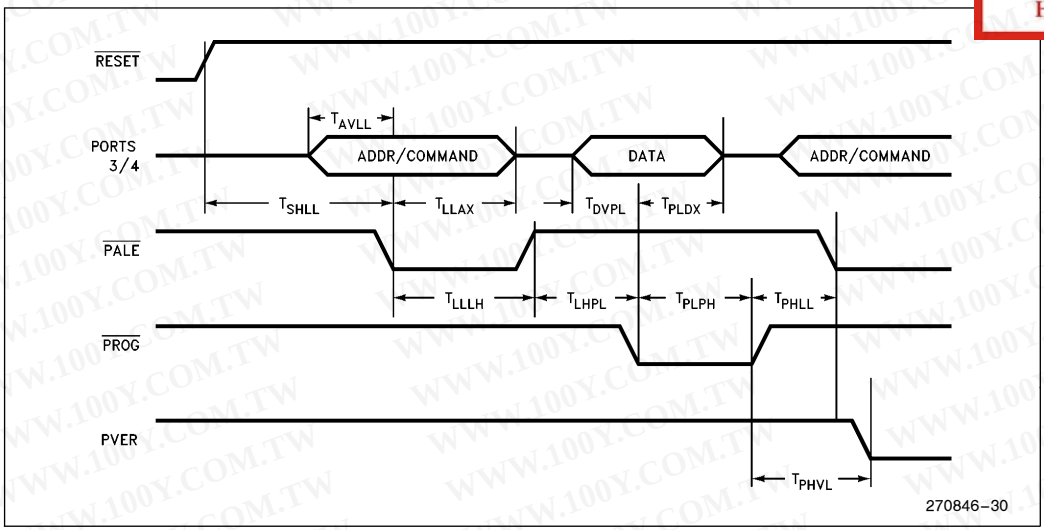
Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
V_{PP} must be within 1V of V_{CC} while V_{CC} < 4.5V. V_{PP} must not have a low impedance path to ground of V_{SS} while V_{CC} > 4.5V.

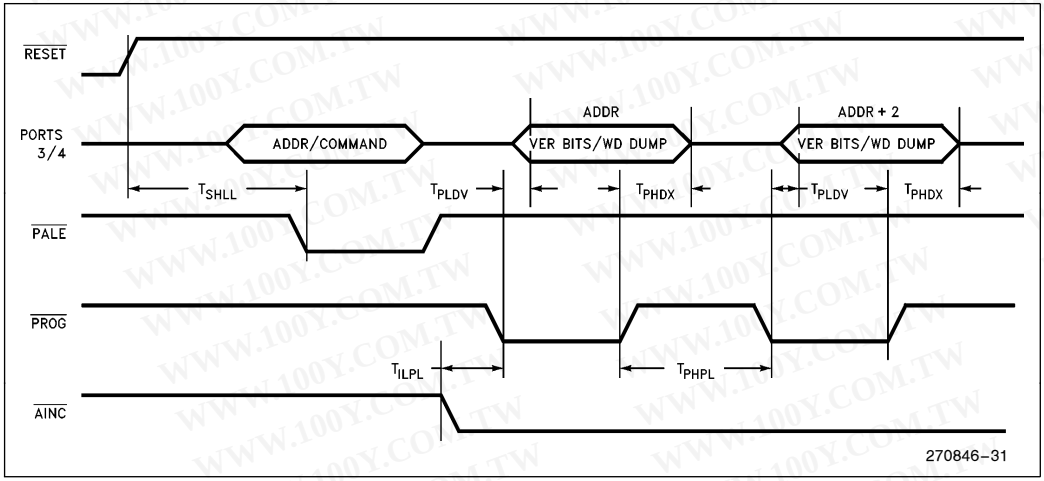
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE

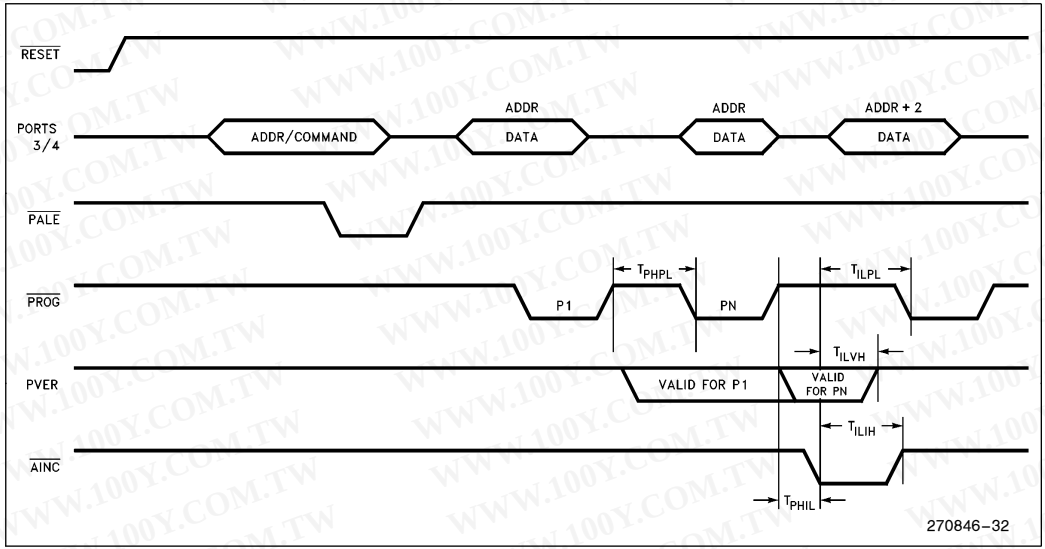


SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



10-BIT A/D CHARACTERISTICS

The speed of the A/D converter in the 10-bit mode can be adjusted by setting a clock prescaler on or off. At high frequencies more time is needed for the comparator to settle. The maximum frequency with the clock prescaler disabled is 6 MHz. The conversion times with the prescaler turned on or off is shown in the table below. The AD__TIME register has not been characterized for the 10-bit mode.

The converter is ratiometric, so the absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

Clock Prescaler On IOC2.4 = 0	Clock Prescaler Off IOC2.4 = 1
156.5 States 19.5 μs @ 16 MHz	89.5 States 29.8 μs @ 6 MHz

A/D CONVERTER SPECIFICATIONS

The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Parameter	Typical (3)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	±3			LSBs	
Zero Offset Error	±3			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 2
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Resistance		750	1.2K	Ω	
DC Input Leakage		0	3.0	μA	
Sample Time: Prescaler On Prescaler Off	16 8			States States	
Input Capacitance	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. DC to 100 KHz.
2. Multiplexer Break-Before-Make Guaranteed.
3. Typical values are expected for most devices at 25°C.

8-BIT MODE A/D CHARACTERISTICS

The 8-bit mode trades off resolution for a faster conversion time. The AD__TIME register must be used when performing an 8-bit conversion.

Sample Time 20 States	Convert Time 56 States
A6H in AD__TIME 9.8 μs @ 16 MHz	

The following specifications are tested @ 16 MHz with OA6H in AD__TIME. The actual AD__TIME register is tested with all possible values, to ensure functionality, but the accuracy of the A/D converter is not.

Parameter	Typical	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±2	LSBs	
Full Scale Error	±1			LSBs	
Zero Offset Error	±2			LSBs	
Non-Linearity		0	±2	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

NOTES:
*An "LSB", as used here, has a value of approximately 20 mV.
1. Typical values are expected for most devices at 25°C.

8XC196KB TO 87C196KC DESIGN CONSIDERATIONS

1. Memory Map. The 87C196KC has 512 bytes of RAM/SFRs and 16K of ROM/EPROM. The extra 256 bytes of RAM will reside in locations 100H–1FFH and the extra 8K of EPROM will reside in locations 4000H–5FFFH. These locations are external memory on the 87C196KB.
2. The CDE pin on the KB has become a V_{SS} pin on the KC to support 16 MHz operation.
3. EPROM programming. The 87C196KC has a different programming algorithm to support 16K of on-board memory. When performing Run-Time Programming, use the section of code on page 99 of the 80C196KC User's Guide, Order Number 270704.
4. ONCE Mode Entry. The ONCE mode is entered on the 87C196KC by driving the TXD pin low on the rising edge of RESET. The TXD pin is held high by a pullup that is specified at 1.4 mA and remain at 2.0V. This Pullup must not be overridden or the 87C196KC will enter the ONCE mode.
5. During the bus HOLD state, the 87C196KC weakly holds RD, WR, ALE, BHE and INST in their inactive states. The 87C196KB only holds ALE in its inactive state.
6. A RESET pulse from the 87C196KC is 16 states rather than 4 states as on the 87C196KB (i.e., a watchdog timer overflow). This provides a longer RESET pulse for other devices in the system.

87C196KC B-3 STEP ERRATA

1. NMI during PTS skips an address: When an NMI interrupts a PTS routine, the first byte of the instruction following completion of the PTS cycle is lost. This results in incorrect code execution. Workaround: NMI must be disabled using external hardware during any PTS activity.
2. QBD port glitch. There is a strong negative glitch on all QBD Port pins (P1.x and P2.6, P2.7) synchronous with the first falling edge of CLKOUT. This glitch lasts about 10 ns, and only occurs one time following the initial application of V_{CC}. The time for the pin to return to V_{CC} may be several microseconds, depending on pin loading capacitance. Workaround: External systems and devices should be disabled from responding to this glitch until after the first CLKOUT falling edge has occurred.
3. Divide error during HOLD or READY. The result of a signed divide instruction may be off by one if executed while the device is held off the bus by HOLD or READY and the queue is empty. Specific timings of HOLD or READY going active or inactive must be met. Workaround for HOLD: disable HOLD during signed divide operations (using hardware or software). Workaround for READY: problem will only occur if unlimited wait state mode is selected, and 14 or more wait states are inserted.
4. The HSI unit has two errata: one dealing with resolution and the other with first entries into the FIFO.

   The HSI resolution is 9 states instead of 8 states. Events on the same line may be lost if they occur faster than once every 9 state times.

   There is a mismatch between the 9 state time HSI resolution and the 8 state time timer. This causes one time value to be unused every 9 timer counts.

   Events may receive a time-tag on one count later than expected because of this ‘‘skipped’’ time value.

   If the first two events into an empty FIFO (not including the Holding Register) occur in the same internal phase, both are recorded with one time-tag. Otherwise, if the second event occurs within 9 states after the first, its time-tag is one count later than the first time tag. If this is the ‘‘skipped’’ time value, the second event’s time-tag is 2 counts later than the first’s.

   If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register after 8 state times, leaving the FIFO empty again. If the second event occurs after this time, it will act as a new first event into an empty FIFO.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

DATASHEET REVISION HISTORY

The following are the key differences between this datasheet and the -003 version:

1. The ‘‘advanced information’’ status was dropped and replaced with production status (no label).
2. Trademarks were updated.