



勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

160 MHz Rail-to-Rail Amplifier with Disable

AD8041

FEATURES

Fully Specified for +3 V, +5 V, and ± 5 V Supplies
Output Swings Rail to Rail
Input Voltage Range Extends 200 mV Below Ground
No Phase Reversal with Inputs 1 V Beyond Supplies
Disable/Power-Down Capability
Low Power of 5.2 mA (26 mW on +5 V)
High Speed and Fast Settling on +5 V:
160 MHz -3 dB Bandwidth ($G = +1$)
160 V/ μ s Slew Rate
30 ns Settling Time to 0.1%
Good Video Specifications ($R_L = 150 \Omega$, $G = +2$)
Gain Flatness of 0.1 dB to 30 MHz
0.03% Differential Gain Error
0.03° Differential Phase Error
Low Distortion
-69 dBc Worst Harmonic @ 10 MHz
Outstanding Load Drive Capability
Drives 50 mA 0.5 V from Supply Rails
Cap Load Drive of 45 pF

APPLICATIONS

Power Sensitive High Speed Systems
Video Switchers
Distribution Amplifiers
A/D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)
Single-Supply Multiplexer

PRODUCT DESCRIPTION

The AD8041 is a low power voltage feedback, high speed amplifier designed to operate on +3 V, +5 V or ± 5 V supplies. It has true single supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

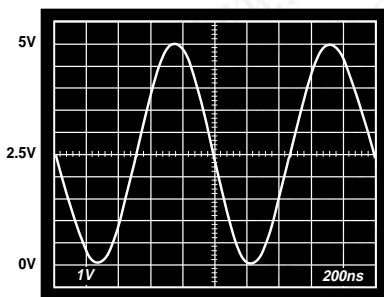
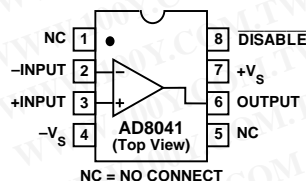


Figure 1. Output Swing: Gain = -1 , $V_S = +5$ V

CONNECTION DIAGRAM 8-Pin Plastic Mini-DIP and SOIC



The output voltage swing extends to within 50 mV of each rail, providing the maximum output dynamic range. Additionally, it features gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase error of 0.03% and 0.03° on a single +5 V supply. This makes the AD8041 ideal for professional video electronics such as cameras, video switchers or any high speed portable equipment. The AD8041's low distortion and fast settling make it ideal for buffering high speed A-to-D converters.

The AD8041 has a high speed disable feature useful for multiplexing or for reducing power consumption (1.5 mA). The disable logic interface is compatible with CMOS or open-collector logic. The AD8041 offers low power supply current of 5.8 mA max and can run on a single +3 V power supply. These features are ideally suited for portable and battery powered applications where size and power are critical.

The wide bandwidth of 160 MHz along with 160 V/ μ s of slew rate on a single +5 V supply make the AD8041 useful in many general purpose high speed applications where dual power supplies of up to ± 6 V and single supplies from +3 V to +12 V are needed. The AD8041 is available in 8-pin plastic DIP and SOIC over the industrial temperature range of -40°C to $+85^\circ\text{C}$.

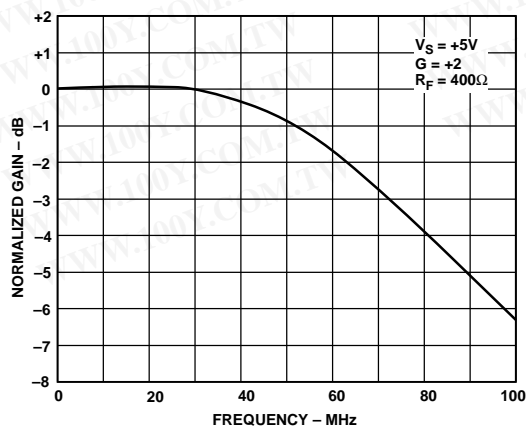


Figure 2. Frequency Response: Gain = $+2$, $V_S = +5$ V

REV. 0

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AD8041—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $R_L = 2\text{ k}\Omega$ to 2.5 V , unless otherwise noted)

| Parameter | Conditions | Min | AD8041A Typ | Max | Units |
|--|---|--------------|-----------------|-----|------------------------------|
| DYNAMIC PERFORMANCE | | | | | |
| –3 dB Small Signal Bandwidth, $V_O < 0.5\text{ V p-p}$ | $G = +1$ | 130 | 160 | | MHz |
| Bandwidth for 0.1 dB Flatness | $G = +2$, $R_L = 150\ \Omega$ | | 30 | | MHz |
| Slew Rate | $G = -1$, $V_O = 2\text{ V Step}$ | 130 | 160 | | V/ μs |
| Full Power Response | $V_O = 2\text{ V p-p}$ | | 24 | | MHz |
| Settling Time to 0.1% | $G = -1$, $V_O = 2\text{ V Step}$ | | 35 | | ns |
| Settling Time to 0.01% | | | 55 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Total Harmonic Distortion | $f_C = 5\text{ MHz}$, $V_O = 2\text{ V p-p}$, $G = +2$, $R_L = 1\text{ k}\Omega$ | | –72 | | dB |
| Input Voltage Noise | $f = 10\text{ kHz}$ | | 16 | | nV/ $\sqrt{\text{Hz}}$ |
| Input Current Noise | $f = 10\text{ kHz}$ | | 600 | | fA/ $\sqrt{\text{Hz}}$ |
| Differential Gain Error (NTSC) | $G = +2$, $R_L = 150\ \Omega$ to 2.5 V | | 0.03 | | % |
| Differential Phase Error (NTSC) | $G = +2$, $R_L = 150\ \Omega$ to 2.5 V | | 0.03 | | Degrees |
| | $G = +2$, $R_L = 75\ \Omega$ to 2.5 V | | 0.01 | | % |
| | $G = +2$, $R_L = 75\ \Omega$ to 2.5 V | | 0.19 | | Degrees |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | $T_{\text{MIN}}-T_{\text{MAX}}$ | | 2 | 7 | mV |
| Offset Drift | | | 10 | 8 | mV |
| Input Bias Current | $T_{\text{MIN}}-T_{\text{MAX}}$ | | 1.2 | 2 | $\mu\text{V}/^\circ\text{C}$ |
| | | | | 3 | μA |
| Input Offset Current | | | 0.2 | 0.5 | μA |
| Open-Loop Gain | $R_L = 1\text{ k}\Omega$ | 86 | 95 | | dB |
| | $T_{\text{MIN}}-T_{\text{MAX}}$ | | 90 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 160 | | k Ω |
| Input Capacitance | | | 1.8 | | pF |
| Input Common-Mode Voltage Range | | | –0.2 to 4 | | V |
| Common-Mode Rejection Ratio | $V_{\text{CM}} = 0\text{ V}$ to 3.5 V | 74 | 80 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing: $R_L = 10\text{ k}\Omega$ | | | 0.05 to 4.95 | | V |
| $R_L = 1\text{ k}\Omega$ | | 0.35 to 4.75 | 0.1 to 4.9 | | V |
| $R_L = 50\ \Omega$ | | 0.4 to 4.4 | 0.3 to 4.5 | | V |
| Output Current | $V_{\text{OUT}} = 0.5\text{ V}$ to 4.5 V | | 50 | | mA |
| Short Circuit Current | Sourcing | | 90 | | mA |
| | Sinking | | 150 | | mA |
| Capacitive Load Drive | $G = +1$ | | 45 | | pF |
| POWER SUPPLY | | | | | |
| Operating Range | | 3 | | 12 | V |
| Quiescent Current | | | 5.2 | 5.8 | mA |
| Quiescent Current (Disabled) | | | 1.4 | 1.7 | mA |
| Power Supply Rejection Ratio | $V_S = 0, +5\text{ V}, \pm 1\text{ V}$ | 72 | 80 | | dB |
| DISABLE CHARACTERISTICS | | | | | |
| Turn-Off Time | $V_O = 2\text{ V p-p}$ @ 10 MHz , $G = +2$ | | 120 | | ns |
| Turn-On Time | $R_F = R_L = 2\text{ k}\Omega$ | | 230 | | ns |
| Off Isolation (Pin 8 Tied to $-V_S$) | $R_F = R_L = 2\text{ k}\Omega$ | | 70 | | dB |
| Off Voltage (Device Disabled) | $R_L = 100\ \Omega$, $f = 5\text{ MHz}$, $G = +2$, $R_F = 1\text{ k}\Omega$ | | $< +V_S - 0.25$ | | V |
| On Voltage (Device Enabled) | | | Open or $+V_S$ | | V |

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SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$, $V_S = +3\text{ V}$, $R_L = 2\text{ k}\Omega$ to 1.5 V , unless otherwise noted)

| Parameter | Conditions | AD8041A | | | Units |
|--|--|-------------|-------------------------|-----|---------|
| | | Min | Typ | Max | |
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth, V _O < 0.5 V p-p | G = +1 | 120 | 150 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = +2, R _L = 150 Ω | | 25 | | MHz |
| Slew Rate | G = −1, V _O = 2 V Step | 120 | 150 | | V/μs |
| Full Power Response | V _O = 2 V p-p | | 20 | | MHz |
| Settling Time to 0.1% | G = −1, V _O = 2 V Step | | 40 | | ns |
| Settling Time to 0.01% | | | 55 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Total Harmonic Distortion | f _C = 5 MHz, V _O = 2 V p-p, G = −1, R _L = 100 Ω | | −55 | | dB |
| Input Voltage Noise | f = 10 kHz | | 16 | | nV/√Hz |
| Input Current Noise | f = 10 kHz | | 600 | | fA/√Hz |
| Differential Gain Error (NTSC) | G = +2, R _L = 150 Ω to 1.5 V, Input V _{CM} = 1 V | | 0.07 | | % |
| Differential Phase Error (NTSC) | G = +2, R _L = 150 Ω to 1.5 V, Input V _{CM} = 1 V | | 0.05 | | Degrees |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | T _{MIN} –T _{MAX} | | 2 | 7 | mV |
| Offset Drift | | | 10 | 8 | mV |
| Input Bias Current | T _{MIN} –T _{MAX} | | 1.2 | 2.3 | μV/°C |
| Input Offset Current | | | | 3 | μA |
| Open-Loop Gain | R _L = 1 kΩ | 85 | 94 | 0.6 | μA |
| | T _{MIN} –T _{MAX} | | | 89 | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | V _{CM} = 0 V to 1.5 V | | 160 | | kΩ |
| Input Capacitance | | | 1.8 | | pF |
| Input Common-Mode Voltage Range | | | −0.2 to 2 | | V |
| Common-Mode Rejection Ratio | | | 72 | 80 | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing: R _L = 10 kΩ | V _{OUT} = 0.5 V to 2.5 V | | 0.05 to 2.95 | | V |
| R _L = 1 kΩ | | 0.45 to 2.7 | 0.1 to 2.9 | | V |
| R _L = 50 Ω | | 0.5 to 2.6 | 0.25 to 2.75 | | V |
| Output Current | | | 50 | | mA |
| Short Circuit Current | | Sourcing | 70 | | mA |
| | | Sinking | 120 | | mA |
| Capacitive Load Drive | G = +1 | | 40 | | pF |
| POWER SUPPLY | | | | | |
| Operating Range | V _S = 0, +3 V, ±0.5 V | 3 | | 12 | V |
| Quiescent Current | | | 5.0 | 5.6 | mA |
| Quiescent Current (Disabled) | | | 1.3 | 1.5 | mA |
| Power Supply Rejection Ratio | | 68 | 80 | | dB |
| DISABLE CHARACTERISTICS | | | | | |
| Turn-Off Time | V _O = 2 V p-p @ 10 MHz, G = +2 | | 90 | | ns |
| Turn-On Time | R _F = R _L = 2 kΩ | | 170 | | ns |
| Off Isolation (Pin 8 Tied to −V _S) | R _F = R _L = 2 kΩ | | 70 | | dB |
| Off Voltage (Device Disabled) | R _L = 100 Ω, f = 5 MHz, G = +2, R _F = 1 kΩ | | <+V _S − 0.25 | | V |
| On Voltage (Device Enabled) | | | Open or +V _S | | V |

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AD8041—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{ V}$, $R_L = 2\text{ k}\Omega$ to 0 V , unless otherwise noted)

| Parameter | Conditions | AD8041A | | | Units |
|--|---|---------------|---------------------------|-----|---------|
| | | Min | Typ | Max | |
| DYNAMIC PERFORMANCE | | | | | |
| –3 dB Small Signal Bandwidth, V _O < 0.5 V p-p | G = +1 | 140 | 170 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = +2, R _L = 150 Ω | | 32 | | MHz |
| Slew Rate | G = –1, V _O = 2 V Step | 140 | 170 | | V/μs |
| Full Power Response | V _O = 2 V p-p | | 26 | | MHz |
| Settling Time to 0.1% | G = –1, V _O = 2 V Step | | 30 | | ns |
| Settling Time to 0.01% | | | 50 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Total Harmonic Distortion | f _C = 5 MHz, V _O = 2 V p-p, G = +2, R _L = 1 kΩ | | –77 | | dB |
| Input Voltage Noise | f = 10 kHz | | 16 | | nV/√Hz |
| Input Current Noise | f = 10 kHz | | 600 | | fA/√Hz |
| Differential Gain Error (NTSC) | G = +2, R _L = 150 Ω | | 0.02 | | % |
| Differential Phase Error (NTSC) | G = +2, R _L = 150 Ω | | 0.03 | | Degrees |
| | G = +2, R _L = 75 Ω | | 0.02 | | % |
| | G = +2, R _L = 75 Ω | | 0.10 | | Degrees |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | T _{MIN} –T _{MAX} | | 2 | 7 | mV |
| Offset Drift | | | 10 | 8 | μV/°C |
| Input Bias Current | T _{MIN} –T _{MAX} | | 1.2 | 2.3 | μA |
| Input Offset Current | | | 0.2 | 3 | μA |
| Open-Loop Gain | R _L = 1 kΩ | 90 | 99 | 0.6 | dB |
| | T _{MIN} –T _{MAX} | | 95 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 160 | | kΩ |
| Input Capacitance | | | 1.8 | | pF |
| Input Common-Mode Voltage Range | | | –5.2 to 4 | | V |
| Common-Mode Rejection Ratio | V _{CM} = –5 V to 3.5 V | 72 | 80 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing: R _L = 10 kΩ | | | –4.95 to +4.95 | | V |
| R _L = 1 kΩ | | –4.45 to +4.6 | –4.8 to +4.8 | | V |
| R _L = 50 Ω | | –4.3 to +3.2 | –4.5 to +3.8 | | V |
| Output Current | V _{OUT} = –4.5 V to 4.5 V | | 50 | | mA |
| Short Circuit Current | Sourcing | | 100 | | mA |
| | Sinking | | 160 | | mA |
| Capacitive Load Drive | G = +1 | | 50 | | pF |
| POWER SUPPLY | | | | | |
| Operating Range | | 3 | | 12 | V |
| Quiescent Current | | | 5.8 | 6.5 | mA |
| Quiescent Current (Disabled) | | | 1.6 | 2.2 | mA |
| Power Supply Rejection Ratio | V _S = –5, +5 V, ±1 V | 68 | 80 | | dB |
| DISABLE CHARACTERISTICS | | | | | |
| Turn-Off Time | V _O = 2 V p-p @ 10 MHz, G = +2 | | 120 | | ns |
| Turn-On Time | R _F = 2 kΩ | | 320 | | ns |
| Off Isolation (Pin 8 Tied to –V _S) | R _L = 100 Ω, f = 5 MHz, G = +2, R _F = 1 kΩ | | 70 | | dB |
| Off Voltage (Device Disabled) | | | <+V _S – 0.25 V | | |
| On Voltage (Device Enabled) | | | Open or +V _S | | |

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

| | |
|---|-------------------------------|
| Supply Voltage | +12.6 V |
| Internal Power Dissipation ² | |
| Plastic Package (N) | 1.3 Watts |
| Small Outline Package (R) | 0.9 Watts |
| Input Voltage (Common Mode) | $\pm V_S$ |
| Differential Input Voltage | ± 3.4 V |
| Output Short Circuit Duration | Observe Power Derating Curves |
| Storage Temperature Range N, R | -65°C to +125°C |
| Operating Temperature Range (A Grade) ... | -40°C to +85°C |
| Lead Temperature Range (Soldering 10 sec) | +300°C |

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Specification is for the device in free air:

8-Pin Plastic Package: $\theta_{JA} = 90^\circ\text{C/Watt}$

8-Pin SOIC Package: $\theta_{JA} = 160^\circ\text{C/Watt}$

ORDERING GUIDE

| Model | Temperature Range | Package Option |
|---------------|-------------------|--------------------|
| AD8041AN | -40°C to +85°C | 8-Pin Plastic DIP |
| AD8041AR | -40°C to +85°C | 8-Pin Plastic SOIC |
| AD8041AR-REEL | | REEL-SOIC |
| AD8041-EB | | Evaluation Board |

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8041 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8041 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

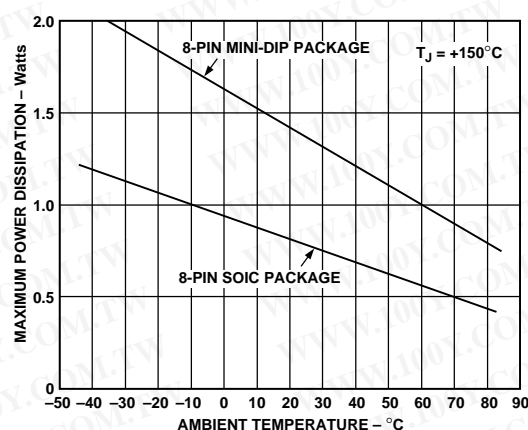


Figure 3. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8041 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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AD8041—Typical Performance Characteristics

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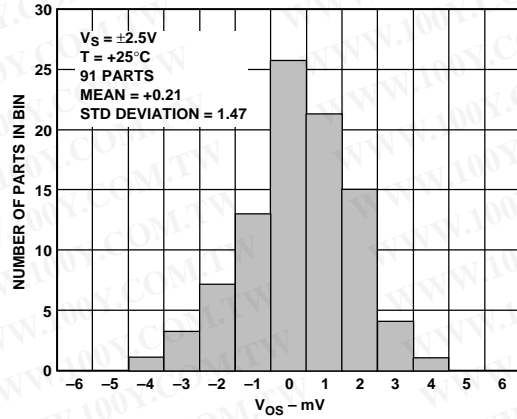


Figure 4. Typical Distribution of V_{OS}

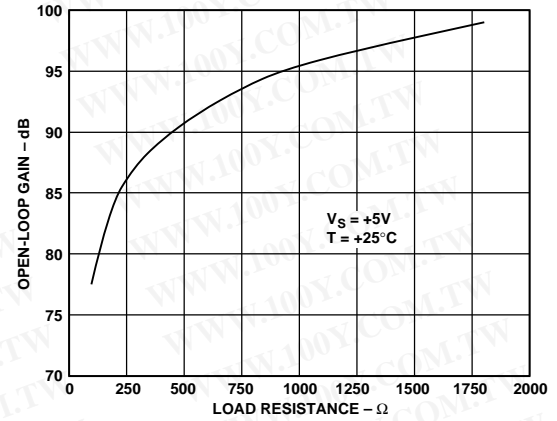


Figure 7. Open-Loop Gain vs. R_L to +25°C

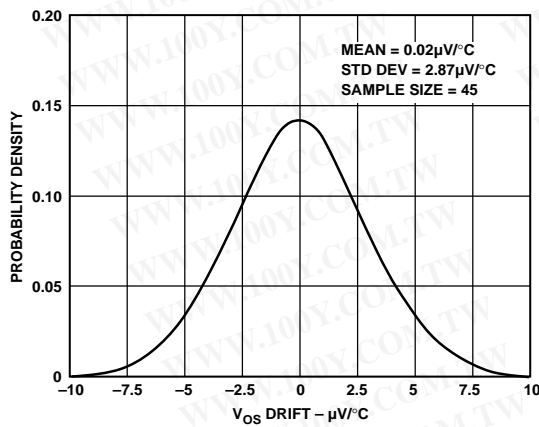


Figure 5. V_{OS} Drift Over -40°C to +85°C

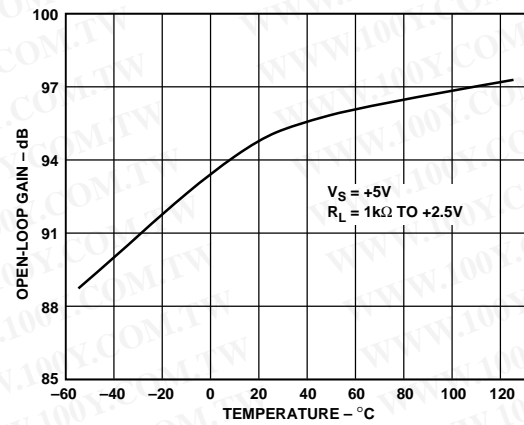


Figure 8. Open-Loop Gain vs. Temperature

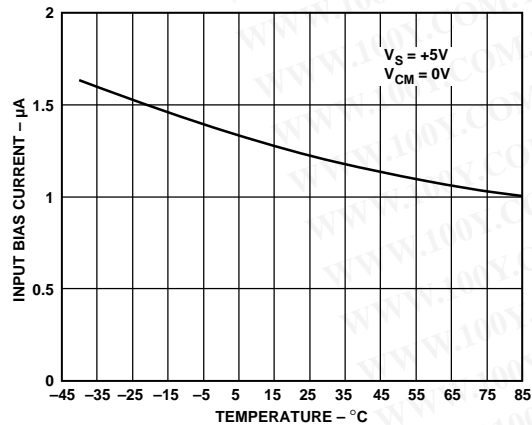


Figure 6. I_B vs. Temperature

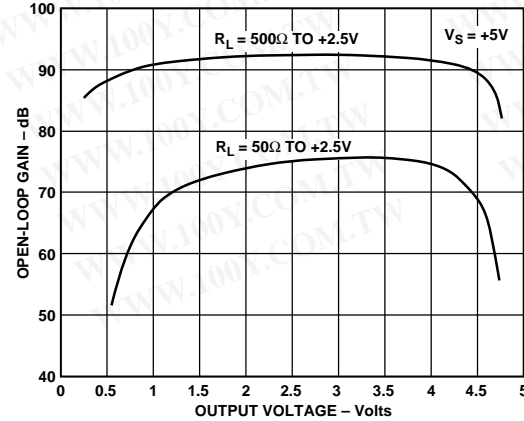


Figure 9. Open-Loop Gain vs. Output Voltage

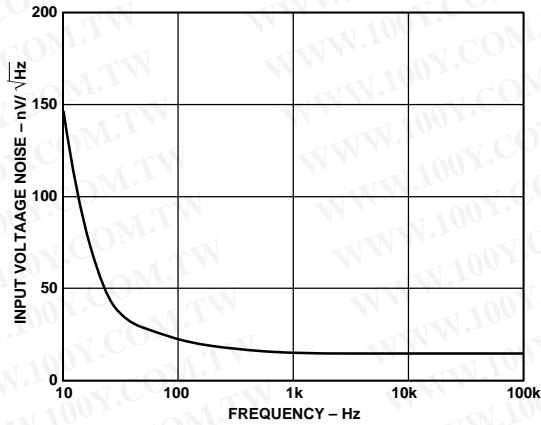


Figure 10. Input Voltage Noise vs. Frequency

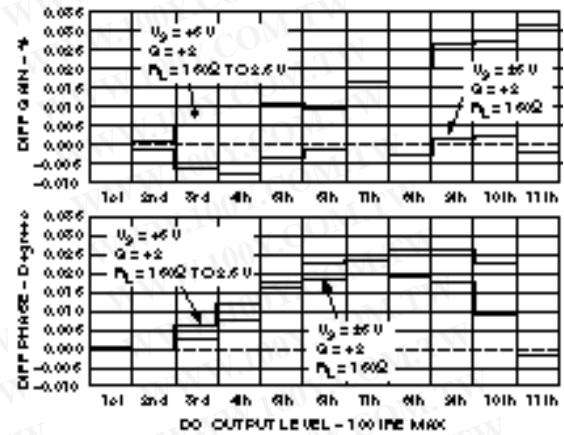


Figure 13. Differential Gain and Phase Errors

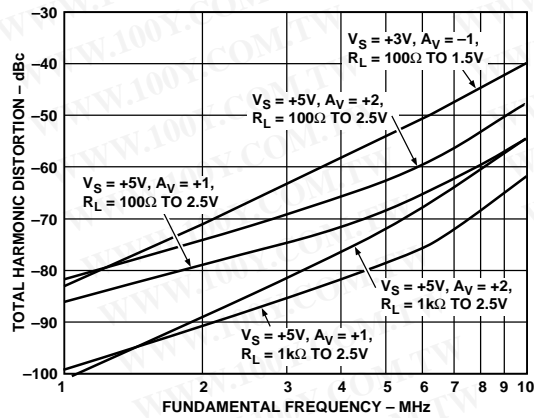


Figure 11. Total Harmonic Distortion

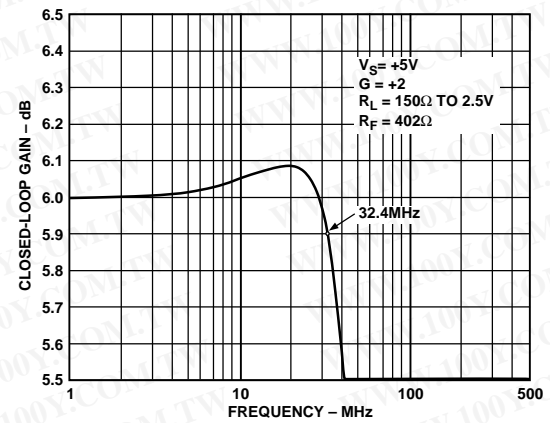


Figure 14. 0.1 dB Gain Flatness

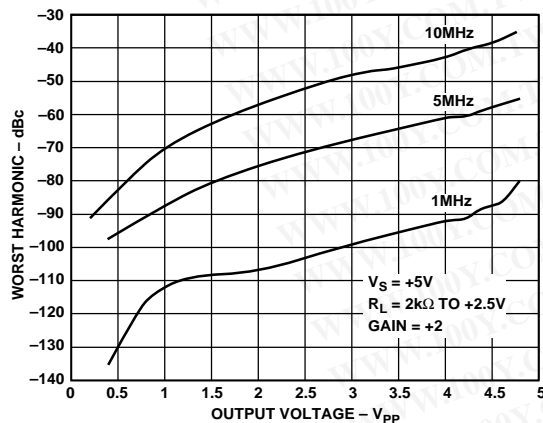


Figure 12. Worst Harmonic vs. Output Voltage

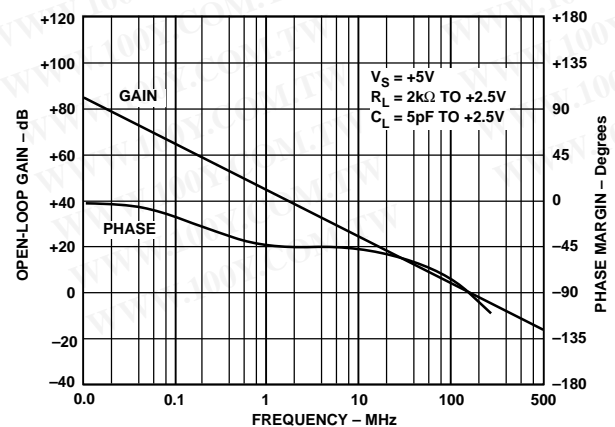


Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

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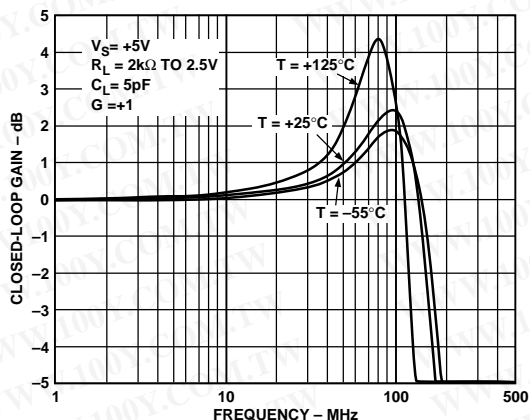


Figure 16. Closed-Loop Frequency Response vs. Temperature

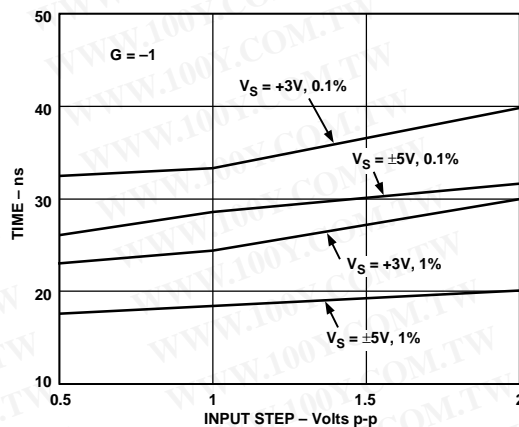


Figure 19. Settling Time vs. Input Step

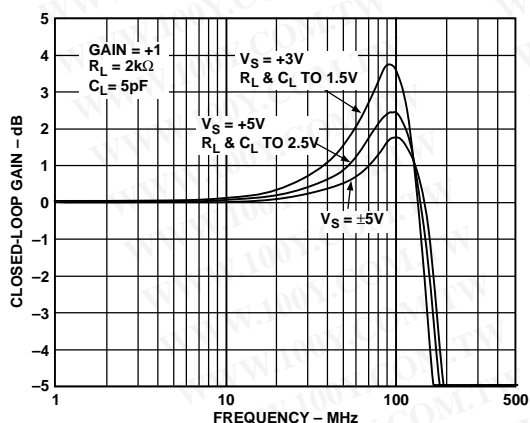


Figure 17. Closed-Loop Frequency Response vs. Supply

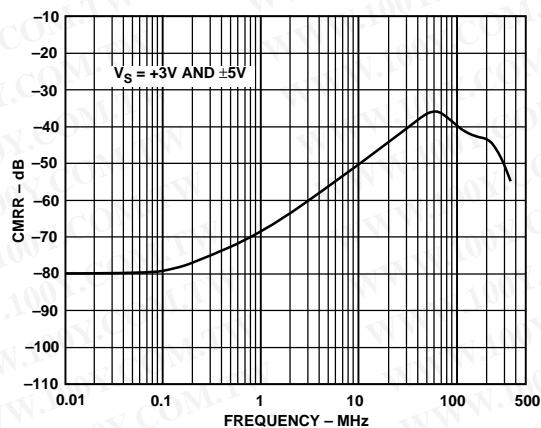


Figure 20. CMRR vs. Frequency

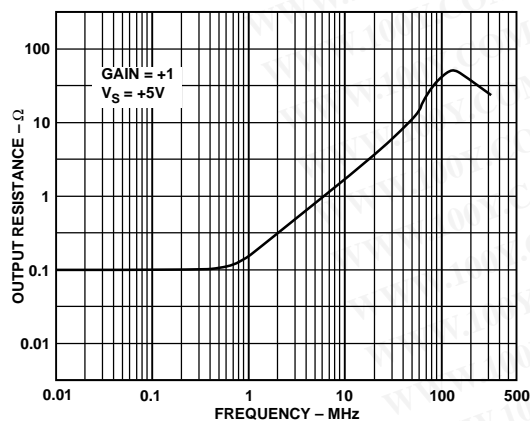


Figure 18. Output Resistance vs. Frequency

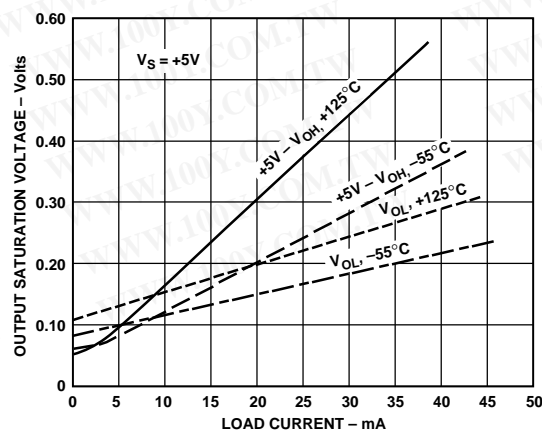


Figure 21. Output Saturation Voltage vs. Load Current

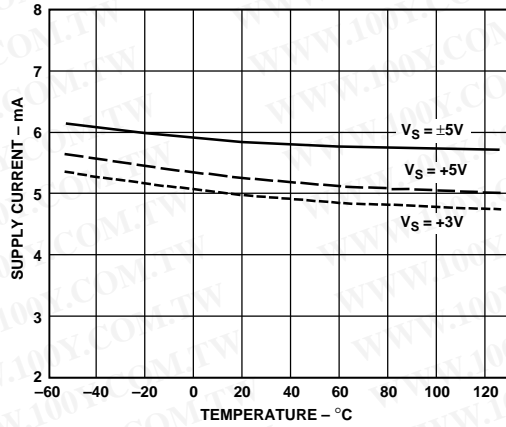


Figure 22. Supply Current vs. Temperature

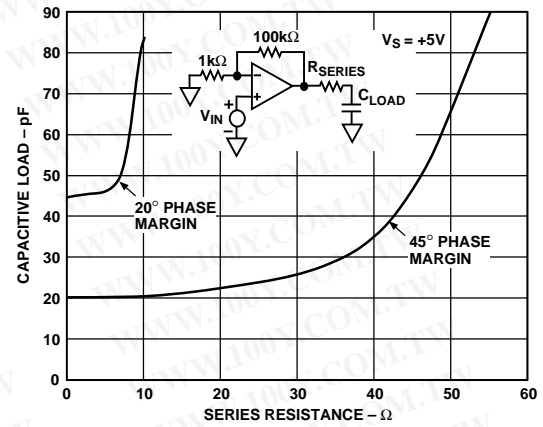


Figure 25. Capacitive Load vs. Series Resistance

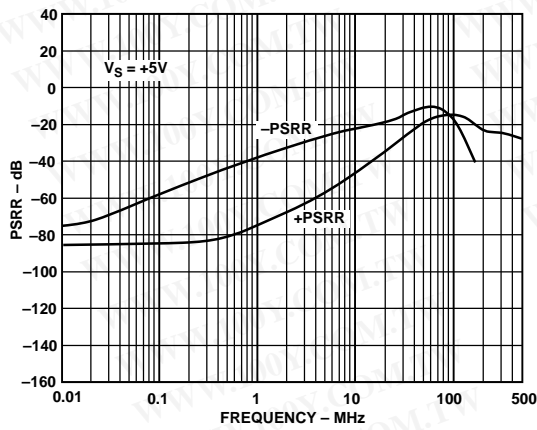


Figure 23. PSRR vs. Frequency

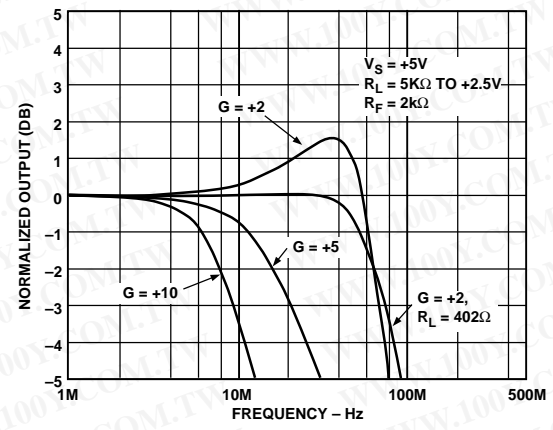


Figure 26. Frequency Response vs. Closed-Loop Gain

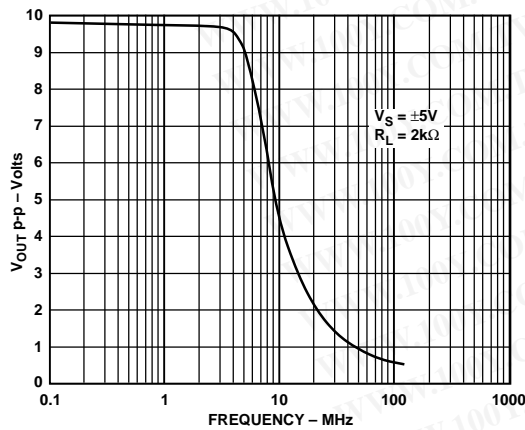


Figure 24. Output Voltage Swing vs. Frequency

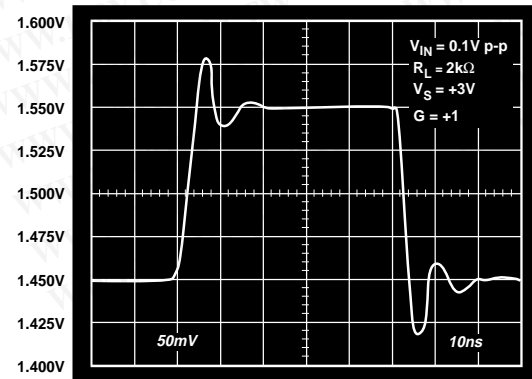


Figure 27. Pulse Response, $V_S = +3V$

AD8041—Typical Performance Characteristics

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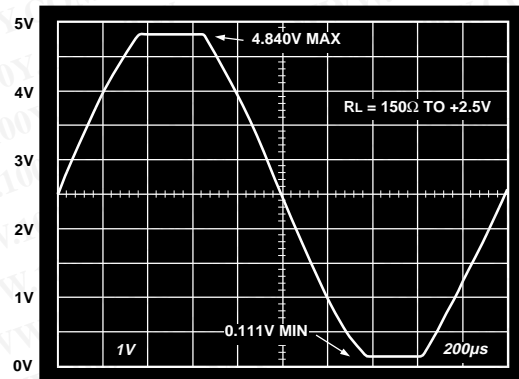


Figure 28a.

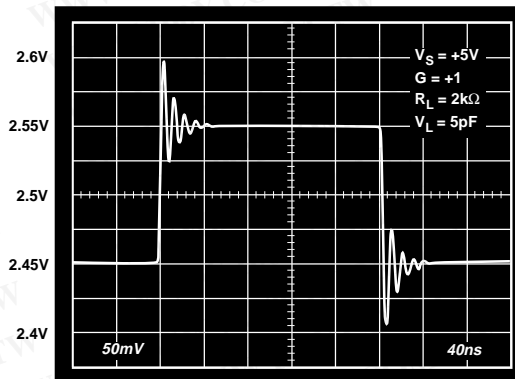


Figure 30. 100 mV Step Response, $V_S = +5V$, $G = +1$

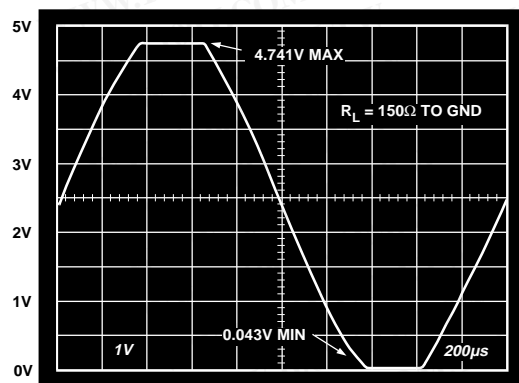


Figure 28b.

Figure 28a-b. Output Swing vs. Load Reference Voltage, $V_S = +5V$, $G = -1$

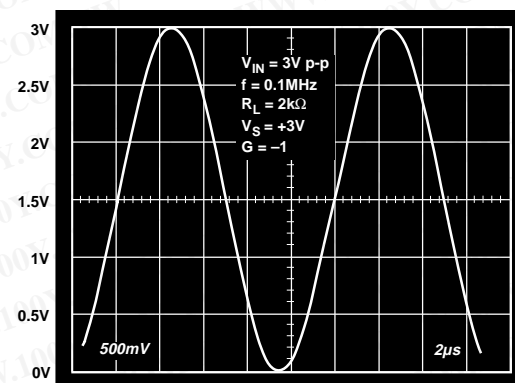


Figure 31. Output Swing, $V_S = +3V$, $V_{IN} = 3V$ p-p

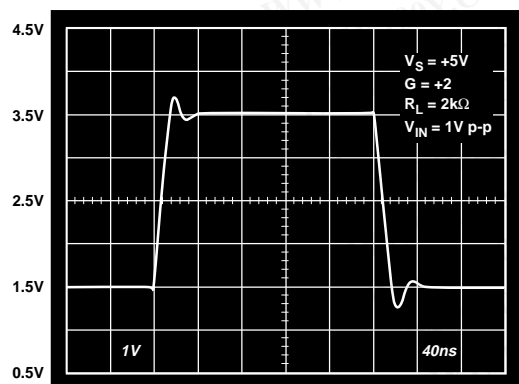


Figure 29. One Volt Step Response, $V_S = +5V$, $G = +2$

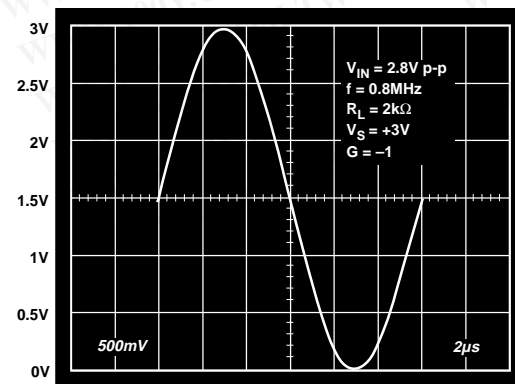


Figure 32. Output Swing, $V_S = +3V$, $V_{IN} = 2.8V$ p-p

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 33, the AD8041 recovers within 50 ns from negative overdrive and within 25 ns from positive overdrive.

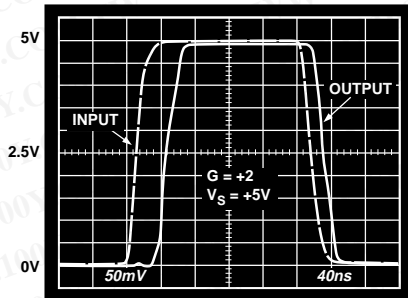


Figure 33. Overdrive Recovery

Circuit Description

The AD8041 is fabricated on Analog Devices' proprietary eXtra-Fast Complementary Bipolar (XFCB) process which enables the construction of PNP and NPN transistors with similar f_T s in the 2 GHz–4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features allow the construction of high frequency, low distortion amplifiers with low supply currents. This design uses a differential output input stage to maximize bandwidth and headroom (see Figure 34). The smaller signal swings required on the first stage outputs (nodes S1P, S1N) reduce the effect of nonlinear currents due to junction capacitances and improve the distortion performance. With this design harmonic distortion of better than –85 dB @ 1 MHz into 100 Ω with $V_{OUT} = 2$ V p-p (Gain = +2) on a single 5 volt supply is achieved.

The complementary common-emitter design of the output stage provides excellent load drive without the need for emitter followers, thereby improving the output range of the device considerably with respect to conventional op amps. High output drive capability is provided by injecting all output stage predriver currents directly into the bases of the output devices Q8 and Q36. Biasing of Q8 and Q36 is accomplished by I8 and I5, along with a common-mode feedback loop (not shown). This circuit topology allows the AD8041 to drive 50 mA of output current with the outputs within 0.5 V of the supply rails.

On the input side, the device can handle voltages from –0.2 V below the negative rail to within 1.2 V of the positive rail. Exceeding these values will not cause phase reversal; however, the input ESD devices will begin to conduct if the input voltages exceed the rails by greater than 0.5 V.

A “Nested Integrator” topology is used in the AD8041 (see small-signal schematic shown in Figure 35). The output stage can be modeled as an ideal op amp with a single-pole response and a unity-gain frequency set by transconductance g_{m2} and

capacitor C9. R1 is the output resistance of the input stage; g_m is the input transconductance. C7 and C9 provide Miller compensation for the overall op amp. The unity gain frequency will occur at $g_m/C9$. Solving the node equations for this circuit yields:

$$\frac{V_{OUT}}{V_i} = \frac{A0}{(sR1[C9(A2+1)]+1) \times \left(s \left[\frac{g_{m2}}{C3} \right] + 1 \right)}$$

where $A0 = g_m g_{m2} R2 R1$ (Open-Loop Gain of Op Amp)
 $A2 = g_{m2} R2$ (Open-Loop Gain of Output Stage)

The first pole in the denominator is the dominant pole of the amplifier, and occurs at about 180 Hz. This equals the input stage output impedance R1 multiplied by the Miller-multiplied value of C9. The second pole occurs at the unity-gain bandwidth of the output stage, which is 250 MHz. This type of architecture allows more open-loop gain and output drive to be obtained than a standard two-stage architecture would allow.

Output Impedance

The low frequency open-loop output impedance of the common emitter output stage used in this design is approximately 6.5 k Ω . While this is significantly higher than a typical emitter follower output stage, when connected with feedback the output impedance is reduced by the open-loop gain of the op amp. With 110 dB of open-loop gain the output impedance is reduced to less than 0.1 Ω . At higher frequencies the output impedance will rise as the open-loop gain of the op amp drops; however, the output also becomes capacitive due to the integrator capacitors C9 and C3. This prevents the output impedance from ever becoming excessively high (see Figure 18), which can cause stability problems when driving capacitive loads. In fact, the AD8041 has excellent cap-load drive capability for a high-frequency op amp. Figure 25 demonstrates that the AD8041 exhibits a 45° margin while driving a 20 pF direct capacitive load. In addition, running the part at higher gains will also improve the capacitive load drive capability of the op amp.

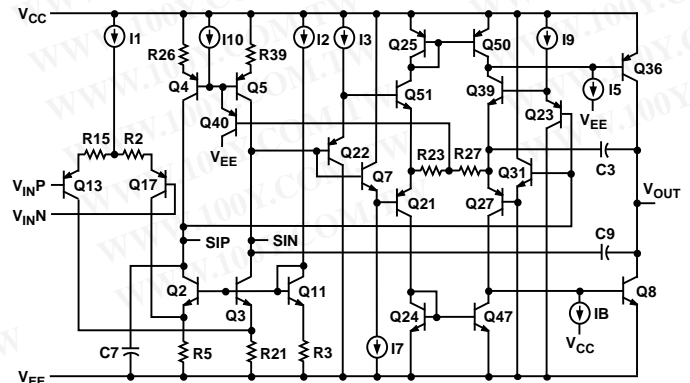


Figure 34. AD8041 Simplified Schematic

AD8041

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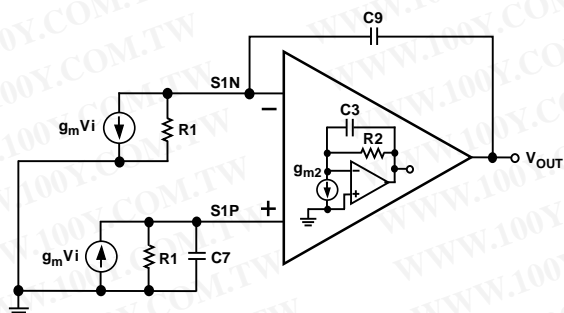


Figure 35. Small Signal Schematic

Disable Operation

The AD8041 has an active-low disable pin, which can be used to three-state the output of the part and also lower its supply current. If the disable pin is left floating, the part is enabled and will perform normally. If the disable pin is pulled to 2.5 V (min) below the positive supply, output of the AD8041 will be disabled and the nominal supply current will drop to less than 1.6 mA. For best isolation, the disable pin should be pulled to as low a voltage as possible; ideally, the negative supply rail.

The disable pin on the AD8041 allows it to be configured as an 2:1 mux as shown in Figure 36 and can be used to switch many types of high speed signals. Higher order multiplexers can also be built. The break-before-make switching time is approximately 50 ns to disable the output and 300 ns to enable the output.

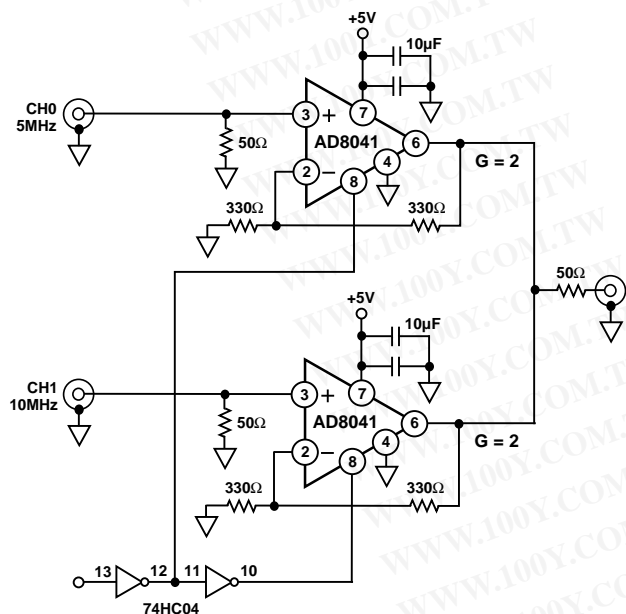


Figure 36. 2:1 Multiplexer

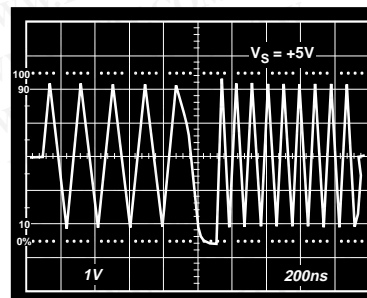


Figure 37. 2:1 Multiplexer Performance

Single Supply A/D Conversion

Figure 38 shows the AD8041 driving the analog inputs of the AD9050 in a dc coupled system with single ended signals. All components are powered from a single +5 V supply. The AD820 is used to offset the ground referenced input signal to the level required by the AD9050. The AD8041 is used to add in the offset with the ground referenced input signal and buffer the input to AD9050. The nominal input range of the AD9050

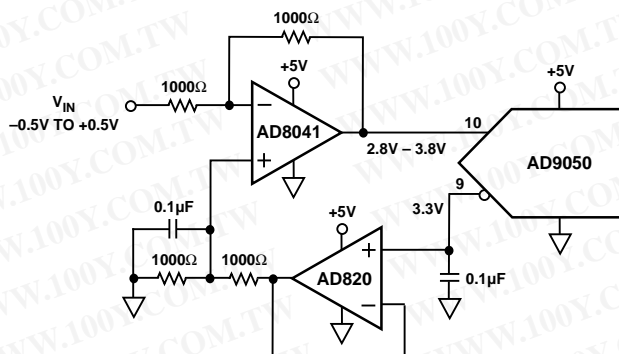


Figure 38. 10-Bit, 40 MSPS A/D Conversion

is +2.8 V and +3.8 V (1 V p-p centered at +3.3 V). This circuit provides 40 MSPS analog-to-digital conversion on just 330 mW of power while delivering 10-bit performance.

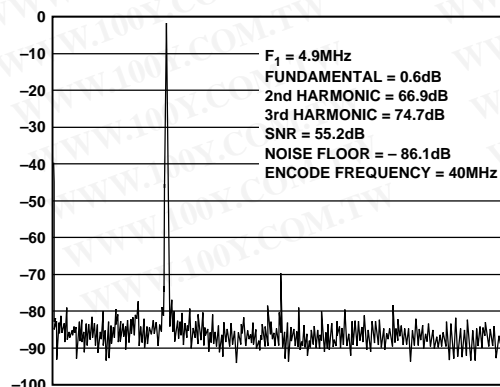


Figure 39. FFT Output of Circuit in Figure 38

APPLICATIONS

RGB Buffer

The AD8041 can provide buffering of RGB signals that include ground while operating from a single +3 V or +5 V supply.

The signals that drive an RGB monitor are usually supplied by current output DACs that operate from a +5 V only supply. These can triple DACs like the ADV7120 and ADV7122 from Analog Devices or integrated into the graphics controller IC as in most PCs these days.

During the horizontal blanking interval the currents output from the DACs go to zero and the RGB signals are pulled to ground via the termination resistors. If more than one RGB monitor is desired, it cannot simply be connected in parallel because it will provide an additional termination. Therefore, buffering must be provided before connecting a second monitor.

Since the RGB signals include ground as part of their dynamic output range, it has previously been required to use a dual supply op amp to provide this buffering. In some systems this is the only component that requires a negative supply so it can be quite inconvenient to incorporate this multiple monitor feature.

Figure 40 shows a schematic of one channel of a single supply gain-of-two buffer for driving a second RGB monitor. No current is required when the amplifier output is at ground. The termination resistor at the monitor helps pull the output down at low voltage levels.

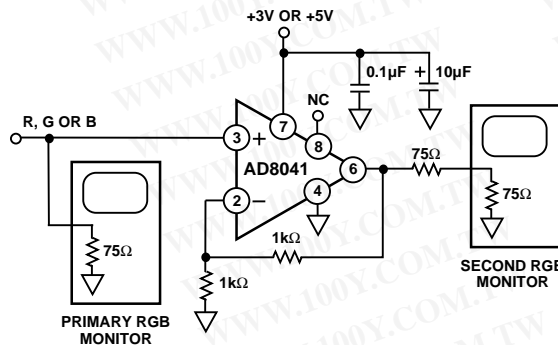


Figure 40. Single Supply RGB Buffer

Figure 41 is an oscilloscope photo of the circuit in Figure 40 operating from a +3 V supply and driven by the Blue signal of a color bar pattern. Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700 mV peak. The output of the AD8041 is 1.4 V with the termination resistors providing a divide-by-two. The Red and Green signals can be buffered in the same manner with duplication of this circuit.

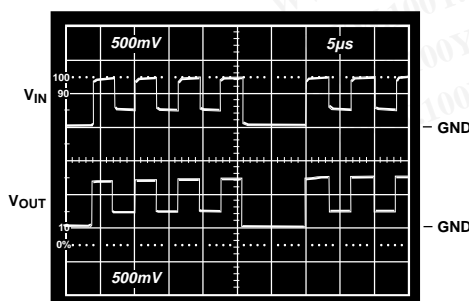


Figure 41. +3 V, RGB Buffer

Single Supply Composite Video Line Driver

Figure 42 shows a schematic of a single supply gain-of-two composite video line driver. Since the sync tips of a composite video signal extend below ground, the input must be ac coupled and shifted positively to provide signal swing during these negative excursions in a single supply configuration.

The input is terminated in 75 Ω and ac coupled via C_{IN} to a voltage divider that provides the dc bias point to the input. Setting the optimal bias point requires some understanding of the nature of composite video signals and the video performance of the AD8041.

Signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capability than their peak-to-peak amplitude after ac coupling. As a worst case, the dynamic signal swing required will approach twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high at a fraction of a percent duty cycle and vice versa.

Composite video is not quite this demanding. One bounding extreme is for a signal that is mostly black for an entire frame, but has a white (full intensity), minimum width spike at least once per frame.

The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal will have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for only about 75% of the time.

As a result of the duty cycle variations between the two extremes presented above, a 1 V p-p composite video signal that is multiplied by a gain of two requires about 3.2 V p-p of dynamic voltage swing at the output for an op amp to pass a composite video signal of arbitrary duty cycle without distortion.

Some circuits use a sync tip clamp along with ac coupling to hold the sync tips at a relatively constant level in order to lower the amount of dynamic signal swing required. However, these circuits can have artifacts like sync tip compression unless they are driven by sources with very low output impedance.

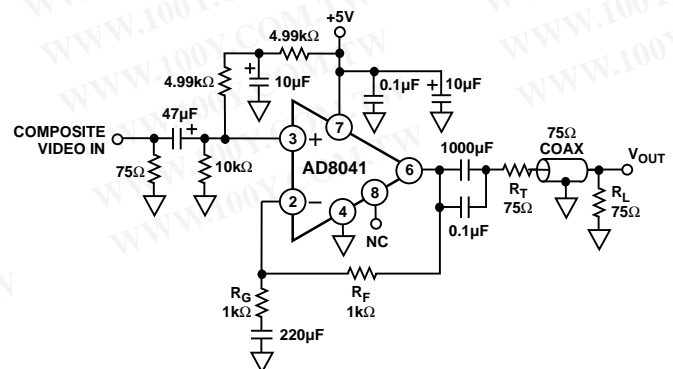


Figure 42. Single Supply Composite Video Line Driver

The AD8041 not only has ample signal swing capability to handle the dynamic range required without using a sync tip clamp, but also has good video specifications like differential gain and differential phase when buffering these signals in an ac coupled configuration.

AD8041

To test this, the differential gain and differential phase were measured for the AD8041 while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect to be observed is that the sync tips become compressed before the differential gain and differential phase are adversely affected. Thus, there must be adequate swing in the negative direction to pass the sync tips without compression.

As the upper supply is lowered to approach the video, the differential gain and differential phase were not significantly adversely affected until the difference between the peak video output and the supply reached 0.6 V. Thus, the highest video level should be kept at least 0.6 V below the positive supply rail.

Taking the above into account, it was found that the optimal point to bias the noninverting input is at 2.2 V dc. Operating at this point, the worst case differential gain is measured at 0.06% and the worst case differential phase is 0.06°.

The ac coupling capacitors used in the circuit at first glance appear quite large. A composite video signal has a lower frequency band edge of 30 Hz. The resistances at the various ac coupling points—especially at the output—are quite small. In order to minimize phase shifts and baseline tilt, the large value capacitors are required. For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slightly observable change in the picture quality.

Sync Stripper

Some RGB monitor systems use only three cables total and carry the synchronizing signals along with the Green (G) signal on the same cable. The sync signals are pulses that go in the negative direction from the blanking level of the G signal.

In some applications like prior to digitizing component video signals with A/D converters, it is desirable to remove or strip the sync portion from the G signal. Figure 43 is a schematic of a circuit using the AD8041 running on a single +5 V supply that performs this function.

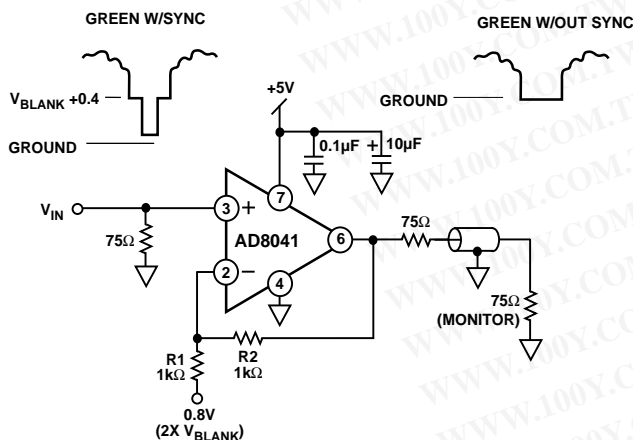


Figure 43. Single Supply Sync Stripper

Referring to Figure 44, the Green plus sync signal is output from an ADV7120, a single supply triple video DAC. Because the DAC is single supply, the lowest level of the sync tip is at ground or slightly above. The AD8041 is set for a gain of two to compensate for the divide by two of the output terminations.

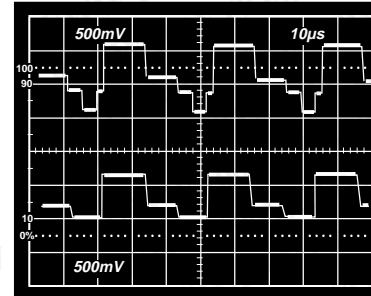


Figure 44. Single Supply Sync Stripper

The reference voltage for R1 should be twice the dc blanking level of the G signal. If the blanking level is at ground and the sync tip is negative as in some dual supply systems, then R1 can be tied to ground. In either case, the output will have the sync removed and have the blanking level at ground.

Layout Considerations

The specified high speed performance of the AD8041 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are necessary.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce the stray capacitance.

Chip capacitors should be used for the supply bypassing (see Figure 45). One end should be connected to the ground plane and the other within 1/8 inch of each power pin. An additional large (0.47 μF–10 μF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

Evaluation Board

An evaluation board for the AD8041 is available which has been carefully laid out and tested to demonstrate that the specified high speed performance of the device can be realized. For ordering information, please refer to the ordering guide.

The layout of the evaluation board can be used as shown or serve as a guide for a board layout.

Table I. Recommended Component Values

| Component | AD8041A Gain | | | | |
|------------------------|--------------|--------------|--------------|--------------|--------------|
| | +1 | +2 | +2 | +5 | +10 |
| R_F | 0 Ω | 2 k Ω | 400 Ω | 2 k Ω | 2 k Ω |
| R_G | | 2 k Ω | 400 Ω | 500 Ω | 220 Ω |
| R_O (Nominal) | 75 Ω | 75 Ω | 75 Ω | 75 Ω | 75 Ω |
| R_T (Nominal) | 75 Ω | 75 Ω | 75 Ω | 75 Ω | 75 Ω |
| Small Signal BW (MHz) | | | | | |
| $V_S = +5$ V | 160 | 67 | 72 | 20 | 9 |
| 0.1 dB Bandwidth (MHz) | | | | | |
| $V_S = +5$ V | | 7 | 32 | | |

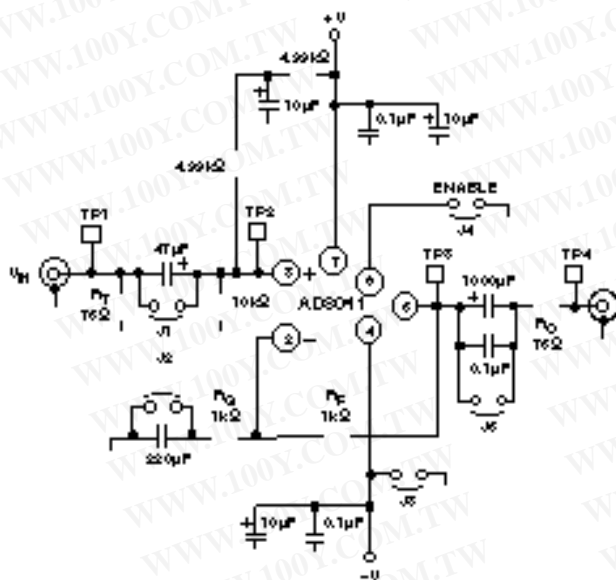


Figure 45. Noninverting Configurations for Evaluation Boards

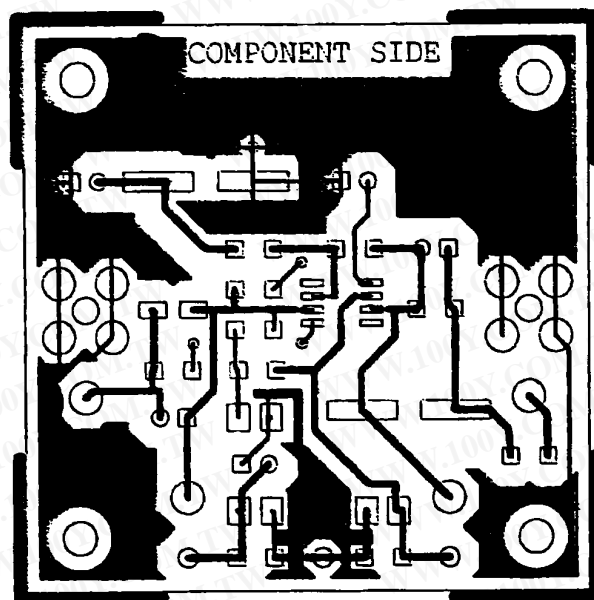
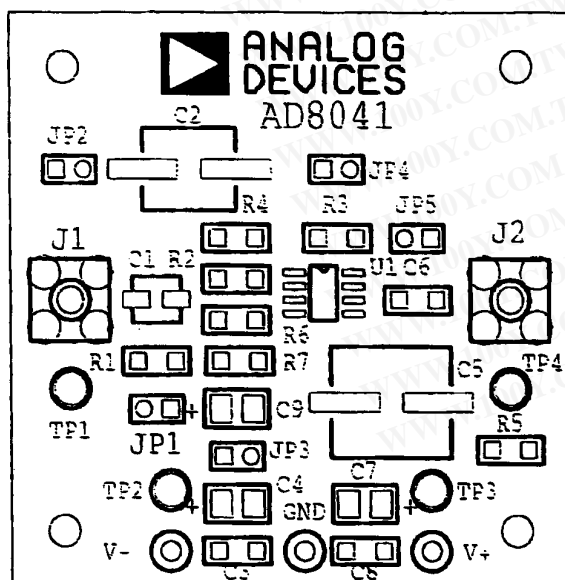


Figure 47. Board Layout (Component Side)



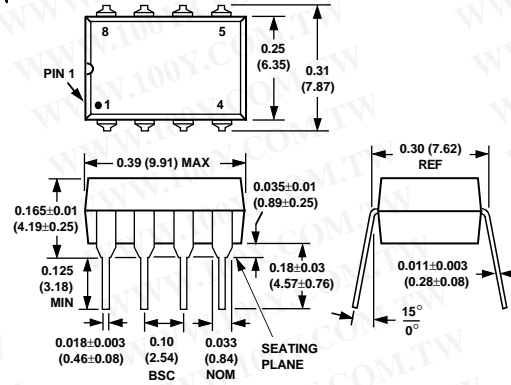
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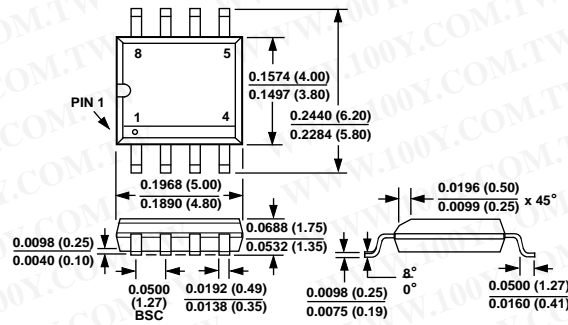
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead Plastic SOIC (SO-8)



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