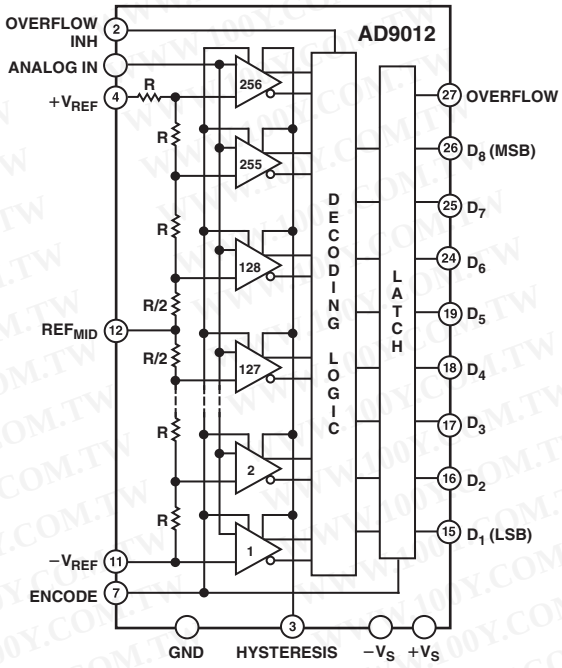
High Speed 8-Bit TTL A/D Converter

AD9012

FEATURES
100 MSPS ENCODE Rate
Very Low Input Capacitance—16 pF
Low Power—1 W
TTL Compatible Outputs
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Guidance
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9012 is an 8-bit, ultrahigh speed, analog-to-digital converter. The AD9012 is fabricated in an advanced bipolar process that allows operation at sampling rates up to 100 megasamples/second. Functionally, the AD9012 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the TTL compatible output latches.

The exceptionally wide large-signal analog input bandwidth of 160 MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9012 allows very accurate acquisition of high speed pulse inputs without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9012 is available in two grades: one with 0.5 LSB linearity and one with 0.75 LSB linearity. Both versions are offered in an industrial grade, –25°C to +85°C, packaged in a 28-lead DIP and a 28-lead JLCC. The military temperature range devices, –55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

The AD9012 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9012/883B data sheet for detailed specifications.

REV. F

AD9012–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5.0 V; $-V_S$ = –5.2 V; Differential Reference Voltage = 2.0 V; unless otherwise noted.)

Parameter	Temp	Test Level	AD9012AQ/AJ Min	AD9012AQ/AJ Typ	AD9012AQ/AJ Max	AD9012BQ/BJ Min	AD9012BQ/BJ Typ	AD9012BQ/BJ Max	AD9012SQ/SE Min	AD9012SQ/SE Typ	AD9012SQ/SE Max	AD9012TQ/TE Min	AD9012TQ/TE Typ	AD9012TQ/TE Max	Unit
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Linearity	25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Linearity	25°C	I		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			Guaranteed			Guaranteed			
INITIAL OFFSET ERROR															
Top of Reference Ladder	25°C	I		7	15		7	15		7	15		7	15	mV
	Full	VI			18			18			18			18	mV
Bottom of Reference Ladder	25°C	I		6	10		6	10		6	10		6	10	mV
	Full	VI			13			13			13			13	mV
Offset Drift Coefficient	Full	V		25			25			25			25		µV/°C
ANALOG INPUT															
Input Bias Current[1]	25°C	I		60	200		60	200		60	200		60	200	µA
	Full	VI			200			200			200			200	µA
Input Resistance	25°C	I	25	200		25	200		25	200		25	200		kΩ
Input Capacitance	25°C	III		16	18		16	18		16	18		16	18	pF
Large Signal Bandwidth[2]	25°C	V		160			160			160			160		MHz
Analog Input Slew Rate[3]	25°C	V		440			440			440			440		V/µs
REFERENCE INPUT															
Reference Ladder Resistance	25°C	VI	40	80	110	40	80	110	40	80	110	40	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	25°C	I	75	100		75	100		75	100		75	100		MSPS
Aperture Delay	25°C	V		3.8			3.8			3.8			3.8		ns
Aperture Uncertainty (Jitter)	25°C	V		15			15			15			15		ps
Output Delay (t_{PD})[4, 5]	25°C	I	4	4.9	11	4	4.9	11	4	4.9	11	4	4.9	11	ns
Transient Response[6]	25°C	V		8			8			8			8		ns
Overvoltage Recovery Time[7]	25°C	V		8			8			8			8		ns
Output Rise Time[4]	25°C	I		6.6	8.0		6.6	8.0		6.6	8.0		6.6	8.0	ns
Output Fall Time[4]	25°C	I		3.3	4.3		3.3	4.3		3.3	4.3		3.3	4.3	ns
Output Time Skew[4, 8]	25°C	V		3.0			3.0			3.0			3.0		ns
ENCODE INPUT															
Logic "1" Voltage[4]	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage[4]	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			250			250			250			250	µA
Logic "0" Current	Full	VI			400			400			400			400	µA
Input Capacitance	25°C	V		2.5			2.5			2.5			2.5		pF
ENCODE Pulsewidth (Low)[9]	25°C	I	2.5			2.5			2.5			2.5			ns
ENCODE Pulsewidth (High)[9]	25°C	I	2.5			2.5			2.5			2.5			ns
OVERFLOW INHIBIT INPUT															
0 V Input Current	Full	VI		200	250		200	250		200	250		200	250	µA
AC LINEARITY[10]															
Effective Bits[11]	25°C	V		7.5			7.5			7.5			7.5		Bits
In-Band Harmonics															
DC to 1.23 MHz	25°C	I	48	55		48	55		48	55		48	55		dBc
DC to 9.3 MHz	25°C	V		50			50			50			50		dBc
DC to 19.3 MHz	25°C	V		44			44			44			44		dBc
Signal-to-Noise Ratio[12]	25°C	I	46	47.6		46	47.6		46	47.6		46	47.6		dBc
Noise Power Ratio[13]	25°C	V		37			37			37			37		dBc
DIGITAL OUTPUT															
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.4			0.4			0.4			0.4	V
POWER SUPPLY[14]															
Positive Supply Current (+5.0 V)	25°C	I		33	45		33	45		33	45		33	45	mA
	Full	VI			48			48			48			48	mA
Supply Current (–5.2 V)	25°C	I		152	179		152	179		152	179		152	179	mA
	Full	VI			191			191			191			191	mA
Nominal Power Dissipation	25°C	V		955			955			955			955		mW
Reference Ladder Dissipation	25°C	V		44			44			44			44		mW
Power Supply Rejection Ratio[15]	25°C	I		0.85	2.5		0.85	2.5		0.8	2.5		0.8	2.5	mV/V

NOTES
[1]Measured with analog input = 0 V.
[2]Measured by FFT analysis where fundamental is –3 dBc.
[3]Input slew rate derived from rise time (10% to 90%) of full-scale step input.
[4]Outputs terminated with two equivalent 'LS00 type loads. (See load circuit.)
[5]Measured from ENCODE into data out for LSB only.
[6]For full-scale step input, 8-bit accuracy is attained in specified time.
[7]Recovers to 8-bit accuracy in specified time, after 150% full-scale input overvoltage.
[8]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.
[9]ENCODE signal rise/fall times should be less than 30 ns for normal operation.
[10]Measured at 75 MSPS ENCODE rate. Harmonic data based on worst-case harmonics.
[11]Analog input frequency = 1.23 MHz.
[12]RMS signal to rms noise, including harmonics with 1.23 MHz. Analog input signal.
[13]NPR measured @ 0.5 MHz. Noise source is 250 mW (rms) from 0.5 MHz to 8 MHz.
[14]Supplies should remain stable within ±5% for normal operation.
[15]Measured at –5.2 V ±5% and +5.0 V ±5%.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . 6 V
Analog to Digital Supply Voltage Differential ($-V_S$) . . . 0.5 V
Negative Supply Voltage ($-V_S$) . . . . . –6 V
Analog Input Voltage . . . . . $-V_S$ to +0.5 V
ENCODE Input Voltage . . . . . –0.5 V to +5 V
OVERFLOW INH Input Voltage . . . . . –5.2 V to 0 V
Reference Input Voltage ($+V_{REF}$, $-V_{REF}$)[2] . . –3.5 V to +0.1 V
Differential Reference Voltage . . . . . 2.1 V
Reference Midpoint Current . . . . . ±4 mA
Digital Output Current . . . . . 30 mA
Operating Temperature Range
AD9012AQ/BQ/AJ/BJ . . . . . –25°C to +85°C
AD9012SE/SQ/TE/TQ . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature[3] . . . . . 150°C
Lead Soldering Temperature (10 sec) . . . . . 300°C

NOTES
[1]Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.
[3]Maximum junction temperature (T_J max) should not exceed 150°C for ceramic and plastic packages:
$T_J = PD\ (\theta_{JA}) + T_A$
$PD\ (\theta_{JC}) + Tc$
where:
PD = power dissipation
θ_{JA} = thermal impedance from junction to ambient (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
T_A = ambient temperature (°C)
T_C = case temperature (°C)
Typical thermal impedances are:
Ceramic DIP θ_{JA} = 42°C/W; θ_{JC} = 10°C/W
Ceramic LCC θ_{JA} = 50°C/W; θ_{JC} = 15°C/W
JLCC θ_{JA} = 59°C/W; θ_{JC} = 15°C/W

Recommended Operating Conditions

Parameter	Input Voltage (V)		
	Min	Nominal	Max
$-V_S$	–5.46	–5.20	–4.94
$+V_S$	+4.75	+5.00	+5.25
$+V_{REF}$	$-V_{REF}$	0.0	+0.1
$-V_{REF}$	–2.1	–2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

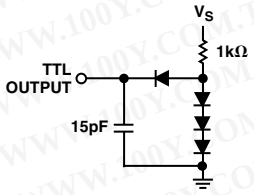


Figure 1. Load Circuit

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at 25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for extended temperature devices; guaranteed by design and characterization testing for industrial devices.

ORDERING GUIDE

Device	Linearity	Temperature Ranges	Package Options*
AD9012AQ	0.75 LSB	–25°C to +85°C	Q-28
AD9012BQ	0.50 LSB	–25°C to +85°C	Q-28
AD9012AJ	0.75 LSB	–25°C to +85°C	J-28A
AD9012BJ	0.50 LSB	–25°C to +85°C	J-28A
AD9012SQ	0.75 LSB	–55°C to +125°C	Q-28
AD9012SE	0.75 LSB	–55°C to +125°C	E-28A
AD9012TQ	0.50 LSB	–55°C to +125°C	Q-28
AD9012TE	0.50 LSB	–55°C to +125°C	E-28A

*E = Leadless Ceramic Chip Carrier; J = Ceramic Leaded Chip Carrier; Q = Cerdip.

CAUTION

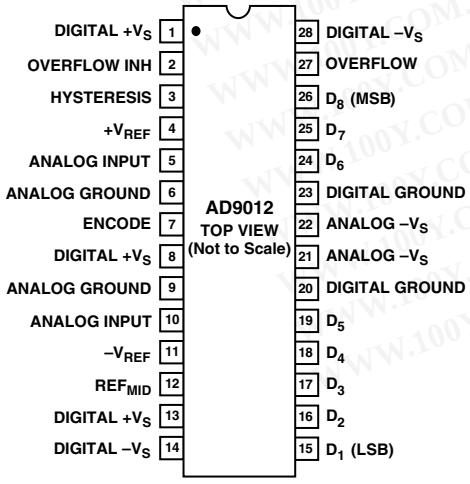
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9012 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

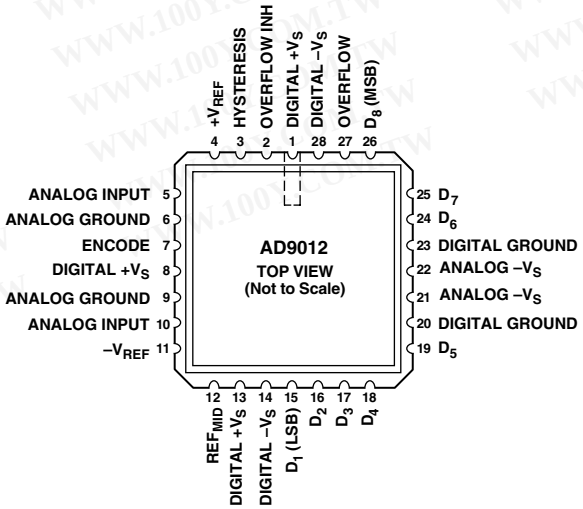
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DIGITAL $+V_S$	One of Three Positive Digital Supply Pins (Nominally 5.0 V)
2	OVERFLOW INH	OVERFLOW INH BIT controls the data output coding for overvoltage inputs (AIN ≥ + V_{REF}).
3	HYSTERESIS	The hysteresis control voltage varies the comparator hysteresis from 0 mV to 10 mV, for a change from –5.2 V to –2.2 V at the hysteresis control pin.
4	$+V_{REF}$	The Most Positive Reference Voltage for the Internal Resistor Ladder
5	ANALOG INPUT	One of Two Analog Input Pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of Two Analog Ground Pins. Both analog ground pins should be connected together.
7	ENCODE	TTL Level ENCODE Command Input. ENCODE is rising edge sensitive.
8	DIGITAL $+V_S$	One of Three Positive Digital Supply Pins (Nominally +5.0 V)
9	ANALOG GROUND	One of Two Analog Ground Pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of Two Analog Input Pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The Most Negative Reference Voltage for the Internal Resistor Ladder
12	REF_{MID}	The Midpoint Tap on the Internal Resistor Ladder
13	DIGITAL $+V_S$	One of Three Positive Digital Supply Pins (Nominally +5.0 V)
14	DIGITAL $-V_S$	One of Two Negative Digital Supply Pins (Nominally –5.2 V). Both digital supply pins should be connected together.
15	D_1 (LSB)	Digital Data Output. D_1 (LSB) is the least significant bit of the digital output word.
16–19	D_2–D_5	Digital Data Output
20	DIGITAL GROUND	One of Two Digital Ground Pins. Both digital grounds pins should be connected together.
21, 22	ANALOG $-V_S$	One of Two Negative Analog Supply Pins (Nominally –5.2 V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of Two Digital Ground Pins. Both digital ground pins should be connected together.
24, 25	D_6, D_7	Digital Data Output
26	D_8 (MSB)	Digital data output D_8 (MSB) is the most significant bit of the digital output word.
27	OVERFLOW	Overflow Data Output. Logic HIGH indicates an input overvoltage (V_{IN} > + V_{REF}) if OVERFLOW INH is enabled (overflow enabled, floating). See OVERFLOW INH.
28	DIGITAL $-V_S$	One of Two Negative Digital Supply Pins (Nominally –5.2 V). Both digital supply pins should be connected together.

Analog Input	Overflow Enabled (Floating) of D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8	Overflow Inhibited (GND) of D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
V_{IN} + V_{REF}	1 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1
V_{IN} < + V_{REF}	0 X X X X X X X X	0 X X X X X X X X

PIN CONFIGURATIONS





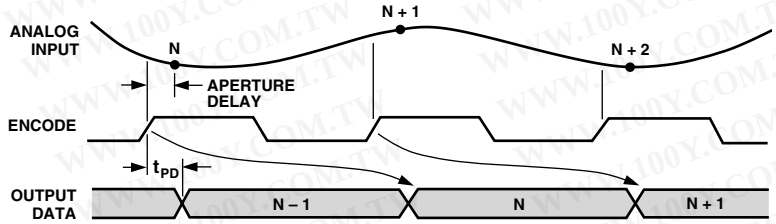


Figure 2. Timing Diagram

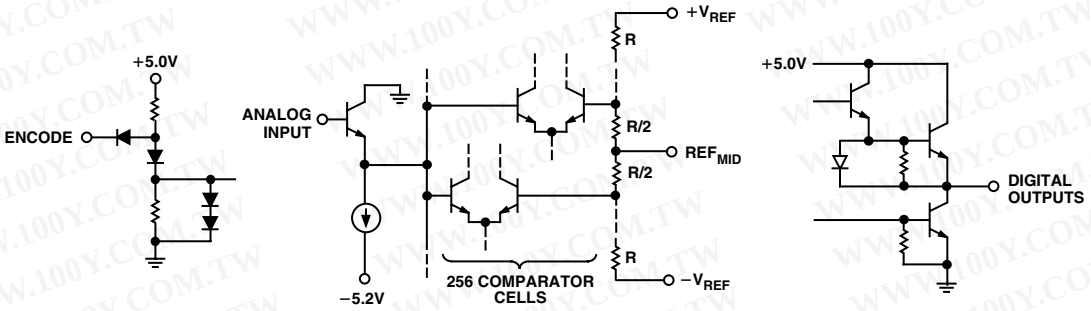
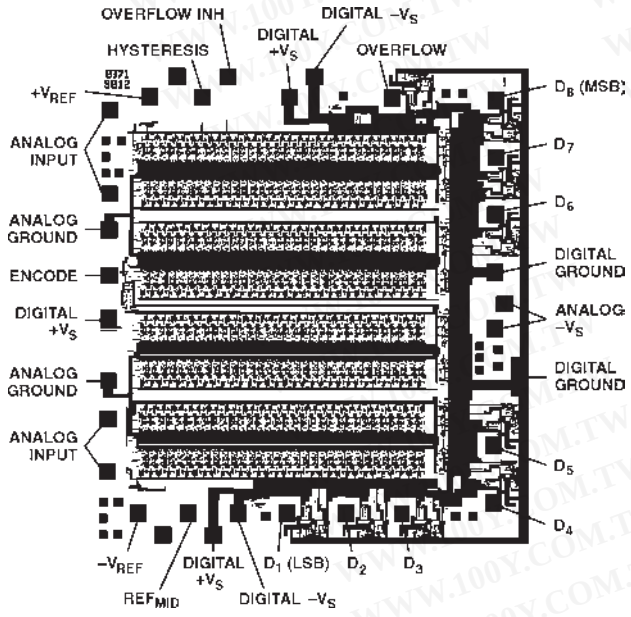


Figure 3. Input Output Circuits

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions . . . . . 111 mils × 123 mils × 15 mils (±2) mils
Pad Dimensions . . . . . 4 mils × 4 mils
Metallization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . –V_S
Passivation . . . . . Nitride
Die Attach . . . . . Gold Eutectic (Ceramic)
. . . . . Epoxy (Plastic)
Bond Wire . . . . . 1 mil to 1.3 mil Gold; Gold Ball Bonding

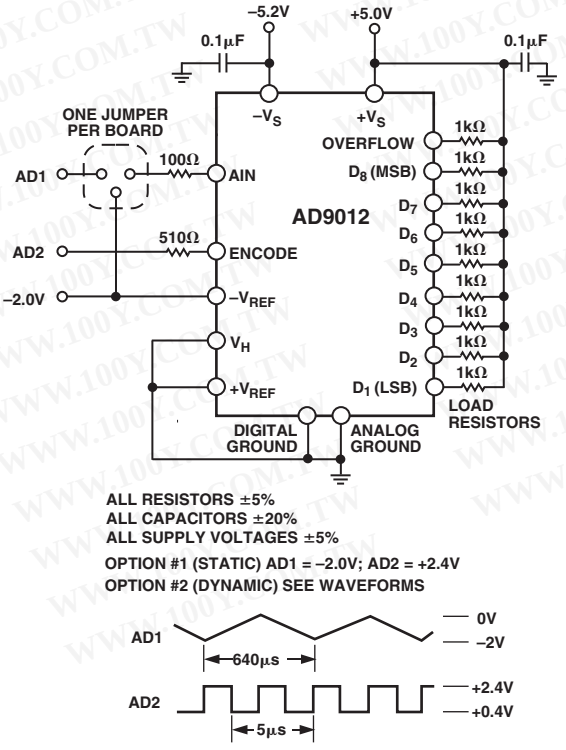


Figure 4. Burn-In Diagram

APPLICATION INFORMATION

The AD9012 is compatible with all standard TTL logic families. However, to operate at the highest ENCODE rates, the supporting logic around the AD9012 will need to be equally fast. Two possible choices are the AS and the ALS families. Whichever of the TTL logic families is used, special care must be exercised to keep digital switching noise away from the analog circuits around the AD9012. The two most critical items are the digital supply lines and the digital ground return.

The input capacitance of the AD9012 is an exceptionally low 16 pF. This allows the use of a wide range of input amplifiers, both hybrid and monolithic. To take full advantage of the 160 MHz input bandwidth of the AD9012, a hybrid amplifier such as the AD9610 will be required. For those applications that do not require the full input bandwidth of the AD9012, some of the more traditional monolithic amplifiers, such as the AD846, should work very well. Overall performance with monolithic amplifiers can be improved by inserting a 40 Ω resistor in series with the amplifier output.

The output data is buffered through the TTL compatible output latches. In addition to the latch propagation delay (t_{PD}), all data is delayed by one clock cycle before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches are triggered on the rising edge of the TTL compatible ENCODE signal (see Figure 2).

The AD9012 also incorporates a HYSTERESIS control pin that provides from 0 mV to 10 mV of additional hysteresis in the comparator input stages. Adjustments in the HYSTERESIS control voltage may help to improve noise immunity and overall performance in harsh environments.

The OVERFLOW INH pin of the AD9012 determines how the converter handles overrange inputs (AIN ≥ + V_{REF}). In the "enabled" state (floating at –5.2 V), the OVERFLOW INH output will be at logic HIGH and all other outputs will be at logic LOW for overrange inputs (return-to-zero operation). In the "inhibited" state (tied to ground), the OVERFLOW INH output will be at logic LOW for overrange inputs, and all other digital outputs will be at logic HIGH (nonreturn-to-zero operation).

The AD9012 provides outstanding error rate performance. This is due to tight control of comparator offset matching and a fault tolerant decoding stage. Additional improvements in error rate are possible through the addition of hysteresis (see HYSTERESIS control pin). This level of performance is extremely important in fault sensitive applications, such as digital radio (QAM).

Dramatic improvements in comparator design and construction give the AD9012 excellent dynamic characteristics, namely SNR (signal-to-noise ratio). The 160 MHz input bandwidth and low error rate performance give the AD9012 an SNR of 47 dB with a 1.23 MHz input. High SNR performance is particularly important in broadcast video applications where signals may pass through the converter several times before the processing is complete. Pulse signature analysis, commonly performed in advanced radar receivers, is another area that is especially dependent on high quality dynamic performance.

LAYOUT SUGGESTIONS

Designs using the AD9012, such as all high speed devices, must follow a few basic layout rules to ensure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high speed designs. The first requirement is for a substantial ground plane around and under the AD9012. Separate ground plane areas for the digital and analog components may be useful, but the separate grounds should be connected together at the AD9012 to avoid the effects of "ground loop" currents.

The second area that requires an extra degree of attention involves the three reference inputs, $+V_{REF}$, REF_{MID}, and $-V_{REF}$. The $+V_{REF}$ input and the $-V_{REF}$ input should both be driven from a low impedance source (note that the $+V_{REF}$ input is typically tied to analog ground). A low drift amplifier should provide satisfactory results, even over an extended temperature range. Adjustments at the REF_{MID} input may be useful in improving the integral linearity by correcting any reference ladder skews.

The reference inputs should be adequately decoupled to ground through 0.1 µF chip capacitors to limit the effects of system noise on conversion accuracy. The power supply pins must also be decoupled to ground to improve noise immunity; 0.1 µF and 0.01 µF chip capacitors should be very effective.

The analog input signal is brought into the AD9012 through two separate input pins. It is very important that the two input pins be driven symmetrically with equal length electrical connections. Otherwise, aperture delay errors may degrade converter performance at high frequencies.

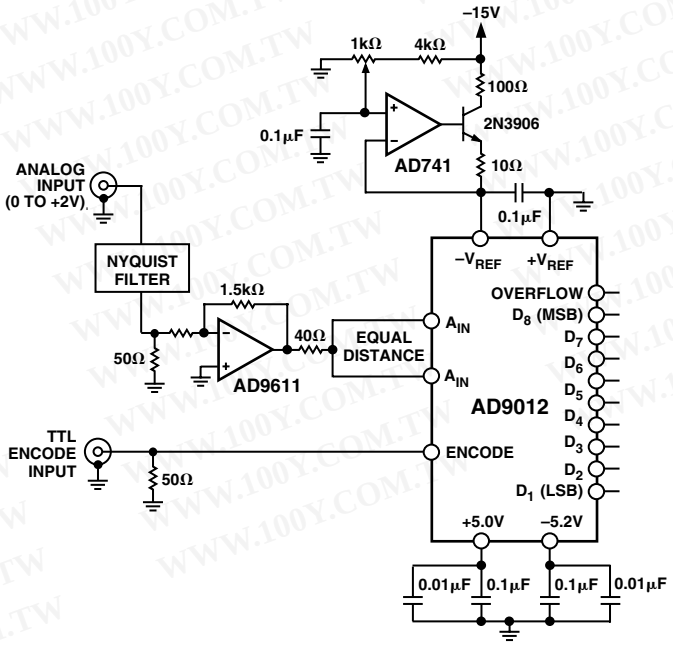


Figure 5. Typical Application

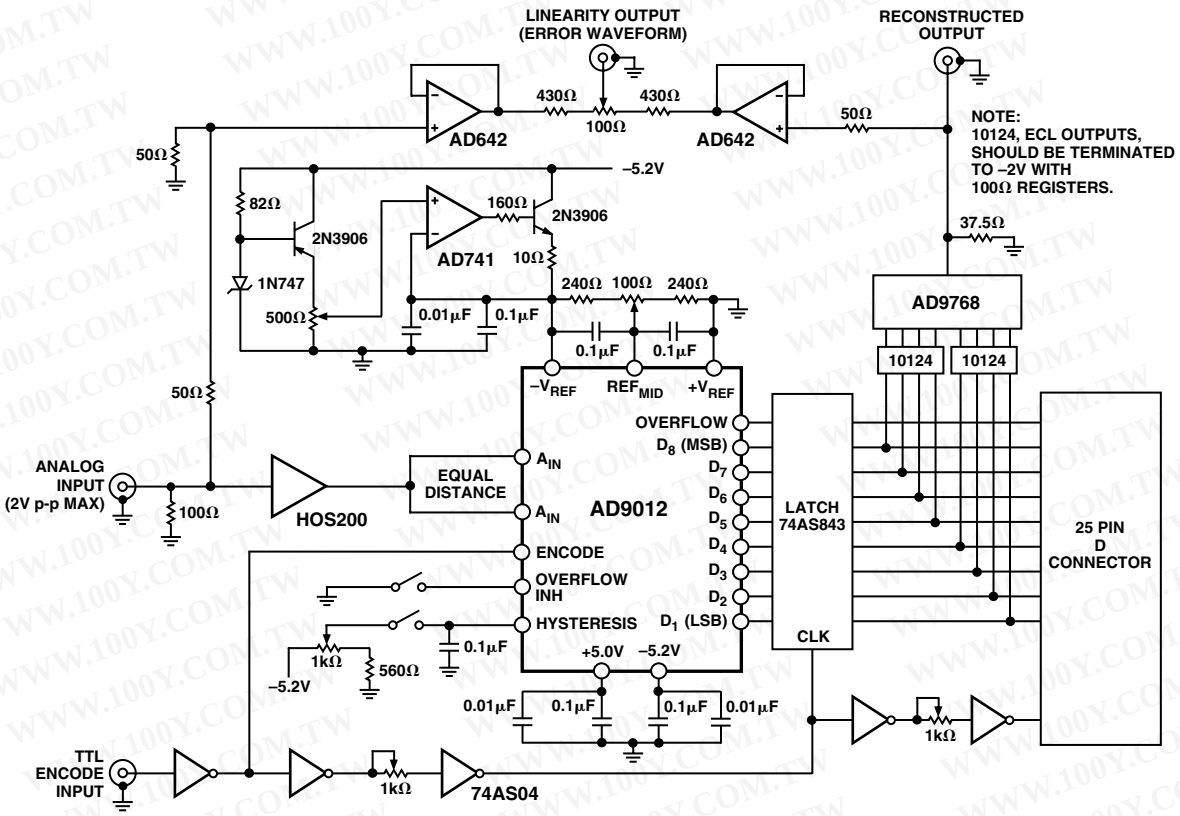


Figure 6. Evaluation Circuit

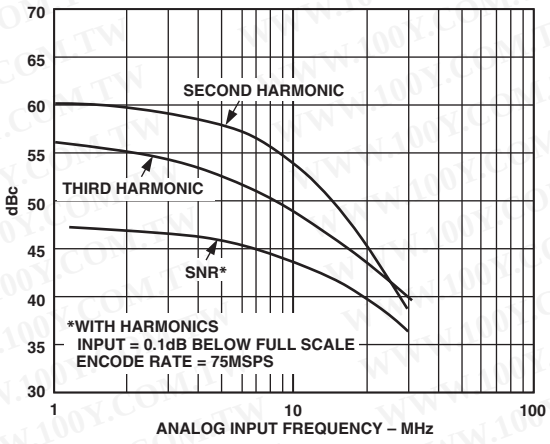
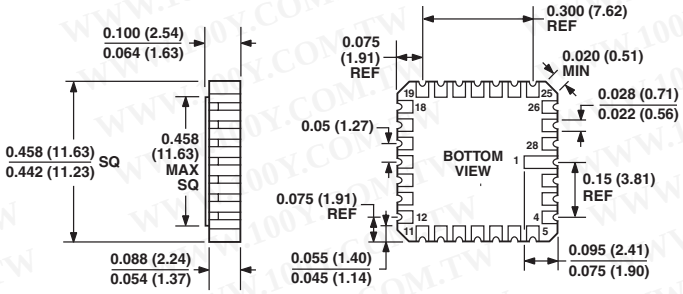


Figure 7. Dynamic Performance

OUTLINE DIMENSIONS

28-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-28A)

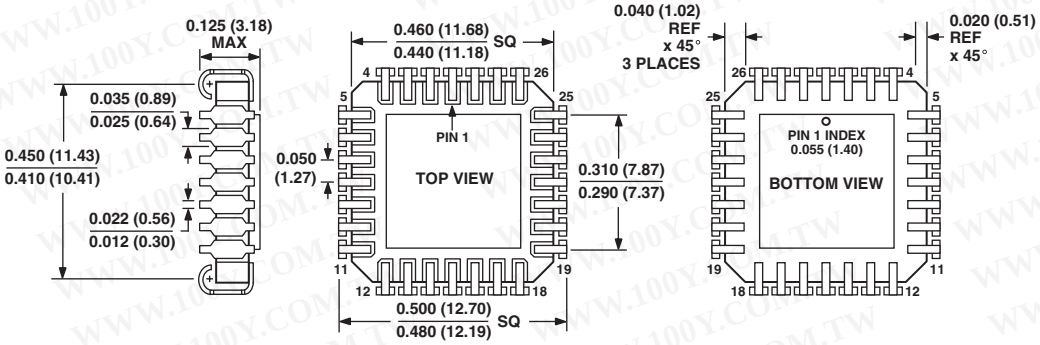
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Ceramic Leaded Chip Carrier – J-Formed Lead [JLCC]
(J-28A)

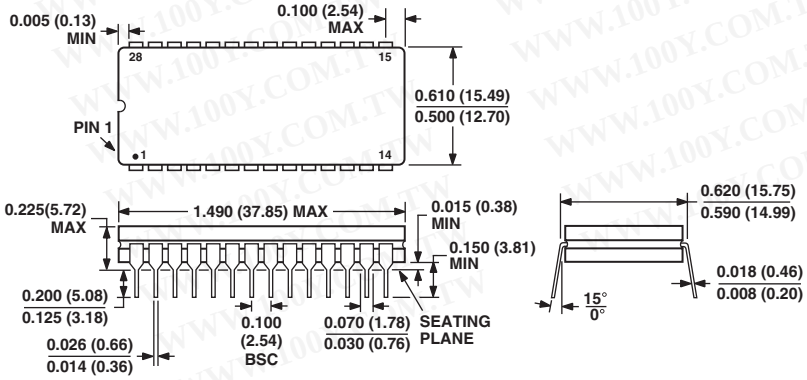
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-28)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page

5/03—Data Sheet changed from REV. E to REV. F.